

JEDEC STANDARD

GRAPHICS DOUBLE DATA RATE (GDDR5X) SGRAM STANDARD

JESD232A.01

(Revision of JESD232A, August 2016)

SEPTEMBER 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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GRAPHICS DOUBLE DATA RATE (GDDR5X) SGRAM STANDARD

(From JEDEC Board Ballot JCB-16-39, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories, item number 1827.99B v1.2).

1 SCOPE

This standard defines the GDDR5X SGRAM memory standard, including features, device operation, electrical characteristics, timings, signal pin assignments, and package.

The purpose of this standard is to define the minimum set of requirements for JEDEC standard compatible 4 Gb through 16 Gb x32 GDDR5X SGRAM devices. System designs based on the required aspects of this standard will be supported by all GDDR5X SGRAM vendors providing JEDEC standard compatible devices. Some aspects of the GDDR5X standard such as AC timings were not standardized. Some features are optional and therefore may vary among vendors. In all cases, vendor data sheets should be consulted for specifics.

This standard was created based on the GDDR5 SGRAM standard (JESD212). Each aspect of the changes were considered and balloted. The accumulation of these ballots were then incorporated to prepare this GDDR5X SGRAM standard.

2 GDDR5X SGRAM STANDARD OVERVIEW

4 Gb = 128 Mb x 32 (8 Mb x 32 x 16 banks) / 256 Mb x 16 (16 Mb x 16 x 16 banks)
6 Gb = 192 Mb x 32 (12 Mb x 32 x 16 banks) / 384 Mb x 16 (24 Mb x 16 x 16 banks)
8 Gb = 256 Mb x 32 (16 Mb x 32 x 16 banks) / 512 Mb x 16 (32 Mb x 16 x 16 banks)
12 Gb = 384 Mb x 32 (24 Mb x 32 x 16 banks) / 768 Mb x 16 (48 Mb x 16 x 16 banks)
16 Gb = 512 Mb x 32 (32 Mb x 32 x 16 banks) / 1 Gb x 16 (64 Mb x 16 x 16 banks)

2.1 FEATURES

- Single ended interface for command, address and data
- Differential clock input CK_t/CK_c for ADD/CMD
- Two differential clock inputs WCK_t/WCK_c, each associated with two data bytes (DQ, DBI_n, EDC)
- Single Data Rate (SDR) commands (CK)
- Double Data Rate (DDR) addresses (CK)
- QDR and DDR operating modes:
 - QDR mode: Quad Data Rate (QDR) data (WCK); 16n prefetch architecture with 512 bit per array read or write access; burst length 16
 - DDR mode: Double Data Rate (DDR) data (WCK); 8n prefetch architecture with 256 bit per array read or write access; burst length 8
- 16 internal banks
- 4 bank groups for t_{CCDL} = 3 t_{CK} and 4 t_{CK}
- Programmable read latency: 5 to 36 t_{CK}; programmable write latency: 1 to 7 t_{CK}
- Write data mask function via address bus (single/double/quad byte mask)
- Data bus inversion (DBI) and address bus inversion (ABI)
- Input/output PLL/DLL
- Address training: address input monitoring via DQ/DBI_n/EDC pins
- WCK2CK clock training with phase information via EDC pins
- Data read and write training via READ FIFO (depth = 6)
- Read FIFO pattern preload by LDFF command
- Direct write data load to READ FIFO via WRTR command
- Consecutive read of READ FIFO via RDTR command
- Read/write EDC on/off mode
- Programmable EDC hold pattern for CDR
- Read/write data transmission integrity secured by cyclic redundancy check (CRC-8)
- Programmable CRC read latency = 1 to 4 t_{CK}; programmable CRC write latency = 7 to 14 t_{CK}
- Low Power modes
- RDQS mode on EDC pins
- On-chip temperature sensor with read-out
- Auto precharge option for each burst access
- Auto refresh mode with per-bank refresh option
- Temperature sensor controlled self refresh rate
- Optional digital t_{RAS} lockout
- On-die termination (ODT) for all high-speed inputs
- Pseudo open drain (POD-135) compatible outputs
- ODT and output driver strength auto-calibration with external resistor ZQ pin (120 Ω)
- Programmable termination and driver strength offsets
- Internal V_{REF} for data inputs with programmable levels
- Selectable external or internal V_{REF} for address / command inputs
- Vendor ID for device identification
- Mirror function with MF pin
- IEEE 1149.1 compliant boundary scan
- 1.35 V supply voltage for device operation (V_{DD}) and I/O interface (V_{DDQ})
- 1.8 V pump voltage (V_{PP})
- 190 ball BGA package

3 FUNCTIONAL DESCRIPTION

3.1 FUNCTIONAL OVERVIEW

The GDDR5X SGRAM is a high speed dynamic random-access memory designed for applications requiring high bandwidth. It is internally configured as 16-bank memory and contains the following number of bits:

4 Gb has 4,294,967,296 bits
6 Gb has 6,442,450,944 bits
8 Gb has 8,589,934,592 bits
12 Gb has 12,884,901,888 bits
16 Gb has 17,179,869,184 bits

The GDDR5X SGRAM's high-speed interface is optimized for point-to-point connections to a host controller. On-die termination (ODT) is provided for all high-speed interface signals to eliminate the need for termination resistors in the system.

The GDDR5X SGRAM supports two operating modes which mainly differ in the internal prefetch and DQ/DBI_n pin to WCK clock frequency ratio. The operating mode is set by a mode register bit:

- In Quad Data Rate (QDR) mode the interface transfers four 32-bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 16-n prefetch a single write or read access consists of a 512 bit wide, two CK clock cycle data transfer at the internal memory core and sixteen corresponding 32 bit wide one-quarter WCK clock cycle data transfers to the I/O pins.
- In Double Data Rate (DDR) mode the interface transfers two 32-bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 8-n prefetch a single write or read access consists of a 256 bit wide, two CK clock cycle data transfer at the internal memory core and eight corresponding 32 bit wide one-half WCK clock cycle data transfers to the I/O pins.

Read and write accesses to the GDDR5X SGRAM are burst oriented; an access starts at a selected location and consists of a total of sixteen data words in QDR mode and eight data words in DDR mode. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command and the next rising CK_c edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising CK_c edge are used to select the bank and the column location for the burst access.

This standard includes all features and functionality required for JEDEC GDDR5X SGRAM devices. Users benefit from knowing that any system design based on the required aspects of the standard are supported by all GDDR5X SGRAM vendors; conversely users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

3.2 SIGNAL STATE TERMINOLOGY

The GDDR5X SGRAM will be operated in both ODT enable (terminated) and ODT disable (unterminated) modes. For highest data rates it is recommended to operate in the ODT enable mode. ODT disable mode is designed to reduce power and may operate at reduced data rates. There exist situations where ODT enable mode can not be guaranteed for a short period of time, for example during power-up.

Four terminologies define the state of a device pin (GDDR5X SGRAM or controller) during operation. The state of the bus will be determined by the combination of the device pins connected to the bus in the system. For example, with GDDR5X it is possible for the device pin to be tristated while the controller pin is High or ODT. In both cases the bus would be High if the ODT is enabled.

Device pin signal level:

- High: a device pin drives the Logic “1” state.
- Low: a device pin drives the Logic “0” state.
- High-Z: a device pin is tristate.
- ODT: a device pin terminates with ODT setting, which could be terminating or tristate depending on mode register setting.

Bus signal level:

- High: one device on the bus is High and all other devices on bus are either ODT or High-Z. The voltage level on the bus would be nominally V_{DDQ} .
- Low: one device on the bus is Low and all other devices on bus are either ODT or High-Z. The voltage level on the bus would be nominally $V_{OL}(DC)$ if ODT is enabled, or V_{SSQ} if High -Z.
- High-Z: all devices on the bus are High-Z. The voltage level on bus is undefined as the bus is floating.
- ODT: at least one device on the bus is ODT and all others are High-Z. The voltage level on the bus would be nominally V_{DDQ} .

3.3 CLOCKING

The GDDR5X SGRAM operates from a differential clock CK_t and CK_c. Commands are registered at every rising edge of CK_t. Addresses are registered at every rising edge of CK_t and every rising edge of CK_c.

The data interface uses two differential forwarded clocks WCK_t and WCK_c, each associated with two data bytes. WCK_t and WCK_c are continuously running and operate at twice the frequency of the command/address clock (CK_t/CK_c). A PLL/DLL is associated with each WCK pair. The use of the PLL/DLL is mandatory in QDR mode and vendor specific in DDR mode.

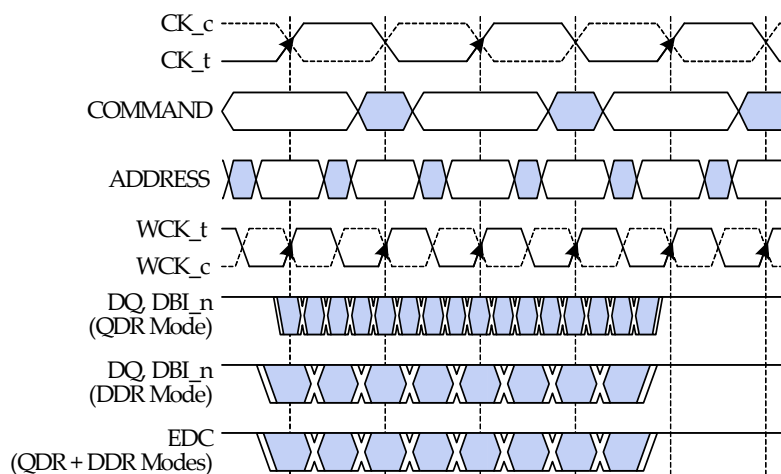
- QDR mode uses a quad data rate data interface and a 16n-prefetch architecture for DQ/DBI_n, and a double data rate data interface and 8n-prefetch architecture for EDC. The PLL/DLL generates four equally spaced clock edges per WCK clock cycle. QDR means that four DQ/DBI_n data words per WCK cycle are registered at these internally generated clock edges. DDR means that two EDC data words per WCK cycle are registered at every second of these internally generated clock edges.
- DDR mode uses a double data rate data interface and an 8n-prefetch architecture for DQ/DBI_n/EDC. DDR means that the data is registered at every rising edge of WCK_t and rising edge of WCK_c.

3.3 CLOCKING (cont'd)

Table 1 and Figure 1 illustrate the clock and interface signal relationship for both QDR and DDR operating modes.

Table 1 — Example Clock and Interface Signal Frequency Relationship

PIN	QDR MODE	DDR MODE	UNIT
CK_t, CK_c	1.5	1.5	GHz
Command	1.5	1.5	Gbps/pin
Address	3.0	3.0	Gbps/pin
WCK_t, WCK_c	3.0	3.0	GHz
DQ, DBI_n	12.0	6.0	Gbps/pin
EDC	6.0	6.0	Gbps/pin



NOTE 1 Figure 1 shows the relationship between the data rate of the buses and the clocks and is not a timing diagram.

Figure 1 — GDDR5X Clocking and Interface Relationship

3.3 CLOCKING (cont'd)

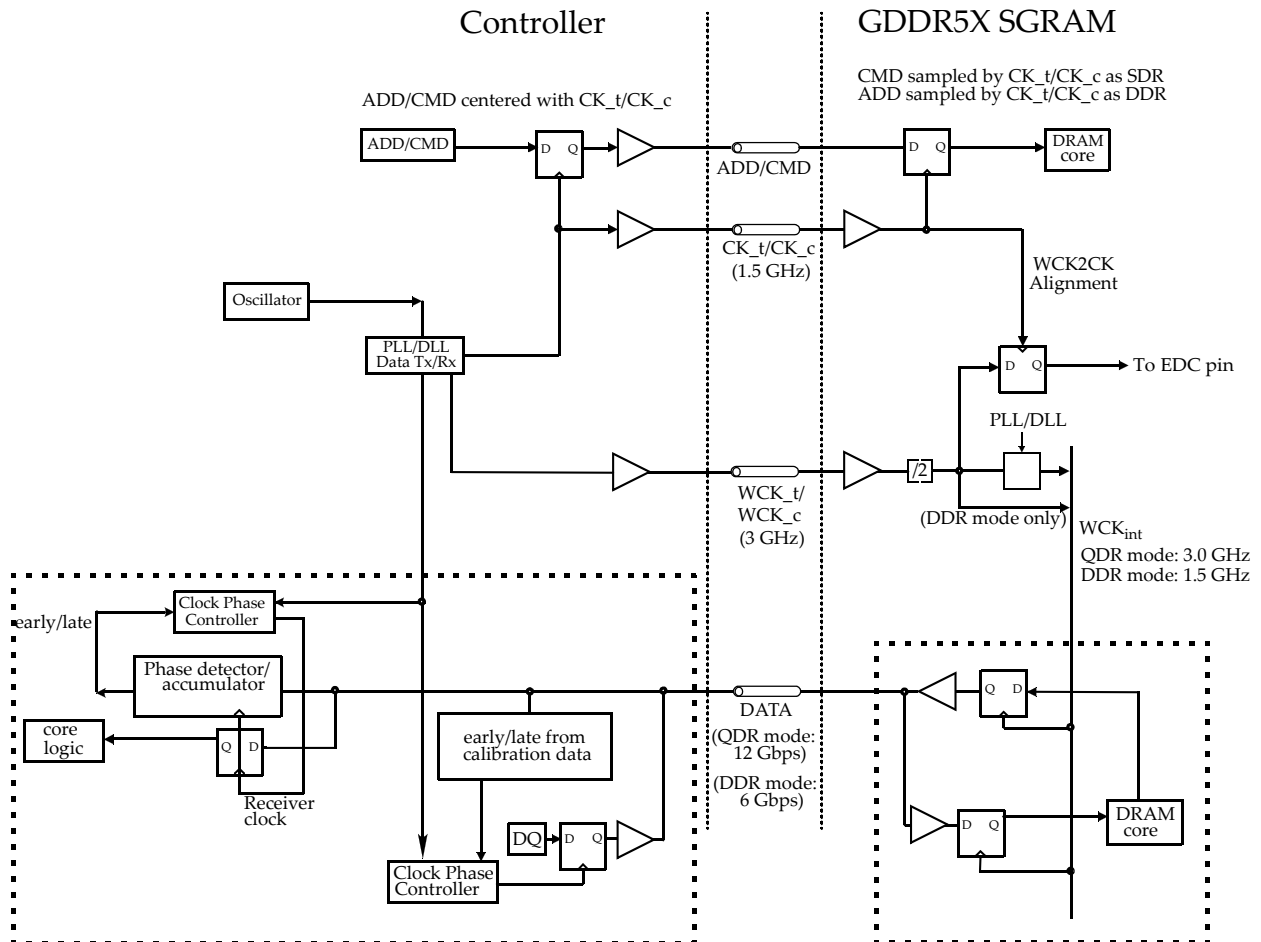


Figure 2 — Block Diagram of an Example Clock System

3.4 ADDRESSING

GDDR5X SGRAMs use a double data rate address scheme to reduce pins required on the device as shown in Table 2. The addresses should be provided in two parts; the first half is latched on the rising edge of CK_t along with the command pins such as RAS_n, CAS_n and WE_n; the second half is latched on the next rising edge of CK_c.

The use of DDR addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned for latching on the initial rising edge for faster decoding.

Table 2 — Address Pairs

Clock	Address Pins									
Rising CK _t	BA3	BA2	BA1	BA0	A14	A12	A11	A10	A9	A8
Rising CK _c	A3	A4	A5	A2	A15	A13	A6	A0	A1	A7

The addressing includes support for 4 Gb to 16 Gb densities and both QDR and DDR operating modes as shown in Table 3.

Table 3 — Addressing Scheme

Density		4 Gb		6 Gb		8 Gb		12 Gb		16 Gb	
I/O Configuration		x32	x16	x32	x16	x32	x16	x32	x16	x32	x16
Row address		A0~A12	A0~A13	A0~A13	A0~A14	A0~A13	A0~A14	A0~A14	A0~A15	A0~A14	A0~A15
Column address DQ[15:0]	QDR Mode	A0~A5		A0~A5		A0~A5		A0~A5		A0~A5	
	DDR Mode	A0~A6		A0~A6		A0~A6		A0~A6		A0~A6	
Column address DQ[31:16]	QDR Mode	A7,A9,A12~A15		A7,A9,A12~A15		A7,A9,A12~A15		A7,A9,A12~A15		A7,A9,A12~A15	
	DDR Mode	A7,A9,A12~A15,A6		A7,A9,A12~A15,A6		A7,A9,A12~A15,A6		A7,A9,A12~A15,A6		A7,A9,A12~A15,A6	
Bank address		BA0~BA3		BA0~BA3		BA0~BA3		BA0~BA3		BA0~BA3	
Autoprecharge		A8		A8		A8		A8		A8	
Page Size		4K	2K	4K	2K	4K	2K	4K	2K	4K	2K
Refresh		16K/32 ms		16K/32 ms		16K/32 ms		16K/32 ms		16K/32 ms	
Refresh period		1.9 μs		1.9 μs		1.9 μs		1.9 μs		1.9 μs	
NOTE 1	The burst order is fixed for Reads and Writes, and the GDDR5X SGRAM does not assign column address bits to distinguish between the UIs of a burst. A memory controller may internally assign such column address bits but these column address bits are not transmitted on the column address bus to the GDDR5X SGRAM.										
NOTE 2	Row address range with A[13:12] = 11 (x32 mode) or A[14:13] = 11 (x16 mode) is not present for 6 Gb density. Row address range with A[14:13] = 11 (x32 mode) or A[15:14] = 11 (x16 mode) is not present for 12 Gb density. ACT/RD/WR commands to these memory locations are illegal.										
NOTE 3	Two column addresses CAL and CAU with shared bank addresses are provided with each WRITE and READ command.										
NOTE 4	For complete details on refresh refer to the vendor's datasheets for values for refresh interval, refresh period and t _{RF} C as t _{RF} C will scale with density and is vendor specific.										

3.4 ADDRESSING (cont'd)

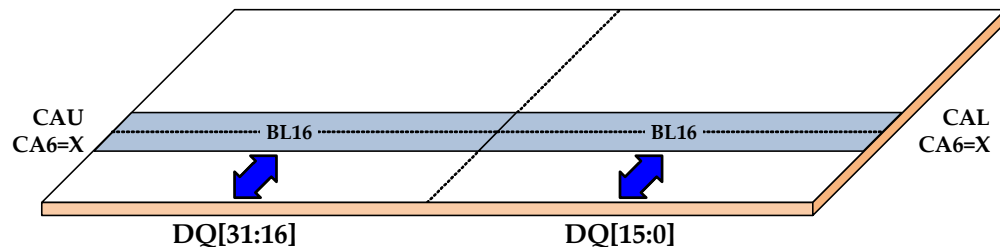
Two column addresses with a common bank address are provided with each READ and WRITE command, allowing two pseudo-independent memory accesses with 32 bytes access granularity in QDR operating mode and 16 bytes access granularity in DDR operating mode:

- The lower column address (CAL) is associated with DQ[15:0] and received on addresses A[5:0].
- The upper column address (CAU) is associated with DQ[31:16] and received on addresses A[15:12, 9, 7].

GDDR5X SGRAM's addressing is transparent between QDR and DDR operating modes: data can be written in QDR operating mode with a single BL=16 WRITE burst, and read in DDR operating mode with two BL=8 READ bursts, and vice versa. Column address A6 is evaluated in DDR operating mode only; it can be considered the LSB and selects between the data corresponding to the first half of a BL=16 burst (UI 0..7) with A6 being set Low, and the data corresponding to the second half of a BL=16 burst (UI 8..15) with A6 being set High.

Figure 3 illustrates the addressing in QDR and DDR operating modes assuming the same column addresses CAL and CAU for lower and upper data bytes. This is equivalent to accesses using a single column address, however, it is required to provide both CAL and CAU along with the READ or WRITE command.

Case 1: Single READ/WRITE burst in QDR Mode (BL16) with CAL = CAU



Case 2: Two READ/WRITE bursts in DDR Mode (BL8) with CAL = CAU

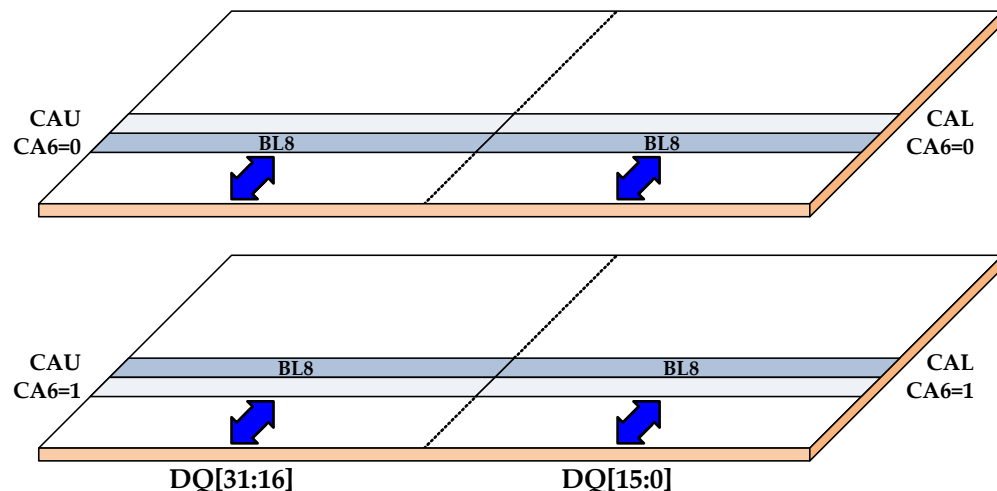
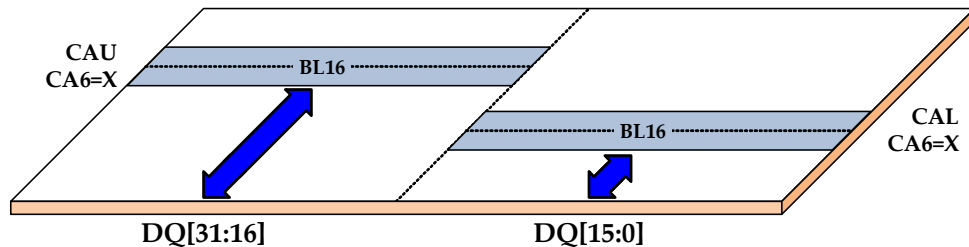


Figure 3 — Column Accesses with Identical Lower and Upper Column Addresses

3.4 ADDRESSING (cont'd)

Figure 4 illustrates the addressing in QDR and DDR operating modes assuming different column address for lower and upper bytes. This corresponds to two pseudo-independent memory accesses with 32 bytes access granularity in QDR operating mode and 16 bytes in DDR operating mode. It is pointed out that both accesses share the bank address and therefore access the same open row in that bank.

Case 3: One READ/WRITE burst in QDR Mode with CAL $\neq$ CAU



Case 4: Two READ/WRITE bursts in DDR Mode with CAL $\neq$ CAU

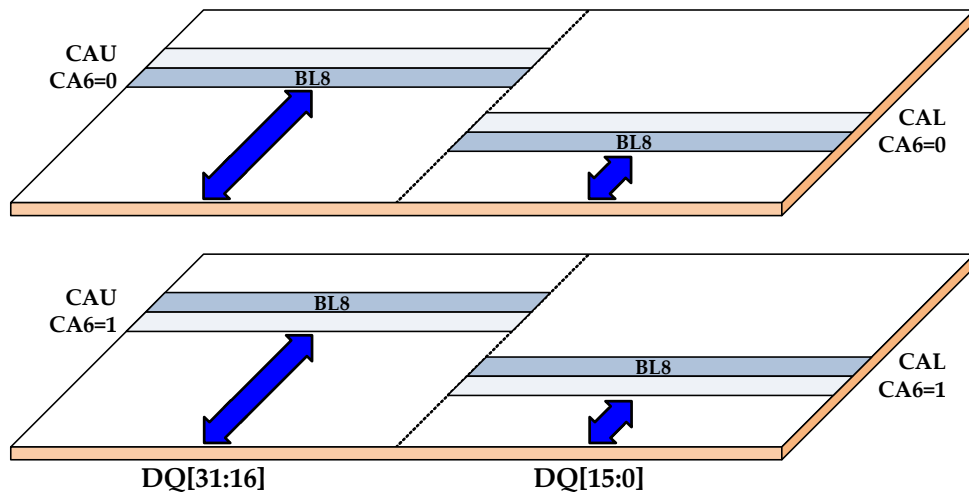
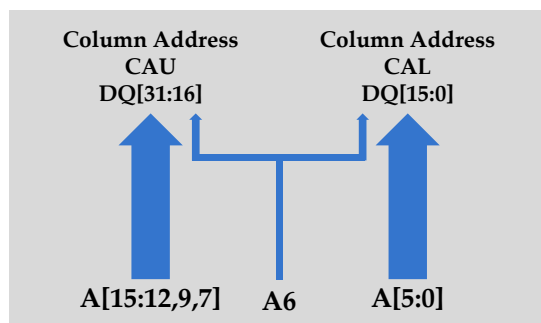


Figure 4 — Column Accesses with Different Lower and Upper Column Addresses

3.4.1 Address Compatibility Mode

GDDR5 SGRAMs receive the column address on the lower address pins only; this column address is used for all data bytes. The address compatibility mode adopts this functionality for GDDR5X SGRAMs (see Figure 3); if enabled by bit A8 in MR8, the device will use the column address received on A[5:0] as CAL and CAU. Address inputs A[15:12, 9, 7] are ignored in this mode. The memory accesses will be identical to those shown in Figure 3 for both BL=16 and BL=8 cases.

Address Compatibility Mode Off



Address Compatibility Mode On

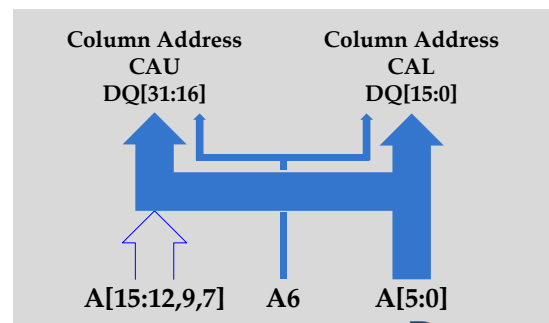


Figure 5 — Address Compatibility Mode

3.5 BANK GROUPS

For devices operating at frequencies above a certain threshold (f_{CKBG}), the activity within a bank group must be restricted to ensure proper operation of the device. The 16 banks are divided into four bank groups. The bank groups feature is controlled by bits A[11:10] in MR3.

Table 4 — Bank Groups

BANKS	ADDRESSING				BANK GROUP
	BA3	BA2	BA1	BA0	
0 to 3	0	0	X	X	Group A
4 to 7	0	1	X	X	Group B
8 to 11	1	0	X	X	Group C
12 to 15	1	1	X	X	Group D

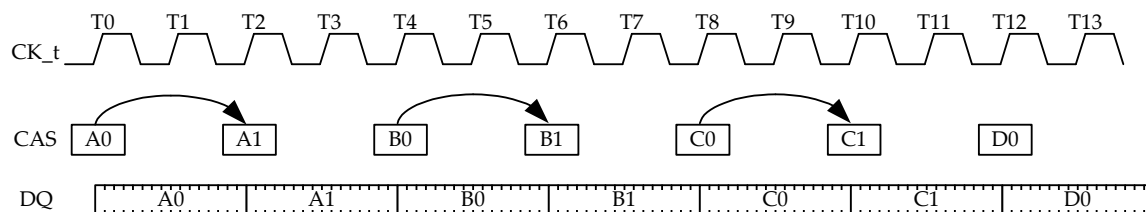
These bank groups allow the specification of different command delay parameters depending on whether back-to-back accesses are to banks within one bank group or across bank groups as shown in Table 5. Figure 6 shows back-to-back column accesses based on t_{CCDL} and t_{CCDS} parameters.

Table 5 — Command Sequences Affected by Bank Groups

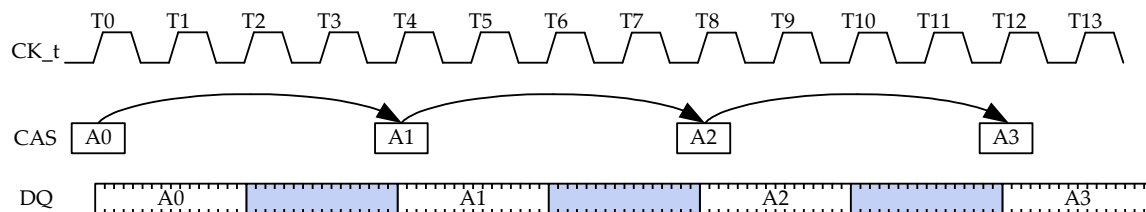
COMMAND SEQUENCE	CORRESPONDING AC TIMING PARAMETER			NOTES
	BANK GROUPS DISABLED	BANK GROUPS ENABLED		
		ACCESSES TO DIFFERENT BANK GROUPS	ACCESSES WITHIN THE SAME BANK GROUP	
ACTIVATE to ACTIVATE	t _{RRDS}	t _{RRDS}	t _{RRDL}	
WRITE to WRITE	t _{CCDS}	t _{CCDS}	t _{CCDL}	
READ to READ	t _{CCDS}	t _{CCDS}	t _{CCDL}	
Internal WRITE to READ	t _{WTRS}	t _{WTRS}	t _{WTRL}	
READ to PRECHARGE	t _{RTPS}	1 t _{ck}	t _{RTPL}	1
NOTE 1 Parameters t _{RTPS} and t _{RTPL} apply only when READ and PRECHARGE go to the same bank; use t _{RTPS} when BG are disabled, and t _{RTPL} when BG are enabled.				

3.5 BANK GROUPS (cont'd)

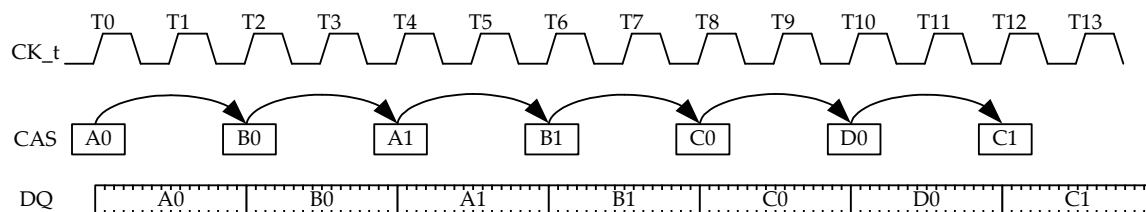
Example 1 (Bank Groups Disabled): $t_{CCDS} = 2 t_{CK}$



Example 2 (Bank Groups Enabled): $t_{CCDL} = 4 t_{CK}$



Example 3 (Bank Groups Enabled): $t_{CCDS} = 2 t_{CK}$



- NOTE 1 Column accesses are to open banks, and t_{RCD} has been met.
 NOTE 2 $RLmrs = 0$ assumed.
 NOTE 3 Ax, Bx, C, Dx: accesses to bank groups A, B, C and D, respectively.
 NOTE 4 With bank groups enabled, t_{CCDL} is $3 * t_{CK}$ or $4 * t_{CK}$ as programmed in MR3.

Figure 6 — t_{CCDS} and t_{CCDL} Timings

3.6 ADDRESS BUS INVERSION (ABI)

Address Bus Inversion (ABI) reduces the power requirements on address pins, as the number of address lines driving a low level can be limited to 5.

The ABI function is associated with the electrical signalling on the address lines between a controller and the GDDR5X SGRAM regardless of whether the information conveyed on the address lines is a row or column address, a mode register op-code, a write data mask, or any other pattern.

The ABI_n input is an active Low double data rate (DDR) signal and sampled by the GDDR5X SGRAM at the rising edge of CK_t and the rising edge of CK_c along with the address inputs.

Once enabled by the corresponding ABI mode register bit, the device inverts the pattern received on the address inputs in case ABI_n is sampled Low, or leaves the pattern non-inverted in case ABI_n is sampled High, as shown in Figure 7.

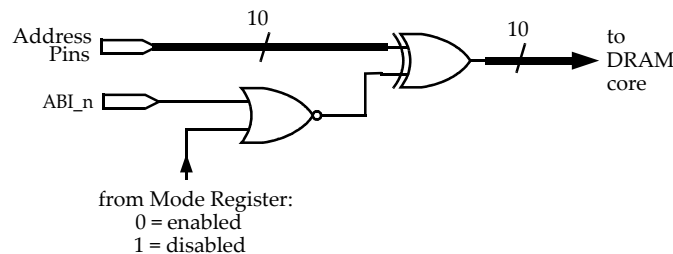


Figure 7 — Example of Address Bus Inversion Logic

The flow diagram in Figure 8 illustrates the ABI operation. The controller decides whether to invert or not invert the data conveyed on the address lines. The GDDR5X SGRAM has to perform the reverse operation based on the level of the ABI_n pin. Address input timing parameters are only valid with ABI being enabled and a maximum of 5 address inputs driven Low.

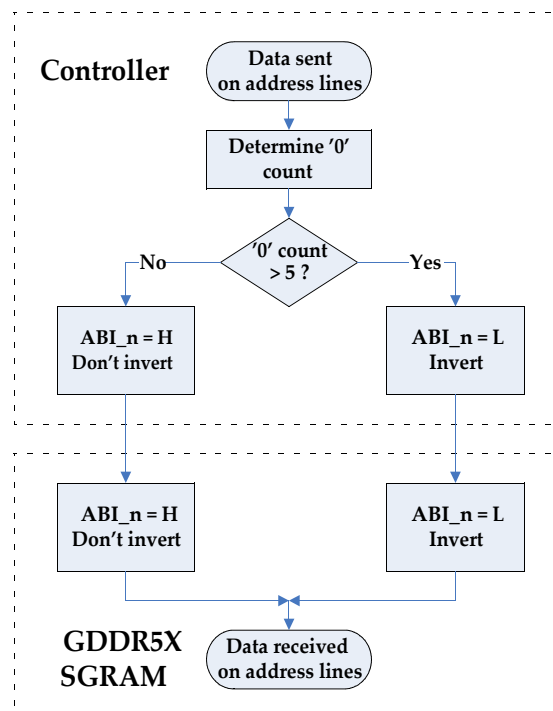


Figure 8 — Address Bus Inversion (ABI) Flow Diagram

3.7 READ and WRITE DATA BUS INVERSION (DBI)

The Data Bus Inversion (DBI_{dc}) reduces the DC power consumption and supply noise-induced jitter on data pins because the number of DQ lines driving a low level can be limited to 4 within a byte. DBI_{dc} is evaluated per byte.

There is one DBI_n pin per byte: DBI0_n is associated with DQ0-DQ7, DBI1_n with DQ8-DQ15, DBI2_n with DQ16-DQ23 and DBI3_n with DQ24-DQ31.

The DBI_n pins are bidirectional active Low double data rate (DDR) signals. For writes, they are sampled by the device along with the DQ of the same byte; for reads, they are driven by the device along with the DQ of the same byte.

Once enabled by the corresponding RDBI mode register bit, the device inverts read data and sets DBI_n Low when the number of '0' data bits within a byte is greater than 4; otherwise the device does not invert the read data and sets DBI_n High, as shown in Figure 9.

Once enabled by the corresponding WDBI Mode Register bit, the device inverts write data received on the DQ inputs in case DBI_n is sampled Low, or leaves the data non-inverted in case DBI_n is sampled High, as shown in Figure 10.

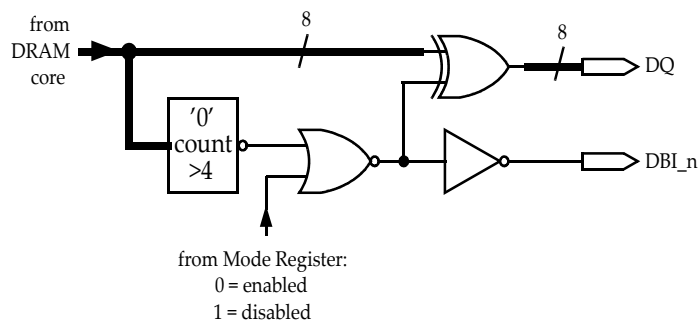


Figure 9 — Example of Data Bus Inversion Logic for READS

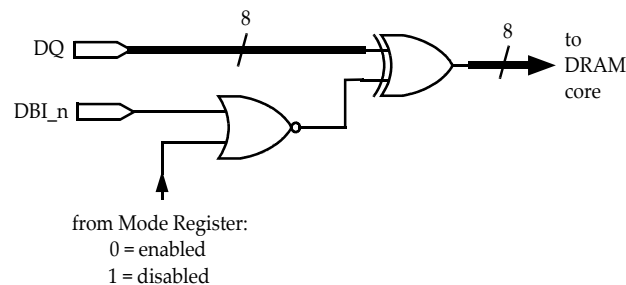


Figure 10 — Example of Data Bus Inversion Logic for WRITES

The flow diagram in Figure 11 illustrates the DBI_{dc} operation. In any case, the transmitter (the controller for writes, the GDDR5X SGRAM for reads) decides whether to invert or not invert the data conveyed on the DQs. The receiver (the GDDR5X SGRAM for writes, the controller for reads) has to perform the reverse operation based on the DBI_n pin level. Data input and output timing parameters are only valid with DBI being enabled and a maximum of 4 data lines per byte driven Low.

3.7 READ and WRITE DATA BUS INVERSION (DBI) (cont'd)

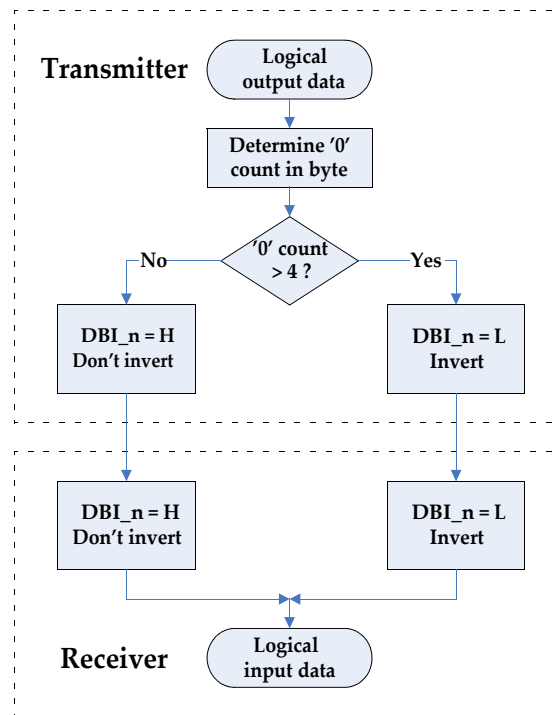


Figure 11 — DBI Flow Diagram

3.7.1 DBI_n Pin Special Function Overview

The DBI_n pin has special behavior compared to DQ pins because of the ability to enable and disable it via MRS. For either WRITE or READ DBI_n pin training, both READ DBI (RDBI) and WRITE DBI (WDBI) must be enabled. The behavior of the DBI_n pin in various mode register settings is summarized as follows:

- If both RDBI and WDBI are enabled, the pin drives DBI FIFO data with RDTR bursts, and the DBI FIFO accepts data from WRTR bursts.
- If only RDBI is enabled, the pin drives ODT except for READ or RDTR bursts.
- If only WDBI is enabled, the pin always drives ODT (unless in reset).
- If both RDBI and WDBI are disabled, the pin always drives ODT (unless in reset).

3.8 ERROR DETECTION CODE (EDC)

Error detection on the data bus is provided to improve system reliability. The device generates a checksum per byte lane for both READ and WRITE data and returns the checksum to the controller. Based on the checksum, the controller can decide if the data (or the returned CRC) was transmitted in error and retry the READ or WRITE command. The GDDR5X SGRAM itself does not perform any error correction. The algorithm detects 100% single bit errors and >99% double bit errors.

The features of the EDC are:

- 8 bit checksum on 144 bits (9 channels x 16 bit burst) in QDR mode, and 72 bits (9 channels x 8 bit burst) in DDR mode;
- dedicated EDC transfer pin per 9 channels;
- asymmetrical latencies on EDC transfer for reads and writes.

The CRC calculation is embedded into the write and read data stream as shown in Figure 46 "Data Paths used for Read and Write Training":

- for writes, the checksum is calculated on the DQ and DBI_n input data before decoding with DBI;
- for reads, the checksum is calculated on the DQ and DBI_n output data after encoding with DBI.

The CRC calculation is not affected by any data mask sent along with WDM, WDMA, WSM or WSMA commands. It is controlled separately for READ and WRITE bursts by the following bits in MR4:

- Bit A9 controls the CRC calculation for READ bursts, and bits A[8:7] hold the CRC read latency (CRCRL);
- Bit A10 controls the CRC calculation for WRITE bursts, and bits A[6:4] hold the CRC write latency (CRCWL)

The EDC latency is based on the RL and CRCRL latencies for read data, and the WL and CRCWL latencies for write data as shown in Table 6. The CRC bursts replace the EDC hold pattern for the duration of the bursts if CRC is enabled.

Table 6 — EDC Latencies

DESCRIPTION	SYMBOL	VALUE	UNITS
EDC READ Latency	EDCRL	RL + CRCRL	t _{CK}
EDC WRITE Latency	EDCWL	WL + CRCWL	t _{CK}

The GDDR5X SGRAM uses a 2-stage algorithm in the CRC calculation on a byte lane basis:

- Step 1: two-input XOR gates compress the first eight bits (D0 - D7) and the second eight bits (D8 - D15) of a 16-bit data burst into an 8-bit data word as shown in Figure 12. The inputs of the 2-input XOR have been carefully chosen to minimize the probability of undetectable double bit errors:
 - a temporal decorrelation combines UI that are latched by different internal WCK clock phases;
 - a spatial decorrelation combines UI from different bit lanes.In DDR mode this step 1 is effectively bypassed by forcing the second eight bits of the 16-bit data burst to 0.
- Step 2: the ATM-8 HEC, $X^8+X^2+X^1+1$, CRC polynomial calculates an 8-bit checksum as shown in Figure 13. The starting seed value is set to 0 in hardware. The bit order is optimized for errors in the time burst direction. All 1s are assumed in the calculation for the DBI_n pin when DBI is disabled for writes or reads in the mode register.

A typical combinatorial logic block implementation of the CRC algorithm consists of 72 parallel two-input XOR gates for step 1 followed by 272 two-input XOR gates in eight 6 XOR gate deep trees for step 2, resulting in a total XOR gate logic depth of 7.

3.8 ERROR DETECTION CODE (EDC) (cont'd)

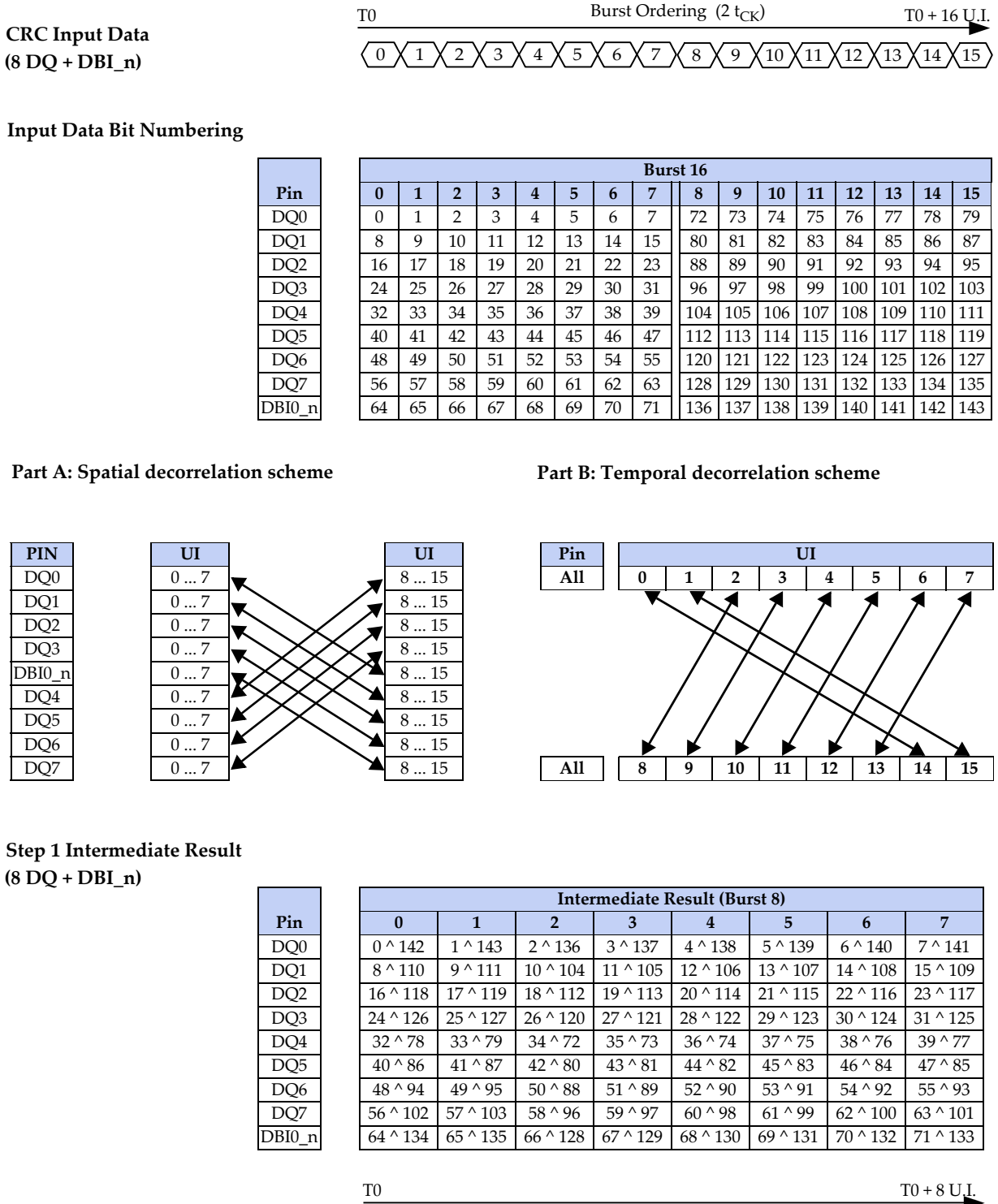
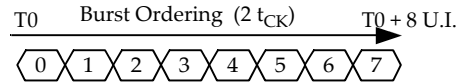


Figure 12 — EDC Calculation Matrix (Step 1)

3.8 ERROR DETECTION CODE (EDC) (cont'd)

Step 1 Intermediate Result
(8 DQ + DBI_n)

CRC Polynomial
 $X^8 + X^2 + X + 1$



Pin	0	1	2	3	4	5	6	7
DQ0	0	1	2	3	4	5	6	7
DQ1	8	9	10	11	12	13	14	15
DQ2	16	17	18	19	20	21	22	23
DQ3	24	25	26	27	28	29	30	31
DQ4	32	33	34	35	36	37	38	39
DQ5	40	41	42	43	44	45	46	47
DQ6	48	49	50	51	52	53	54	55
DQ7	56	57	58	59	60	61	62	63
DBI0_n	64	65	66	67	68	69	70	71

CRC Data Output Bit Ordering

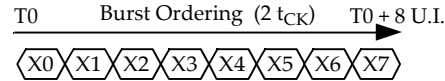


Figure 13 — EDC Calculation Matrix (Step 2)

CRC Equations (Step 2)

$$\begin{aligned}
 \text{CRC}[0] &= D[69] \wedge D[68] \wedge D[67] \wedge D[66] \wedge D[64] \wedge D[63] \wedge D[60] \wedge D[56] \wedge D[54] \wedge \\
 &\quad D[53] \wedge D[52] \wedge D[50] \wedge D[49] \wedge D[48] \wedge D[45] \wedge D[43] \wedge D[40] \wedge D[39] \wedge \\
 &\quad D[35] \wedge D[34] \wedge D[31] \wedge D[30] \wedge D[28] \wedge D[23] \wedge D[21] \wedge D[19] \wedge D[18] \wedge \\
 &\quad D[16] \wedge D[14] \wedge D[12] \wedge D[8] \wedge D[7] \wedge D[6] \wedge D[0]; \\
 \text{CRC}[1] &= D[70] \wedge D[66] \wedge D[65] \wedge D[63] \wedge D[61] \wedge D[60] \wedge D[57] \wedge D[56] \wedge D[55] \wedge \\
 &\quad D[52] \wedge D[51] \wedge D[48] \wedge D[46] \wedge D[45] \wedge D[44] \wedge D[43] \wedge D[41] \wedge D[39] \wedge \\
 &\quad D[36] \wedge D[34] \wedge D[32] \wedge D[30] \wedge D[29] \wedge D[28] \wedge D[24] \wedge D[23] \wedge D[22] \wedge \\
 &\quad D[21] \wedge D[20] \wedge D[18] \wedge D[17] \wedge D[16] \wedge D[15] \wedge D[14] \wedge D[13] \wedge D[12] \wedge \\
 &\quad D[9] \wedge D[6] \wedge D[1] \wedge D[0]; \\
 \text{CRC}[2] &= D[71] \wedge D[69] \wedge D[68] \wedge D[63] \wedge D[62] \wedge D[61] \wedge D[60] \wedge D[58] \wedge D[57] \wedge \\
 &\quad D[54] \wedge D[50] \wedge D[48] \wedge D[47] \wedge D[46] \wedge D[44] \wedge D[43] \wedge D[42] \wedge D[39] \wedge \\
 &\quad D[37] \wedge D[34] \wedge D[33] \wedge D[29] \wedge D[28] \wedge D[25] \wedge D[24] \wedge D[22] \wedge D[17] \wedge \\
 &\quad D[15] \wedge D[13] \wedge D[12] \wedge D[10] \wedge D[8] \wedge D[6] \wedge D[2] \wedge D[1] \wedge D[0]; \\
 \text{CRC}[3] &= D[70] \wedge D[69] \wedge D[64] \wedge D[63] \wedge D[62] \wedge D[61] \wedge D[59] \wedge D[58] \wedge D[55] \wedge \\
 &\quad D[51] \wedge D[49] \wedge D[48] \wedge D[47] \wedge D[45] \wedge D[44] \wedge D[43] \wedge D[40] \wedge D[38] \wedge \\
 &\quad D[35] \wedge D[34] \wedge D[30] \wedge D[29] \wedge D[26] \wedge D[25] \wedge D[23] \wedge D[18] \wedge D[16] \wedge \\
 &\quad D[14] \wedge D[13] \wedge D[11] \wedge D[9] \wedge D[7] \wedge D[3] \wedge D[2] \wedge D[1]; \\
 \text{CRC}[4] &= D[71] \wedge D[70] \wedge D[65] \wedge D[64] \wedge D[63] \wedge D[62] \wedge D[60] \wedge D[59] \wedge D[56] \wedge \\
 &\quad D[52] \wedge D[50] \wedge D[49] \wedge D[48] \wedge D[46] \wedge D[45] \wedge D[44] \wedge D[41] \wedge D[39] \wedge \\
 &\quad D[36] \wedge D[35] \wedge D[31] \wedge D[30] \wedge D[27] \wedge D[26] \wedge D[24] \wedge D[19] \wedge D[17] \wedge \\
 &\quad D[15] \wedge D[14] \wedge D[12] \wedge D[10] \wedge D[8] \wedge D[4] \wedge D[3] \wedge D[2]; \\
 \text{CRC}[5] &= D[71] \wedge D[66] \wedge D[65] \wedge D[64] \wedge D[63] \wedge D[61] \wedge D[60] \wedge D[57] \wedge D[53] \wedge \\
 &\quad D[51] \wedge D[50] \wedge D[49] \wedge D[47] \wedge D[46] \wedge D[45] \wedge D[42] \wedge D[40] \wedge D[37] \wedge \\
 &\quad D[36] \wedge D[32] \wedge D[31] \wedge D[28] \wedge D[27] \wedge D[25] \wedge D[20] \wedge D[18] \wedge D[16] \wedge \\
 &\quad D[15] \wedge D[13] \wedge D[11] \wedge D[9] \wedge D[5] \wedge D[4] \wedge D[3]; \\
 \text{CRC}[6] &= D[67] \wedge D[66] \wedge D[65] \wedge D[64] \wedge D[62] \wedge D[61] \wedge D[58] \wedge D[54] \wedge D[52] \wedge \\
 &\quad D[51] \wedge D[50] \wedge D[48] \wedge D[47] \wedge D[46] \wedge D[43] \wedge D[41] \wedge D[38] \wedge D[37] \wedge \\
 &\quad D[33] \wedge D[32] \wedge D[29] \wedge D[28] \wedge D[26] \wedge D[21] \wedge D[19] \wedge D[17] \wedge D[16] \wedge \\
 &\quad D[14] \wedge D[12] \wedge D[10] \wedge D[6] \wedge D[5] \wedge D[4]; \\
 \text{CRC}[7] &= D[68] \wedge D[67] \wedge D[66] \wedge D[65] \wedge D[63] \wedge D[62] \wedge D[59] \wedge D[55] \wedge D[53] \wedge \\
 &\quad D[52] \wedge D[51] \wedge D[49] \wedge D[48] \wedge D[47] \wedge D[44] \wedge D[42] \wedge D[39] \wedge D[38] \wedge \\
 &\quad D[34] \wedge D[33] \wedge D[30] \wedge D[29] \wedge D[27] \wedge D[22] \wedge D[20] \wedge D[18] \wedge D[17] \wedge \\
 &\quad D[15] \wedge D[13] \wedge D[11] \wedge D[7] \wedge D[6] \wedge D[5];
 \end{aligned}$$

3.8 ERROR DETECTION CODE (EDC) (cont'd)

3.8.1 EDC Pin Special Function Overview

The EDC pin is used for many different functions. The behavior of the EDC pin in various modes is summarized in Table 7.

Table 7 — EDC Pin Behavior

DEVICE STATUS	CONDITION	EDC[3:0] PIN STATUS
Device power-up	RESET_n = Low	High-Z
	RESET_n = High; no WCK clocks	High
	RESET_n = High; stable WCK clocks	EDC hold pattern (default = 1111)
Address training	ADT on (MR15 A10 = 1)	A14/A15 address inputs
WCK2CK training	WCK is sampled High	High
	WCK is sampled Low	Low
Idle	EDC13 INV off (MR4 A11 = 0)	EDC hold pattern
	EDC13 INV on (MR4 A11 = 1)	EDC0, EDC2: EDC hold pattern EDC1, EDC3: inverted EDC hold pattern
WRITE burst	WRCRC on (MR4 A10 = 0)	CRC data
	WRCRC off (MR4 A10 = 1)	EDC hold pattern
READ or RDTR burst	RDCRC on (MR4 A9 = 0)	CRC data
	RDCRC off (MR4 A9 = 1)	EDC hold pattern
LDFE	WRCRC + RDCRC both on or both off	EDC hold pattern
WRTR burst	-	EDC hold pattern
Power-down	WCK enabled (MR5 A1 = 0)	EDC hold pattern
	WCK disabled (MR5 A1 = 1)	High
Self refresh	-	High
READ burst in RDQS mode	RDQS mode on (MR3 A5 = 1)	Fixed 1010 strobe pattern (DDR mode only)
Vendor ID mode	WCK is stable	EDC hold pattern
All except reset	EDC High-Z on (MR8 A2 = 1)	High-Z
	VREFD Monitor on (MR8 A7 = 1)	internal V _{REFD} voltage level

3.9 VREFC and VREFD

The GDDR5X SGRAM offers multiple options for the reference voltages for address/command (V_{REFC}) and data inputs (V_{REFD}).

3.9.1 Reference Voltage for Address/Command Inputs (V_{REFC})

The reference voltage for the address/command inputs (V_{REFC}) can be supplied via the external VREFC pin or be generated internally as illustrated in Figure 14. The selection is made with the rising edge of RESET_n: the device selects internal V_{REFC} with a default level of $0.7 \times V_{\text{DDQ}}$ when the VREFC pin is pulled Low in the system; otherwise external V_{REFC} is selected.

Half VREFC mode enables the V_{REFC} level to be adjusted when the ADD/CMD inputs operate without termination. When bit A6 in MR7 is set to 1, a level of nominally $0.5 \times V_{\text{DDQ}}$ is generated. The maximum operating frequency for this mode is defined by f_{CKVREFC2} . A Half V_{REFC} mode reference voltage change requires t_{VREFC2} to settle.

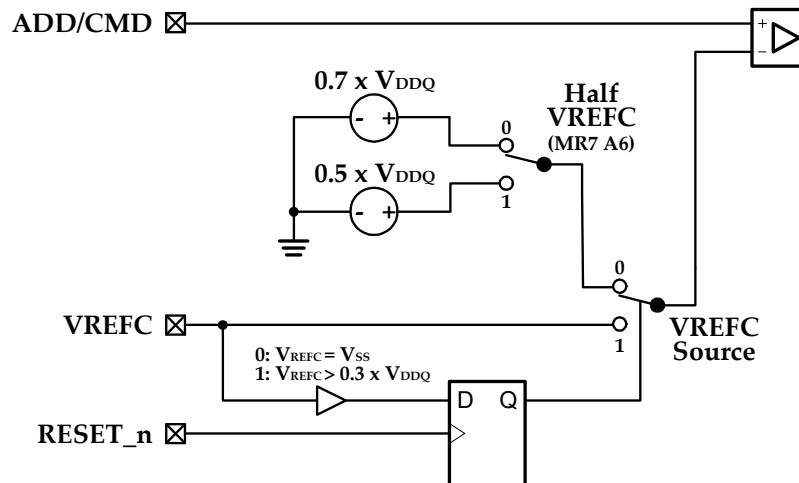


Figure 14 — VREFC Options

3.9.2 Reference Voltage for Data Inputs (V_{REFD})

The reference voltage for the DQ and DBI_n inputs (V_{REFD}) is generated internally, and separate V_{REF} circuits are associated with each data byte.

The V_{REFD} level is linear with a nominal step size of $1/210 \times V_{\text{DDQ}}$ in a range from $0.55 \times V_{\text{DDQ}}$ to $0.85 \times V_{\text{DDQ}}$ as illustrated in Figure 16 and Table 8, and must be set by programming bits A[11:0] in MR6 and bits A[11:0] in MR9 as shown in Table 10. The V_{REFD} settling time t_{VREFD} is a constant value for the device, and is referenced from the MRS command to when the 90% level of the delta between old and new V_{REFD} voltage has been reached as illustrated in Figure 17.

Half VREFD mode enables the V_{REFD} level to be adjusted when the DQ and DBI_n inputs operate without termination. When bit A7 in MR7 is set to 1, a level of nominally $0.5 \times V_{\text{DDQ}}$ is generated. The maximum operating frequency for this mode is defined by f_{CKVREFD2} . A Half VREFD mode reference voltage change requires t_{VREFD2} to settle.

VREF C2D mode enables a backup solution for external VREFD. When bit A6 in MR8 is set to 1, an internal bridge is enabled that connects both V_{REFD} circuits with the V_{REFC} circuit and further with the external VREFC pin. VREF C2D mode requires that external V_{REFC} is selected at power-up.

3.9.2 Reference Voltage for Data Inputs (V_{REFD}) (cont'd)

VREFD Monitor mode allows the observation the internal V_{REFD} voltages at the EDC pins of both double bytes. The mode is controlled by bit A7 in MR8. The settling time is longer than t_{MRD} and depends on the external capacitive load at the EDC pins.

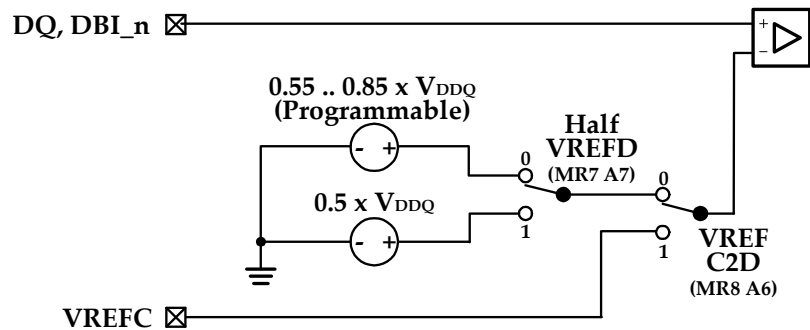


Figure 15 – VREFD Options

Table 8 – VREFD Level

VREFD Level Code		VREFD Level		
MR6 A[11:6] / MR9 A[11:6] MR6 A[5:0] / MR9 A[5:0]	Decimal	% V _{DDQ}	Divider	V _{REFD} [V]
1 1 1 1 1 1	63	0.852	179 / 210	1.151
1 1 1 1 1 0	62	0.848	178 / 210	1.144
1 1 1 1 0 1	61	0.843	177 / 210	1.138
...				
1 0 0 0 0 1	33	0.710	149 / 210	0.958
1 0 0 0 0 0	32	0.705	148 / 210	0.951
0 1 1 1 1 1	31	0.700	147 / 210	0.945
0 1 1 1 1 0	30	0.695	146 / 210	0.939
0 1 1 1 0 1	29	0.690	145 / 210	0.932
...				
0 0 0 0 1 0	2	0.562	118 / 210	0.759
0 0 0 0 0 1	1	0.557	117 / 210	0.752
0 0 0 0 0 0	0	0.552	116 / 210	0.746

3.9.2 Reference Voltage for Data Inputs (V_{REFD}) (cont'd)

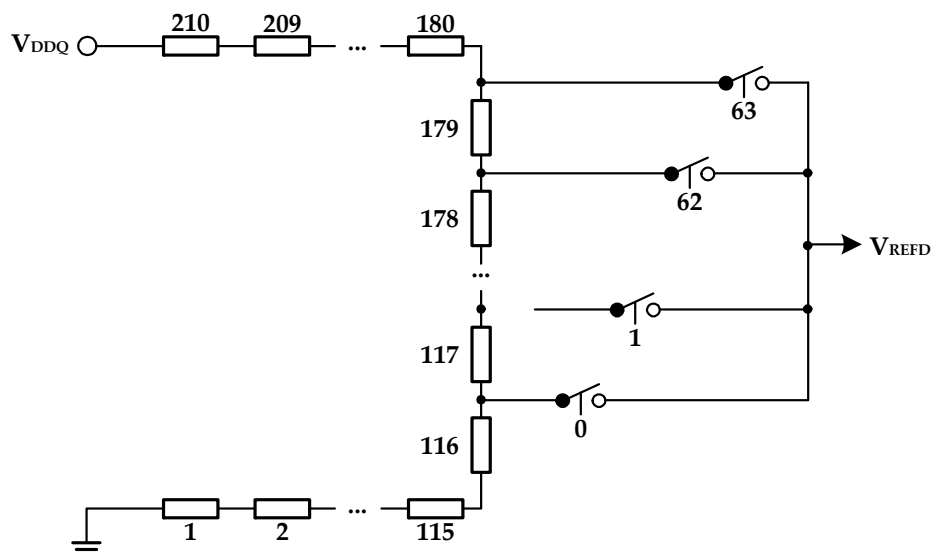


Figure 16 — V_{REFD} Circuit

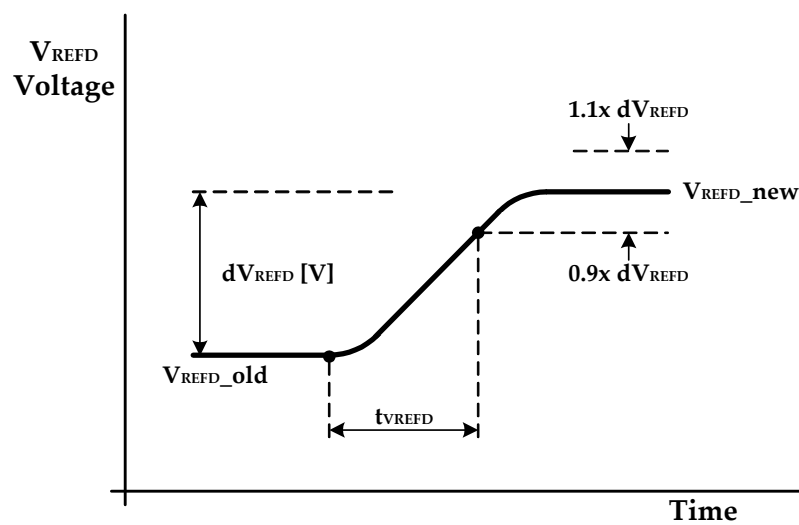


Figure 17 — V_{REFD} Settling Time

3.10 TEMPERATURE SENSOR

GDDR5X SGRAMs incorporate a temperature sensor with digital temperature readout function. This function allows the controller to monitor the device's junction temperature and use this information to make sure the device is operated within the specified temperature range or to adjust interface timings relative to temperature changes over time.

The temperature sensor is permanently enabled.

The temperature readout uses the DRAM Info mode feature. The digital value is driven asynchronously on DQ[7:0] following the MRS command to MR3 that sets bit A7 to 1 and bit A6 to 0. The temperature readout is continuously driven until an MRS command sets both bits to 0.

The device's junction temperature is linearly encoded as shown in Table 9 and Figure 18. The sensor's accuracy is vendor specific.

Table 9 — Temperature Sensor Readout Pattern

TEMPERATURE [°C]	DECIMAL TEMPERATURE READOUT	BINARY TEMPERATURE READOUT DQ[7:0]
-40	0	0000 0000
...	...	...
0	20	0001 0100
2	21	0001 0101
4	22	0001 0110
6	23	0001 0111
8	24	0001 1000
...	...	...
120	80	0101 0000
>120	80	0101 0000

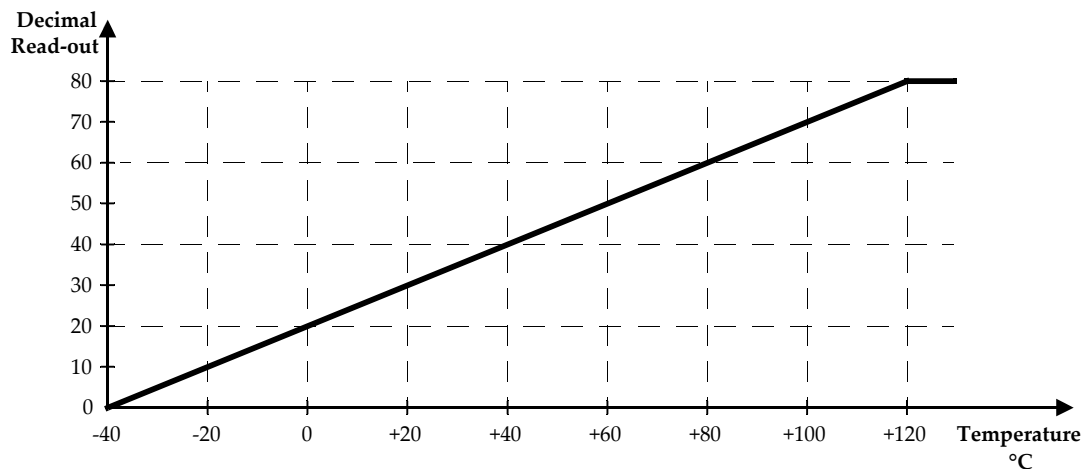


Figure 18 — Temperature Sensor Readout Characteristic

3.11 DUTY CYCLE CORRECTOR (DCC)

The use of the optional Duty Cycle Corrector (DCC) can correct for the static duty cycle error of the WCK clock, resulting in improved timing margins for Reads and Writes. It is recommended to enable the DCC prior to the phase search in WCK2CK training because any shift of rising and falling WCK edges can impact the WCK2CK training results.

DCC operation is controlled by MR7 bits A[11:10]. The duty cycle correction is started by setting bit A10. The DCC must be held in this state for a minimum duration of t_{DCC} . After t_{DCC} is met, bit A11 shall be set to terminate the duty cycle correction and hold the correction code. The DCC may be disabled at any time by resetting bits A11 and A10.

When in the hold state, the DCC remembers its correction code during power-down (with LP2 enabled) and self refresh. In this case the WCK2CK training time upon power-down exit or self refresh exit is not gated by t_{DCC} , as the correction code will be automatically restored. Alternatively, a new duty cycle correction cycle could be started by resetting bit A11.

A new duty cycle correction cycle is required upon a frequency change.

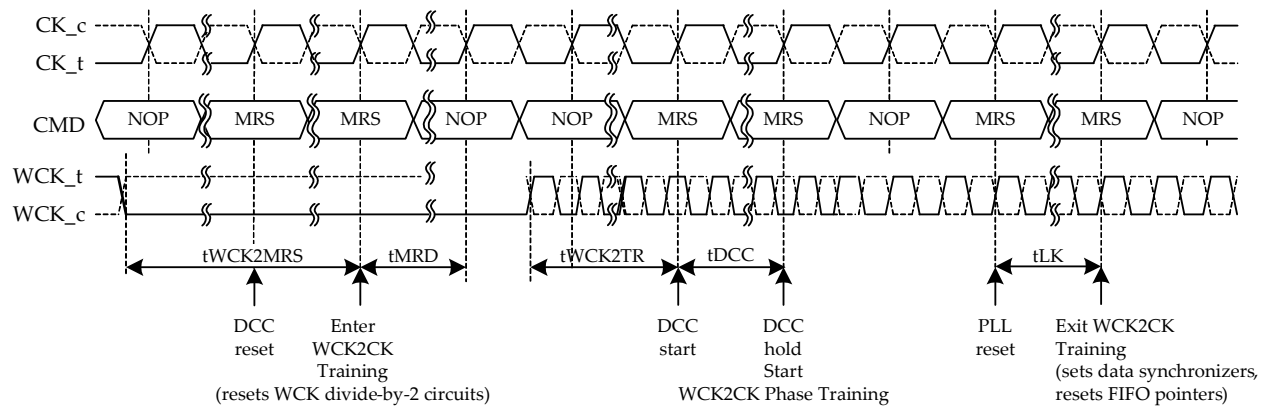


Figure 19 — WCK2CK Training Sequence with DCC

4 MODE REGISTERS

Sixteen mode registers define the specific mode of operation for the GDDR5X SGRAM. MR0 to MR9, MR11, and MR15 are defined as shown in Figure 20. MR10 is reserved for future use, and MR12 to MR14 are reserved for vendor specific features. Reprogramming the mode registers does not alter the contents of the memory array.

All mode registers are programmed via the MODE REGISTER SET (MRS) command and retain the stored information until they are reprogrammed, chip reset, or until the device loses power. Mode registers must be loaded when all banks are idle and no bursts are in progress; the controller must wait the specified time t_{MRD} before initiating any subsequent operations. Violating either of these requirements results in unspecified operation.

No default states are defined for mode registers except when otherwise noted. Users therefore must fully initialize all mode registers to the desired values upon power-up or after a subsequent chip reset.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0. Bits A[15:12] are not used to program the mode registers and not shown in subsequent register definitions.

If the user activates bits in an optional field, either the optional field is activated (if option is implemented in the device) or no action is taken by the device (if option is not implemented).

4 MODE REGISTERS (cont'd)

	BA3	BA2	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
MR0	0	0	0	0	Write Recovery for Auto Precharge (WR)				TM	Read Latency (RLmrs)				Write Latency (WLmrs)		
MR1	0	0	0	1	PLL Reset	ABI	WDBI	RDBI	PLL DLL	Cal Upd	ADD/CMD Termination	Data Termination		Driver Strength		
MR2	0	0	1	0	ADD/CMD/CK Termination Offset			Data and WCK Termination Offset		OCD Pull-up Driver Offset			OCD Pull-down Driver Offset			
MR3	0	0	1	1	Bank Groups		WCK Termination		Info		RDQS Mode	WCK 2CK	WCK 23Inv	WCK 01Inv	Self Refresh	
MR4	0	1	0	0	EDC13 INV	WR CRC	RD CRC	CRC Read Latency (CRCRL)		CRC Write Latency (CRCWL)			EDC Hold Pattern			
MR5	0	1	0	1	RAS						RFU	PLL/DLL Bandwidth (PLLBW)		LP3	LP2	LP1
MR6	0	1	1	0	VREFD Level Byte 0 (MF=0) / Byte 3 (MF=1)						VREFD Level Byte 2 (MF=0) / Byte 1 (MF=1)					
MR7	0	1	1	1	DCC		VDD Range		Half VREFD	Half VREFC	DQ PreA	Auto Sync	LF Mode	PLL DelC	PLL FLock	WCK PIN
MR8	1	0	0	0	CK Termination		Oper. Mode	Add Comp	VREFD Mon	VREF C2D	PLL/DLL Range		Hiber-nate	EDC Hi-Z	WR MSB	RL MSB
MR9	1	0	0	1	VREFD Level Byte 1 (MF=0) / Byte 2 (MF=1)						VREFD Level Byte 3 (MF=0) / Byte 0 (MF=1)					
MR10	1	0	1	0	Reserved											
MR11	1	0	1	1	PASR Row Segment Mask				PASR 2-Bank Mask							
MR12	1	1	0	0	Reserved for Vendor Specific Features											
MR13	1	1	0	1	Reserved for Vendor Specific Features											
MR14	1	1	1	0	Reserved for Vendor Specific Features											
MR15	1	1	1	1	RFU	ADT	MRE MF1	MRE MF0								

Figure 20 — Mode Registers Overview

4.1 MODE REGISTER 0 (MR0)

MR0 controls operating modes such as write latency, read latency, write recovery and test mode as shown in Figure 21. The register is programmed via the MRS command with BA[3:0] = 0000.

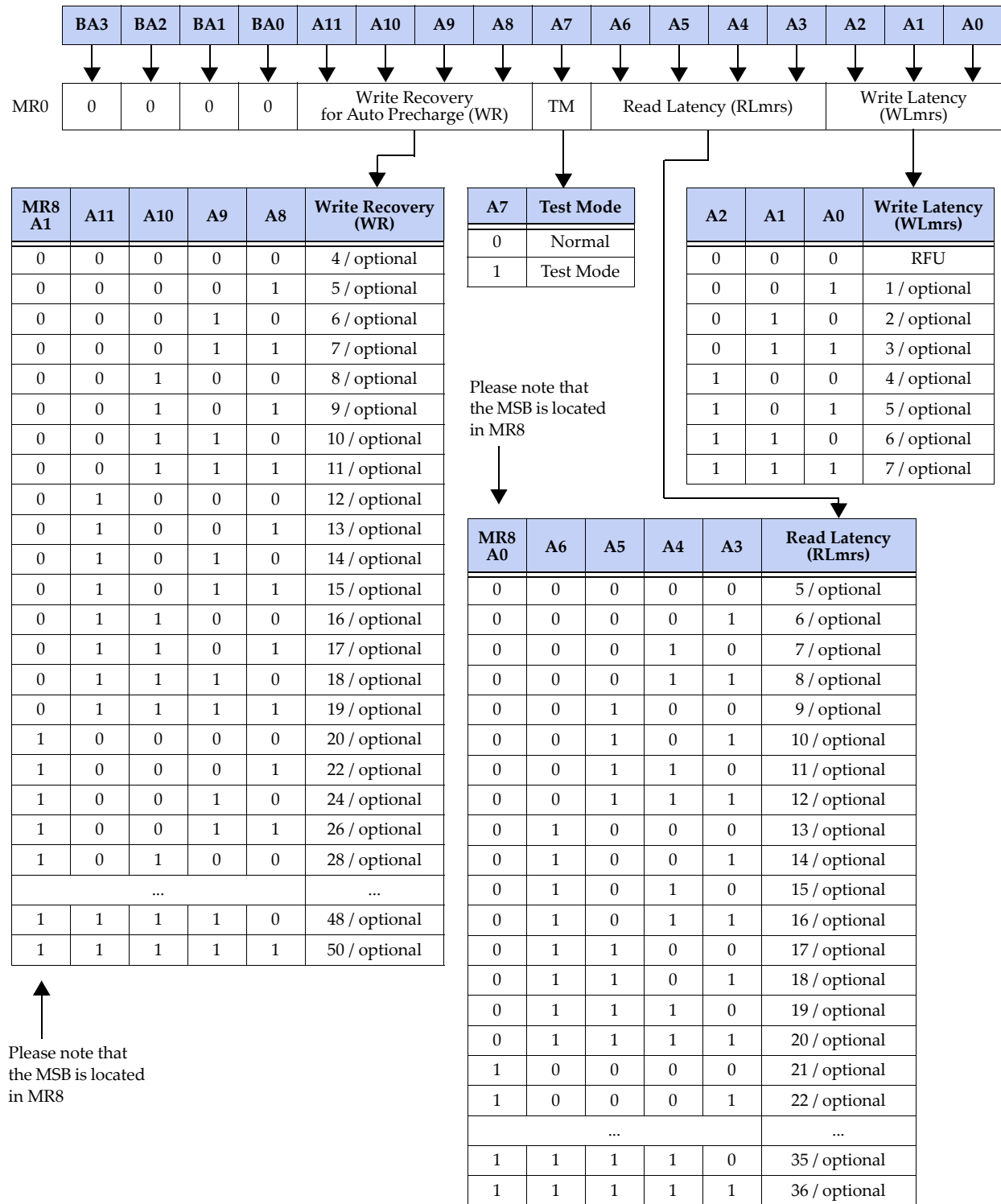


Figure 21 — Mode Register 0 (MR0) Definition

4.1 MODE REGISTER 0 (MR0) (cont'd)

Write Latency (WLMrs)

The write latency (WLMrs) is the delay in clock cycles used in the calculation of the total write latency (WL) between the registration of a WRITE or WRTR command and the availability of the first piece of input data.

WLMrs is specified by bits A[2:0], defining a WLMrs range of 1 to 7 t_{CK} . All WLMrs values are marked as “optional”, allowing the DRAM vendor to define the minimum and maximum supported WLMrs values; the supported WLMrs range must be contiguous. The full write latency definition can be found in the clause entitled OPERATION.

When the write latency is set to small values (i.e., 1,2,... clocks), the input receivers turn off in bank idle and power-down states only, in turn, raising the average operating power. When the write latency is set to higher values (i.e., .. 6, 7 clocks) the input receivers turn on when the WRITE or WRTR command is registered. Refer to vendor datasheets for value(s) of WLMrs where the input receivers only turn on when the WRITE or WRTR command is registered.

Read Latency (RLMrs)

The read latency (RLMrs) is the delay in clock cycles used in the calculation of the total read latency (RL) between the registration of a READ or RDTR command and the availability of the first piece of output data.

RLMrs is specified by bits MR8 A0 and A[6:3], defining a RLMrs range of 5 to 36 t_{CK} . Please note that the MSB is located in MR8; a read latency change therefore may require two MRS commands. All RLMrs values are marked as “optional”, allowing the DRAM vendor to define the minimum and maximum supported RLMrs values; the supported RLMrs range must be contiguous. The full read latency definition can be found in the clause entitled OPERATION.

Write Recovery for Auto Precharge (WR)

The programmed WR value is used for the auto precharge feature along with t_{RP} to determine t_{DAL} .

WR must be programmed with a value greater than or equal to $RU\{t_{WR}/t_{CK}\}$, where RU stands for round up, t_{WR} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time.

WR is specified by bits MR8 A1 and A[11:8], with 1 t_{CK} increments for lower WR values and 2 t_{CK} increments for higher WR values, defining a total WR range of 4 to 50 t_{CK} . Please note that the MSB is located in MR8; a WR change therefore may require two MRS commands.

All WR values are marked as “optional”, allowing the DRAM vendor to define the minimum and maximum supported WR values; the supported WR range must be contiguous.

Test Mode

The normal operating mode is selected by issuing an MRS command with bit A7 set to 0, and bits A[11:8] and A[6:0] set to the desired values. Programming bit A7 to 1 places the device into a test mode that is only to be used by the DRAM manufacturer. No functional operation is specified with test mode enabled.

4.2 MODE REGISTER 1 (MR1)

MR1 controls functions like driver strength, data termination, address/command termination, Read DBI, Write DBI, ABI, control of calibration updates and PLL/DLL as shown in Figure 22. The register is programmed via the MRS command with BA[3:0] = 0001. Bits A10, A[6:4] and A[1:0] of this register are initialized with 0.

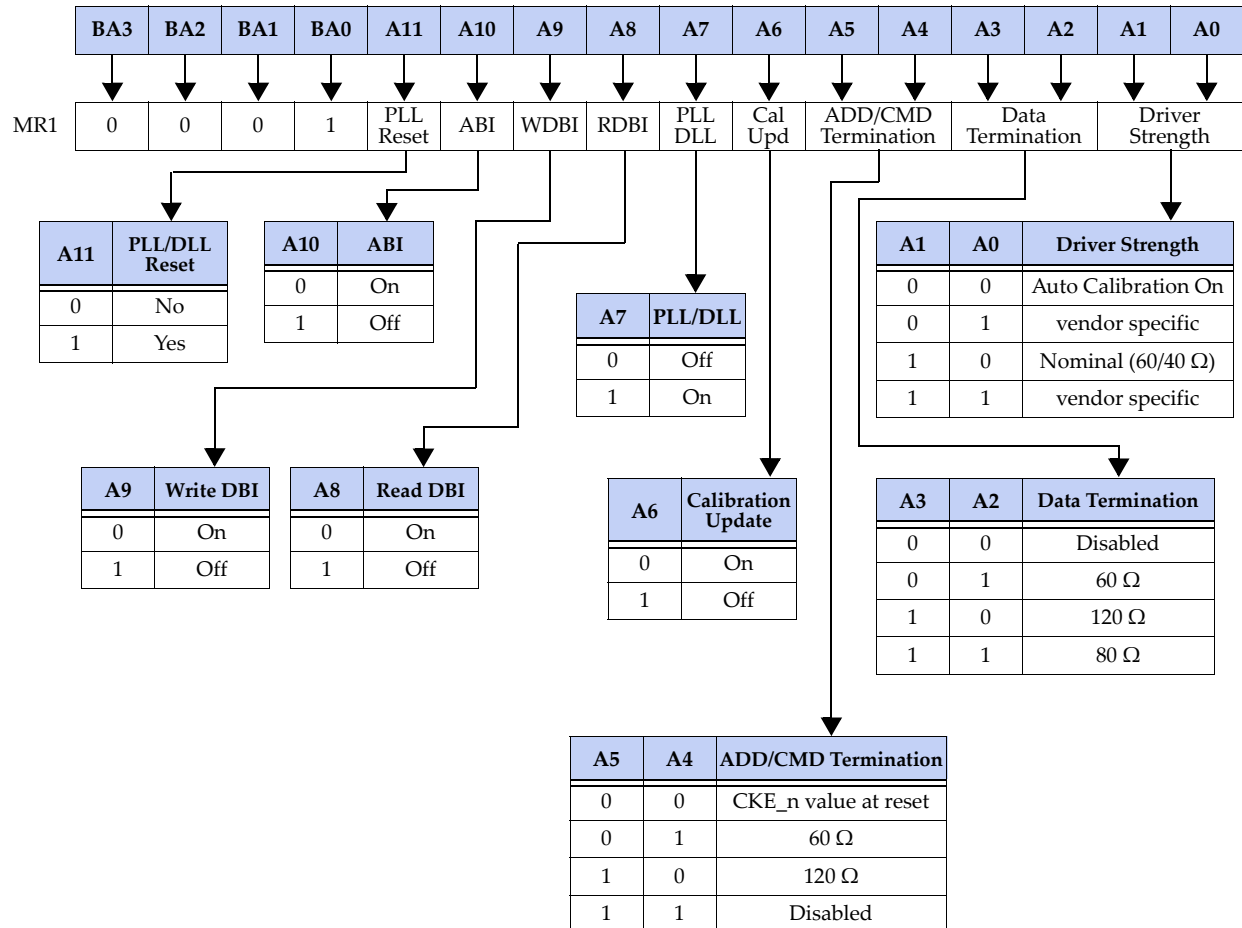


Figure 22 — Mode Register 1 (MR1) Definition

Impedance Autocalibration of Output Buffer and Active Terminator

GDDR5X SGRAMs offer auto calibrating output buffers and on-die terminations (ODT) which enable driver impedance and terminations to be matched to the system within a given range. To adjust the impedance, an external precision resistor is connected between the ZQ pin and V_{SSQ} . A nominal resistor value of 120 Ω is equivalent to the 40 Ω pull-down and 60 Ω pull-up nominal impedances of the device. RESET_n is not internally terminated.

The output driver and on-die termination impedances are updated during all REFRESH (REFAB) commands to compensate for variations in supply voltage and temperature. The impedance updates are transparent to the system.

4.2. MODE REGISTER 1 (MR1) (cont'd)

Driver Strength

Bits A[1:0] define the driver strength. The auto calibration setting enables the auto calibration functionality for the pull-down, pull-up and termination over process, temperature and voltage changes.

The design target for the factory setting is 40 Ω pull-down, 60 Ω pull-up driver strength with nominal process, voltage and temperature conditions. The nominal option enables the factory setting for the pull-down, pull-up driver strength and termination. With this option enabled, driver strength and termination are expected to change with process, voltage and temperature. AC timings are only guaranteed with auto calibration enabled.

Data Termination

Bits A[3:2] define the data termination value for the DQ and DBI_n pins in combination with the driver strength setting. Data termination is disabled by default; it can be set to a value of 60 Ω , 80 Ω or 120 Ω depending on system conditions. Data termination may also be turned off.

ADD/CMD Termination

Bits A[5:4] define the address/command termination. The default setting (00) provides that the address/command termination is determined by latching CKE_n on the rising edge of RESET_n. The address/command termination can also be set to a value of 60 Ω which is intended for a single loaded system, or 120 Ω which is intended for clamshell configurations with two devices sharing a common address/command bus. The address/command termination may also be turned off.

Calibration Update

The calibration update setting enables the calibration value to be updated automatically by the auto calibration engine. The function is enabled by default to reduce update induced jitter. The user may decide to suppress updates from the auto calibration engine by disabling calibration update.

The calibration updates can occur with any REFRESH (REFAB) command. The update is not complete for a time t_{KO} after the REFRESH command is latched. During this t_{KO} time, only NOP commands may be issued.

PLL/DLL and PLL/DLL Reset

The use of a PLL or DLL is mandatory in QDR mode and optional in DDR mode. If PLL/DLL-on operation is desired, the PLL/DLL must be enabled by setting bit A7 to 1.

A PLL/DLL reset is done by turning the PLL/DLL off and then on, or by use of the PLL/DLL reset bit A11. The PLL/DLL reset bit is self clearing, meaning that it returns to 0 after the PLL/DLL reset function has been initiated.

RDBI and WDBI

Bit A8 controls the read data bus inversion (RDBI), and bit A9 controls the write data bus inversion (WDBI). See the Data Bus Inversion (DBI) clause for more details.

ABI

Bit A10 controls the address bus inversion (ABI). ABI is enabled by default. See the Address Bus Inversion (ABI) clause for more details.

4.3 MODE REGISTER 2 (MR2)

MR2 defines the output driver (OCD) and termination (ODT) offsets as shown in Figure 23. The register is programmed via the MRS command with BA[3:0] = 0010.

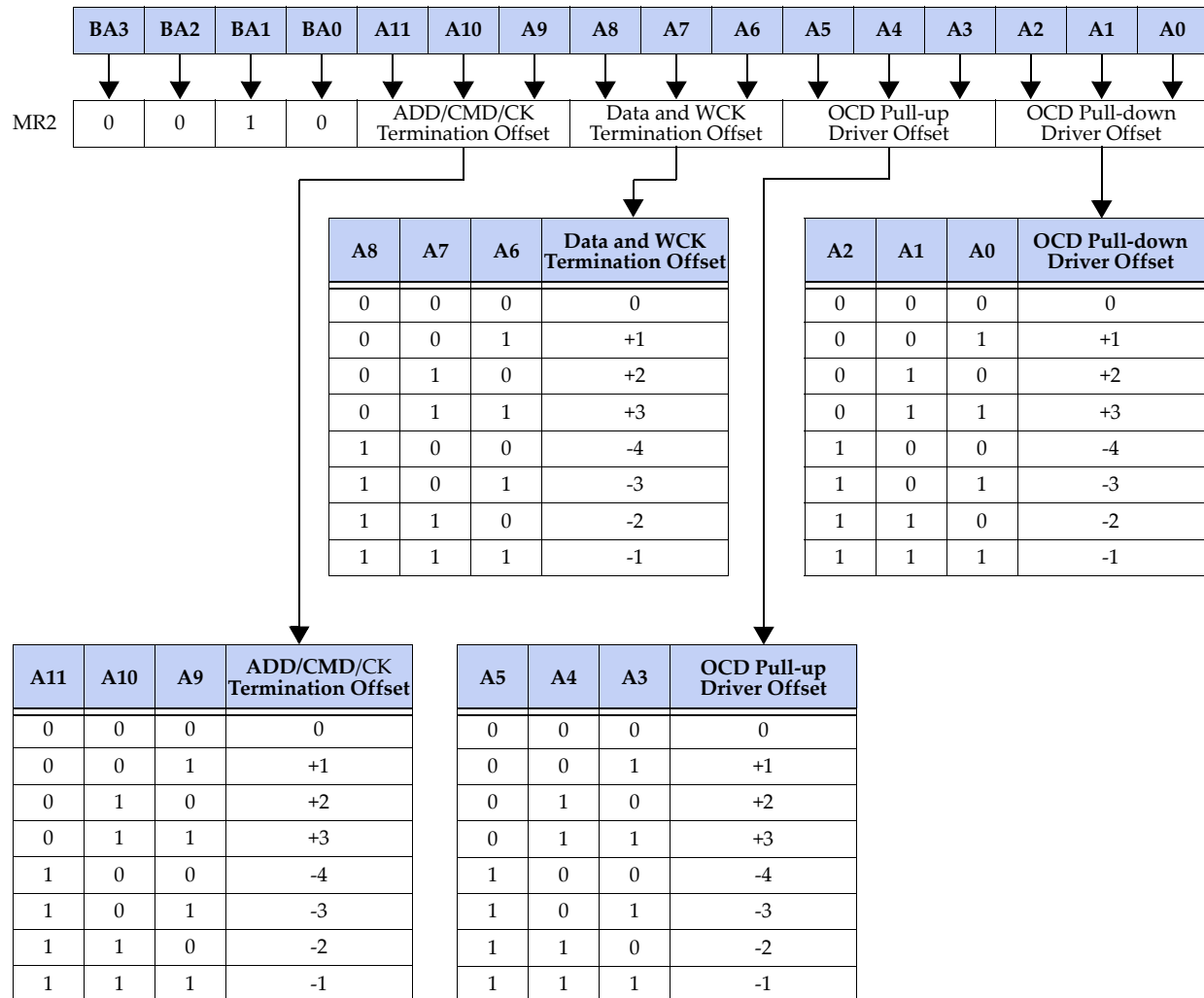


Figure 23 — Mode Register 2 (MR2) Definition

Impedance Offsets

The driver and termination impedances may be offset individually for pull-down driver, pull-up driver, DQ/DBI_n/WCK termination, and address/command/CK termination. The offset impedance step values may not be linear and vary across DRAM vendors and across PVT. With negative offset steps the driver strengths is decreased, and Ron and the termination value are increased. With positive offset steps the driver strengths is increased, and Ron and the termination value are decreased.

IV curves and AC timings are only guaranteed with zero offset.

4.3. MODE REGISTER 2 (MR2) (cont'd)

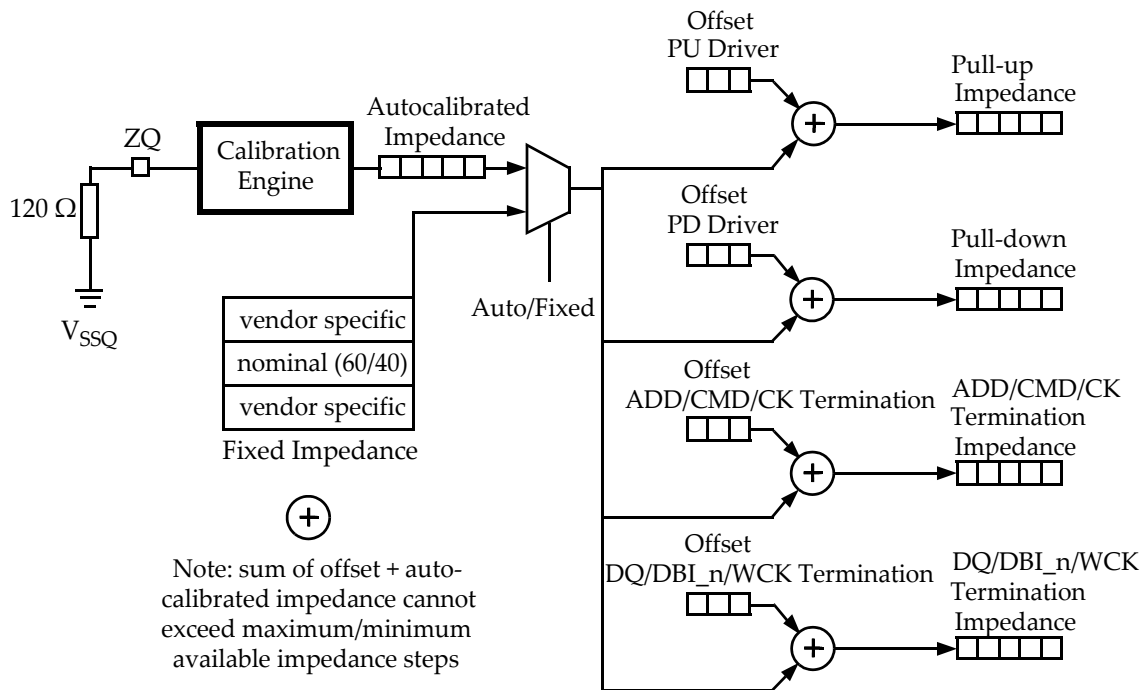


Figure 24 — Impedance Offsets

4.4 MODE REGISTER 3 (MR3)

MR3 controls functions like self refresh, WCK2CK training, RDQS mode, DRAM info, WCK termination and bank groups as shown in Figure 25. The register is programmed via the MRS command with BA[3:0] = 0011. Bits A[9:8] of this register are initialized with 0.

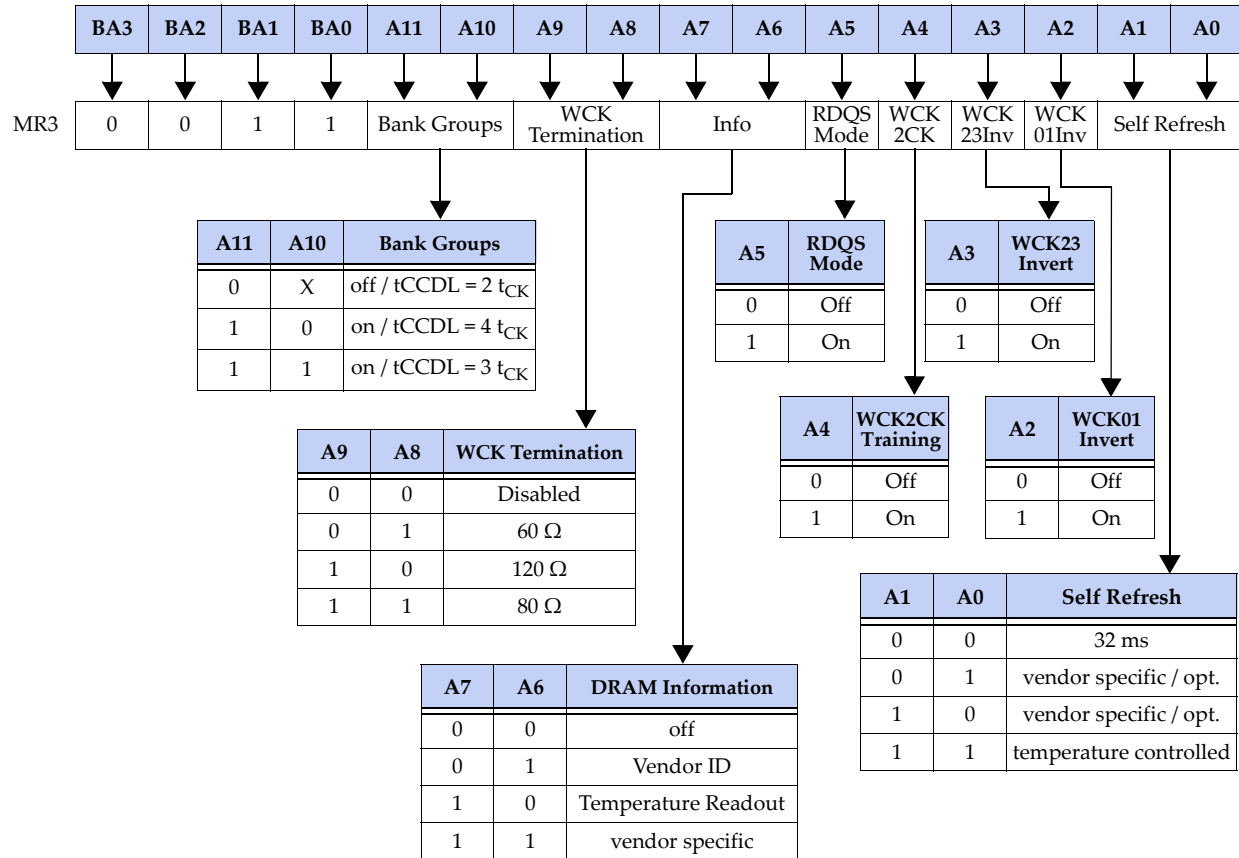


Figure 25 — Mode Register 3 (MR3) Definition

Self Refresh

The refresh interval in self refresh mode may be set to 32ms, or being controlled by an integrated temperature sensor. DRAM vendors may support additional settings related to other temperatures.

WCK01 / WCK23 Inversion

Bits A[3:2] control whether the internal phase should be flipped (inverted) after internally dividing the WCK01 and WCK23 clock inputs by 2, corresponding to a 4 UI phase shift in QDR mode and a 2 U.I. phase shift in DDR mode. The bits are used in conjunction with WCK2CK training mode.

WCK2CK

Bit A4 (WCK2CK) enables and disables the WCK2CK alignment training. For details on this training sequence, see the clause on TRAINING.

RDQS Mode

Bit A5 enables RDQS mode where the EDC pins act as a read strobe. CRC is not supported in RDQS mode, and all related bits in MR4 are ignored. See RDQS mode for more details.

4.4. MODE REGISTER 3 (MR3) (cont'd)

DRAM Information

Bits A[7:6] enable the DRAM information mode which outputs either the Vendor ID, the device's junction temperature or optionally other vendor specific device info. The Vendor ID identifies the manufacturer of the device, and provides the die revision and memory density.

WCK Termination

Bits A[9:8] define the (single-ended) termination for the WCK01_t, WCK01_c, WCK23_t and WCK23_c pins in combination with the driver strength setting. The termination is disabled by default; it can be set to a value of 60 Ω , 80 Ω or 120 Ω depending on system conditions. WCK termination may also be turned off.

Bank Groups

Bit A11 enables the bank groups feature, and bit A10 specifies the min column-to-column command delay t_{CCDL} . With A11 set to 1, back-to-back column accesses within a bank group have to be spaced by 3 or 4 clocks as defined by bit A10. With A11 set to 0, the bank groups feature is disabled and t_{CCDL} equals t_{CCDS} .

Parameter f_{CKBG} specifies the maximum CK clock frequency the device may be operated at with the bank groups feature disabled.

4.5 MODE REGISTER 4 (MR4)

MR4 defines the error detection code (EDC) features as shown in Figure 26. The register is programmed via the MRS command with BA[3:0] = 0100. Bits A[3:0] of this register are initialized with 1111.

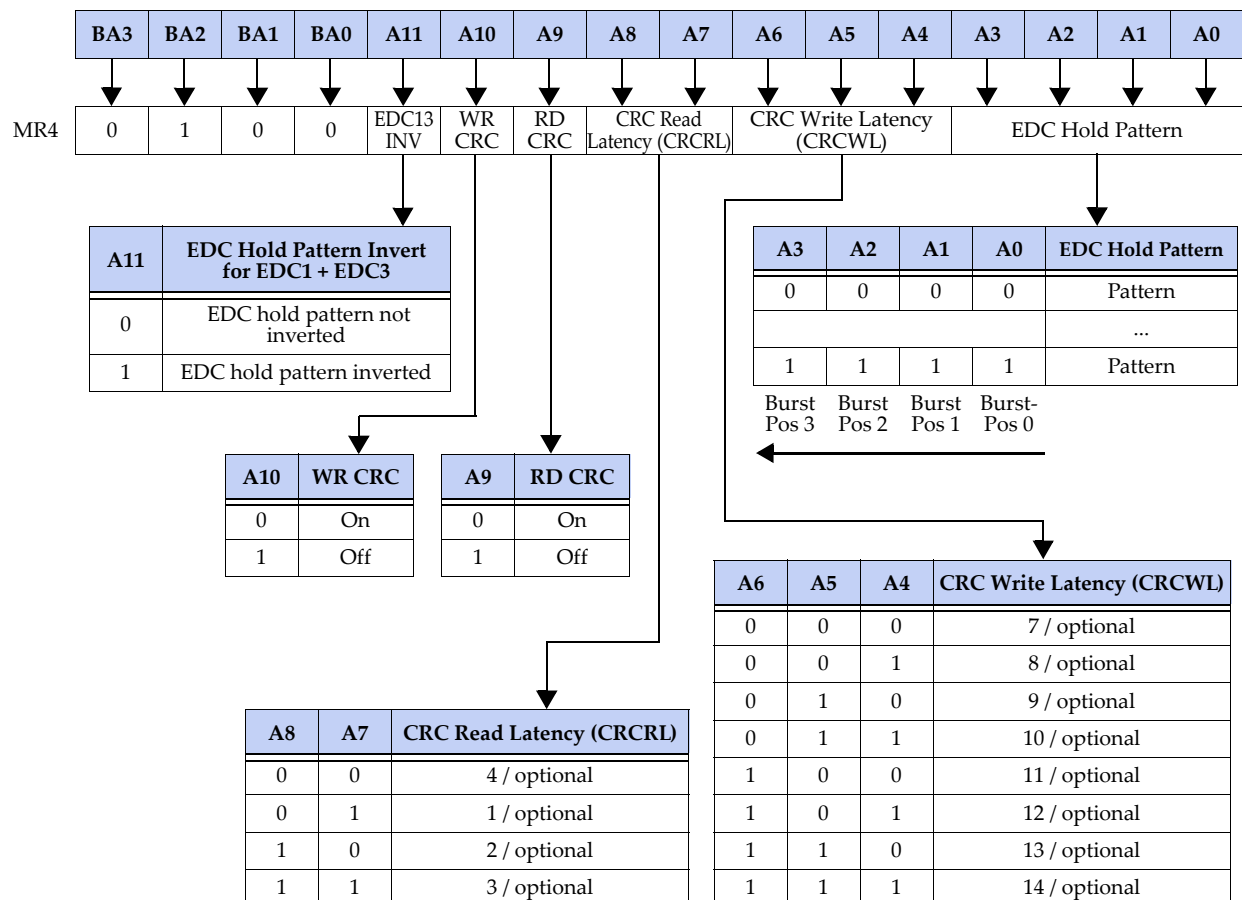


Figure 26 — Mode Register 4 (MR4) Definition

4.5. MODE REGISTER 4 (MR4) (cont'd)

EDC Hold pattern / EDC13 Invert

The 4-bit EDC hold pattern is considered a background pattern transmitted on the EDC pins. The register is initialized with 1111. The pattern is shifted from right to left and repeated with every clock cycle. The output timing is the same as of a READ burst.

CRC bursts calculated from writes or reads replace the EDC hold pattern for the duration of the bursts if CRC is enabled.

With each MRS command to MR4 that changes bits A[11:9] or A[3:0], the EDC hold pattern will be undefined for t_{MRD} .

The EDC hold pattern is not transmitted when the device is in address training mode, in WCK2CK training mode, RDQS mode, self refresh mode, reset state, in power-down state with the LP2 bit set, or when either EDC High-Z or VREFD Monitor mode are enabled.

With bit A11 set to 1, EDC1 and EDC3 transmit the inverted EDC hold pattern, resulting in a pseudo-differential pattern. Please note that this function is not available in x16 mode. Bit A11 is ignored for READ, WRITE and RDTR CRC bursts and the clock phase information in WCK2CK training mode.

Read CRC and CRC Read Latency (CRCRL)

Bit A9 controls the CRC calculation for READ bursts, and bits A[8:7] hold the CRC read latency. When enabled, the calculated CRC pattern is transmitted on the EDC pins after the CRC read latency. With Read CRC off, no CRC is calculated for READ bursts, and the EDC hold pattern is transmitted instead.

All CRCRL values are marked as “optional”, allowing the DRAM vendor to define the minimum and maximum supported CRCRL values; the supported CRCRL range must be contiguous.

Write CRC and CRC Write Latency (CRCWL)

Bit A10 controls the CRC calculation for WRITE bursts, and bits A[6:4] hold the CRC write latency. When enabled, the calculated CRC pattern is transmitted on the EDC pins after the CRC write latency. With Write CRC off, no CRC is calculated for WRITE bursts, and the EDC hold pattern is transmitted instead.

All CRCWL values are marked as “optional”, allowing the DRAM vendor to define the minimum and maximum supported CRCWL values; the supported CRCWL range must be contiguous.

4.6 MODE REGISTER 5 (MR5)

MR5 defines low power modes, PLL/DLL bandwidth and digital RAS as shown in Figure 27. The register is programmed via the MRS command with BA[3:0] = 0101.

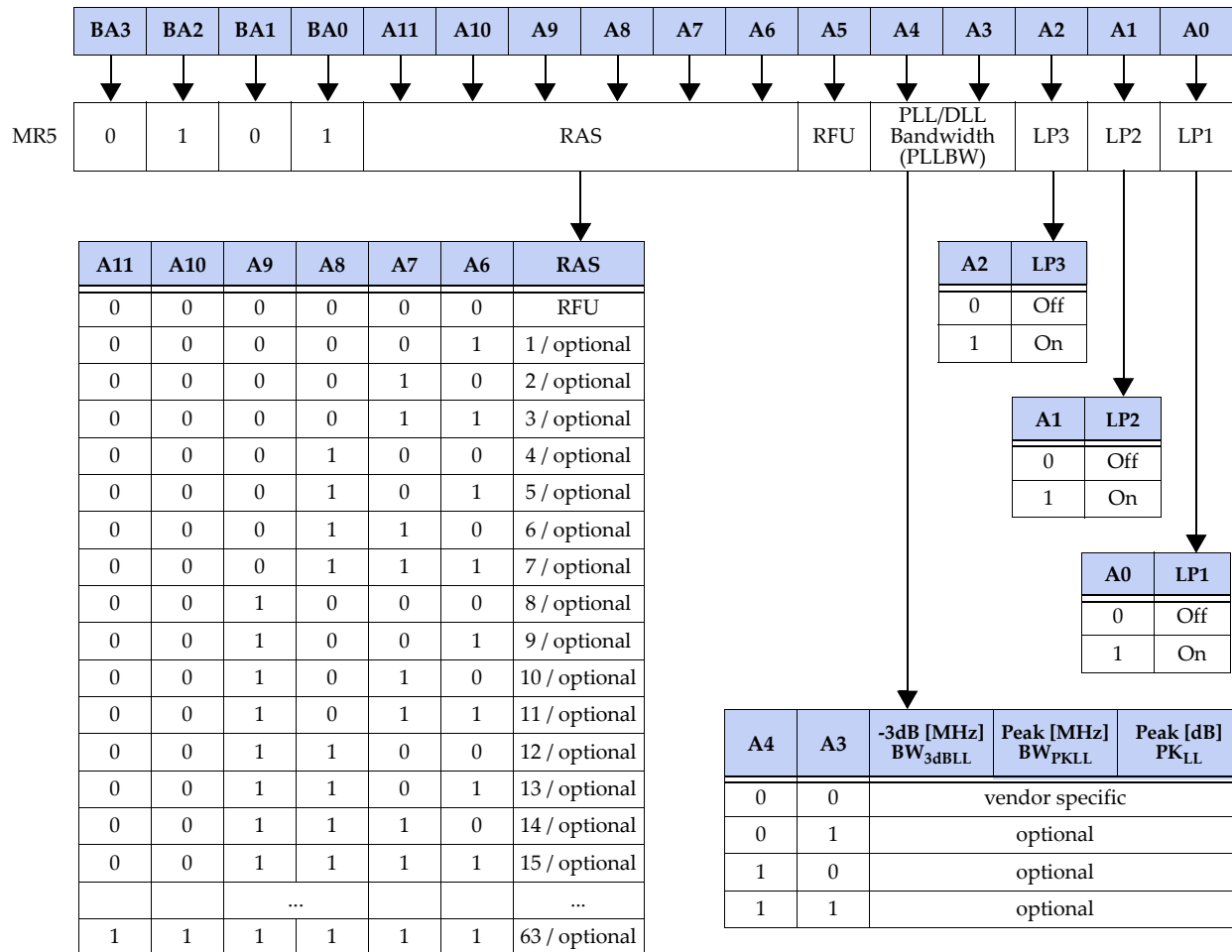


Figure 27 — Mode Register 5 (MR5) Definition

Low Power Modes (LP1, LP2, LP3)

Bits A[2:0] control several low power modes of the device. The modes are independent of each other.

When bit A0 (LP1) is set, several core parameters are relaxed for lower power consumption of the device.

When bit A1 (LP2) is set, the WCK receivers may be turned off during power-down.

When bit A2 (LP3) is set, RDTR, WRTR and LDFF commands shall not be issued while a REFRESH command is being executed.

PLL/DLL Bandwidth

The PLL/DLL bandwidth may optionally be configured to match system characteristics. Each setting defines a unique combination of -3dB corner frequency, peaking frequency and peaking magnitude. All values and tolerances are vendor specific. The use of all settings except 000 is optional.

4.6. MODE REGISTER 5 (MR5) (cont'd)

RAS

RAS must be programmed with a value greater than or equal to $RU\{t_{RAS}/t_{CK}\}$, where RU stands for round up, t_{RAS} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time. All RAS values are marked as “optional”, allowing the DRAM vendor to define the minimum and maximum supported RAS values; the supported RAS range must be contiguous.

If the DRAM vendor does not support the mode register definition of t_{RAS} in clock cycles, the RAS mode register settings will be ignored.

4.7. MODE REGISTER 6 (MR6)

MR6 controls V_{REFD} levels for two of the two of the four data bytes as shown in Figure 28. The register is programmed via the MRS command with BA[3:0] = 0110.

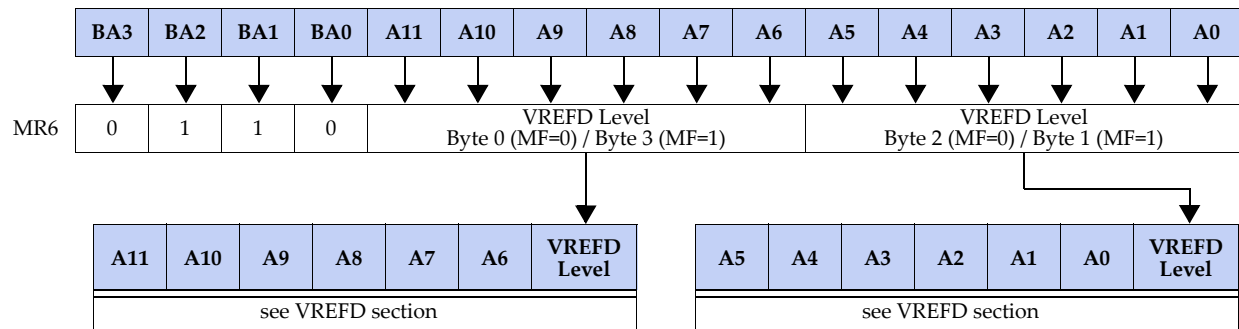


Figure 28 — Mode Register 6 (MR6) Definition

Input Reference Voltage for DQ and DBI_n Pins

Separate reference voltage circuits are associated with each data byte (see VREFD clause). Register bits in MR6 and MR9 (see MODE REGISTER 9 (MR9)) control the V_{REFD} level as summarized in Table 10; the bits are associated with the physical location of the data bytes (see BALLOUT). It is pointed out that in x16 (clamshell) mode it is required to use the Mode Register 0-14 Enable (MRE) bits in MR15 to selectively program the V_{REFD} levels either for the non-mirrored or the mirrored device.

Table 10 — V_{REFD} Level Control

Pin Group	Data Byte (MF=0)	Data Byte (MF=1)	Control Bits	Byte Active	
				x32 Mode	x16 Mode
Rows B to G, columns 3 + 4	Byte 0	Byte 3	MR6 A[11:6]	Yes	Yes
Rows B to G, columns 11 + 12	Byte 1	Byte 2	MR9 A[11:6]	Yes	No
Rows N to V, columns 11 + 12	Byte 2	Byte 1	MR6 A[5:0]	Yes	Yes
Rows N to V, columns 3 + 4	Byte 3	Byte 0	MR9 A[5:0]	Yes	No

4.8 MODE REGISTER 7 (MR7)

MR7 controls functions like the WCK alignment point, PLL fast lock, PLL delay compensation, low frequency mode, auto synchronization, DQ preamble, half VREFC, half VREFD, VDD range and DCC as shown in Figure 29. The register is programmed via the MRS command with BA[3:0] = 0111.

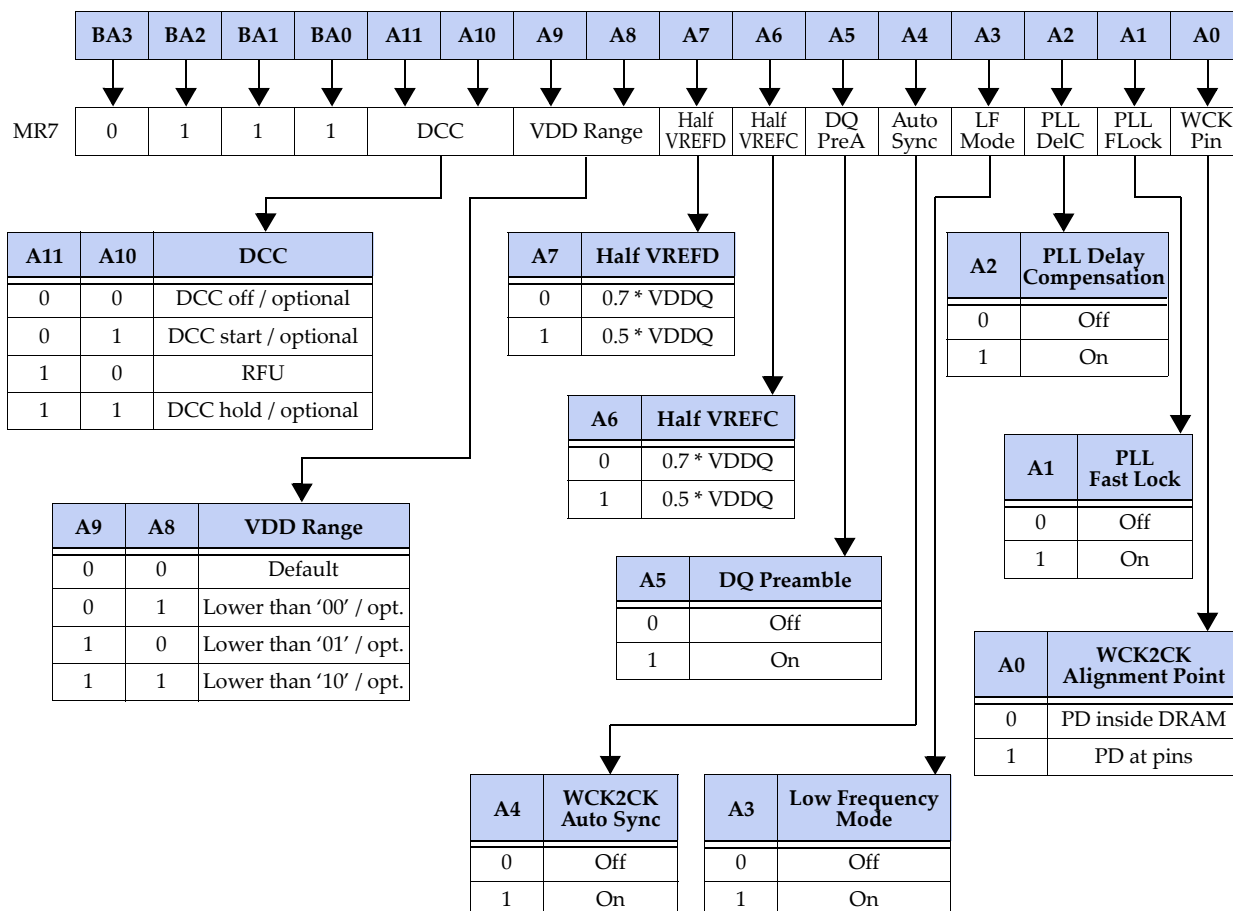


Figure 29 — Mode Register 7 (MR7) Definition

WCK2CK Alignment Point (WCK PIN)

Bit A0 defines the position of the alignment point between CK and WCK clocks. When set to 0, the alignment point will be located at the phase detector inside the GDDR5X SGRAM. When set to 1, the alignment point will be located at the CK and WCK pins. The maximum CK clock frequency in PIN mode is specified by f_{CKPIN} .

PLL Fast Lock

When enabled by bit A1, the PLL's lock time is reduced to t_{FLK} at the expense of a higher power consumption. The bit may be reset once the PLL has locked. PLL Fast Lock is optional.

PLL Delay Compensation

When enabled by bit A2, the PLL's feedback path has a delay equivalent to the WCK clock tree delay.

4.8. MODE REGISTER 7 (MR7) (cont'd)

Low Frequency Mode

When Low Frequency Mode is enabled by bit A3, the power consumption of input receivers and clock trees is reduced. The maximum operating frequency for this low frequency mode (f_{CKLF}) is given in the vendor's datasheet.

WCK2CK Auto Synchronization

GDDR5X SGRAMs support a WCK2CK automatic synchronization mode that eliminates the need for WCK2CK training upon power-down exit or for reducing WCK2CK training time at low frequency. This mode is controlled by bit A4. For a detailed description see WCK2CK Auto Synchronization in the clause entitled WCK2CK Training.

DQ Preamble

When enabled by bit A5, non-gapless READ bursts are preceded by a fixed DQ preamble on the DQ and DBI_n pins of 1 t_{CK} duration. The programmed READ latency does not change when DQ preamble is enabled. The pattern is not encoded with RDBI, however, if RDBI is disabled, the DBI_n pins do not toggle and drive a HIGH.

DQ preamble is supported in QDR mode only; it must be disabled in DDR mode.

Half VREFC and Half VREFD

Bits A6 controls Half VREFC and bit A7 controls Half VREFD. The bits shall be used to adjust the V_{REF} level in case the device is operated without termination. See VREFC and VREFD clause for more details.

VDD Range

Bits A[9:8] are used to adapt DRAM characteristics like internal supply voltages when the actual V_{DD} is lower than the default operating range. The default 00 setting represents the highest V_{DD} supply voltage range supported by the device which typically is 1.35V. All other field values are optional, and the VDD ranges of the optional fields represent voltage ranges lower than the default range in a decreasing voltage order. The actual V_{DD} supply voltage ranges itself are vendor specific.

The bits must be set during device initialization prior to WCK2CK training. GDDR5X SGRAMs supporting multiple voltage and requiring the use of the VDD range must tolerate power-up with a VDD range setting that does not correspond to the actual supply voltage; this includes that the device must be able to execute the MRS command that sets VDD range to the correct value while being operated with an incorrect VDD range setting.

Duty Cycle Correction (DCC)

Bits A[11:10] control the operation of the optional duty cycle corrector (DCC). The DCC can be used to cancel out a static duty cycle error on the WCK clocks. See the clause entitled Duty Cycle Correction (DCC) for more details.

4.9 MODE REGISTER 8 (MR8)

MR8 controls functions like the MSBs for read latency (RLmrs) and write recovery (WR), EDC High-Z, Hibernate self refresh, PLL/DLL range, VREF C2D, VREFD monitor, address compatibility mode, QDR/DDR operating mode, and CK termination as shown in Figure 30. The register is programmed via the MRS command with BA[3:0] = 1000. Bits A[11:10] of this register are initialized with 0.

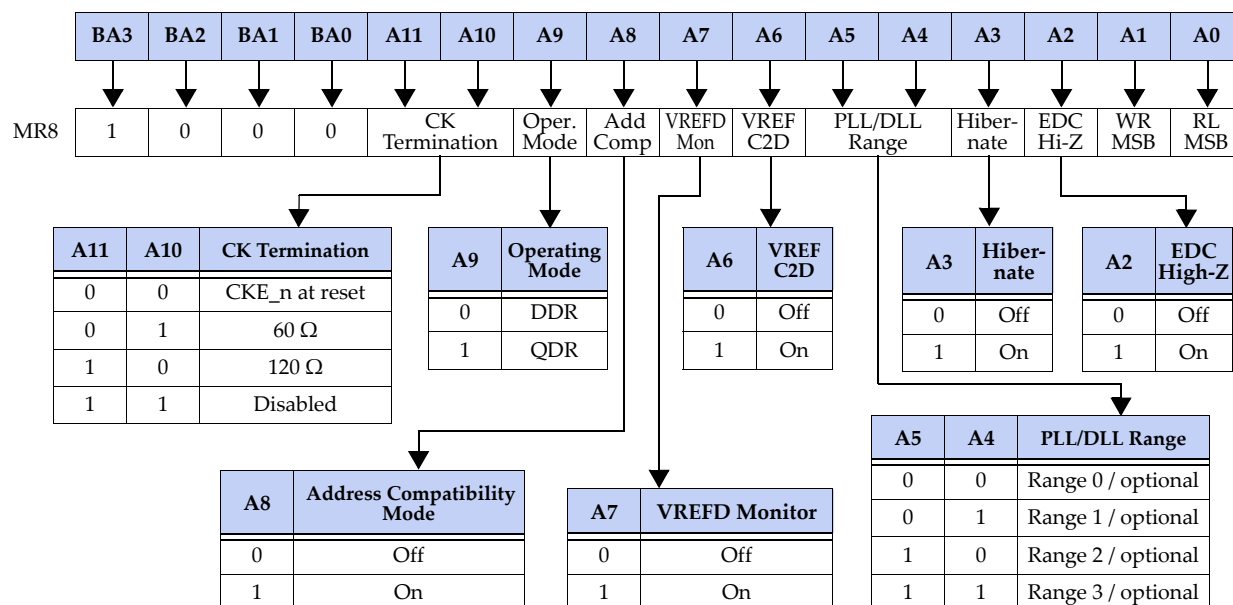


Figure 30 — Mode Register 8 (MR8) Definition

RL MSB and WR MSB

Bits A0 and A1 define the MSB for the read latency (RLmrs) and the write recovery (WR), respectively. See MR0 for more details.

EDC High-Z

With bit A2 set to 1, the EDC pins are in High-Z state. The EDC High-Z function takes precedence over all other features that define the EDC pin's data pattern.

Hibernate Self Refresh

With bit A3 set to 1, the device enters Hibernate self refresh mode with the next SELF REFRESH ENTRY command. The bit is self-clearing.

PLL/DLL Range

Bits A[5:4] may be used to adapt the PLL/DLL characteristics to distinct minimum-to-maximum WCK frequency ranges. All settings and associated WCK frequencies are vendor specific. The DRAM vendor specifications should be consulted for more details.

VREF C2D

Bit A6 enables an internal bridge between the V_{REFC} and V_{REFD} circuits that allows an external V_{REFD} voltage to be supplied via the V_{REFC} pin. See the VREFD clause for more details.

VREFD Monitor

Bit A7 controls the VREFD Monitor mode which allows the observation of the internal V_{REFD} voltage at the EDC pins of both double bytes. See the VREFD clause for more details.

4.9. MODE REGISTER 8 (MR8) (cont'd)

Address Compatibility Mode (Add Comp)

Bit A8 enables the address compatibility mode. The column address received on address inputs A[5:0] is internally used as CAL and CAU in this mode. This mode is intended for controllers that do not support different column addresses CAL and CAU. See the ADDRESSING clause for more details.

Operating Mode

Bit A9 selects between DDR and QDR operating modes.

CK Termination

Bits A[11:10] define the (single-ended) termination for the CK_t and CK_c pins. The default setting (00) provides that the CK termination is determined by latching CKE_n on the rising edge of RESET_n. The CK termination can also be set to a value of 60 Ω which is intended for a single loaded system, or 120 Ω which is intended for clamshell configurations with two devices sharing a common CK clock. The CK termination may also be turned off.

4.10. MODE REGISTER 9 (MR9)

MR9 controls V_{REFD} levels for two of the four data bytes as shown in Figure 31. The register is programmed via the MRS command with BA[3:0] = 1001.

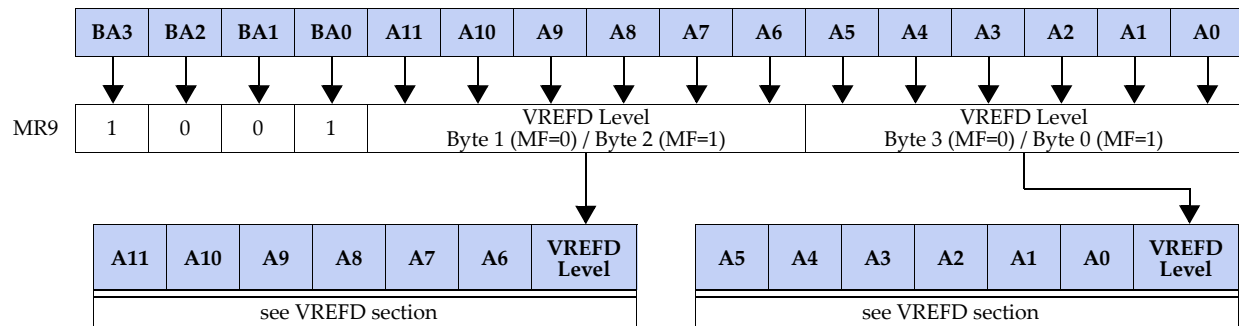


Figure 31 — Mode Register 9 (MR9) Definition

Please refer to MODE REGISTER 6 (MR6) for details.

4.11. MODE REGISTER 10 (MR10)

MR10 is reserved. The register is programmed via the MRS command with BA[3:0] = 1010.

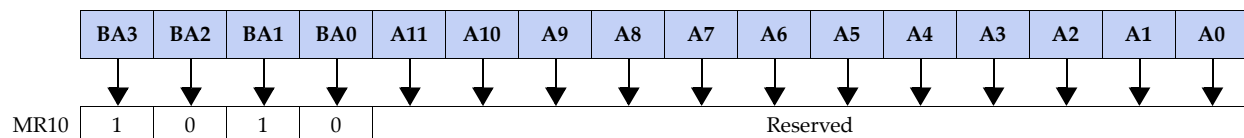


Figure 32 — Mode Register 10 (MR10) Definition

4.12 MODE REGISTER 11 (MR11)

MR11 defines row segment and 2 banks mask for the Partial Array Self Refresh (PASR) as shown in Figure 33. The register is programmed via the MRS command with BA[3:0] = 1011.

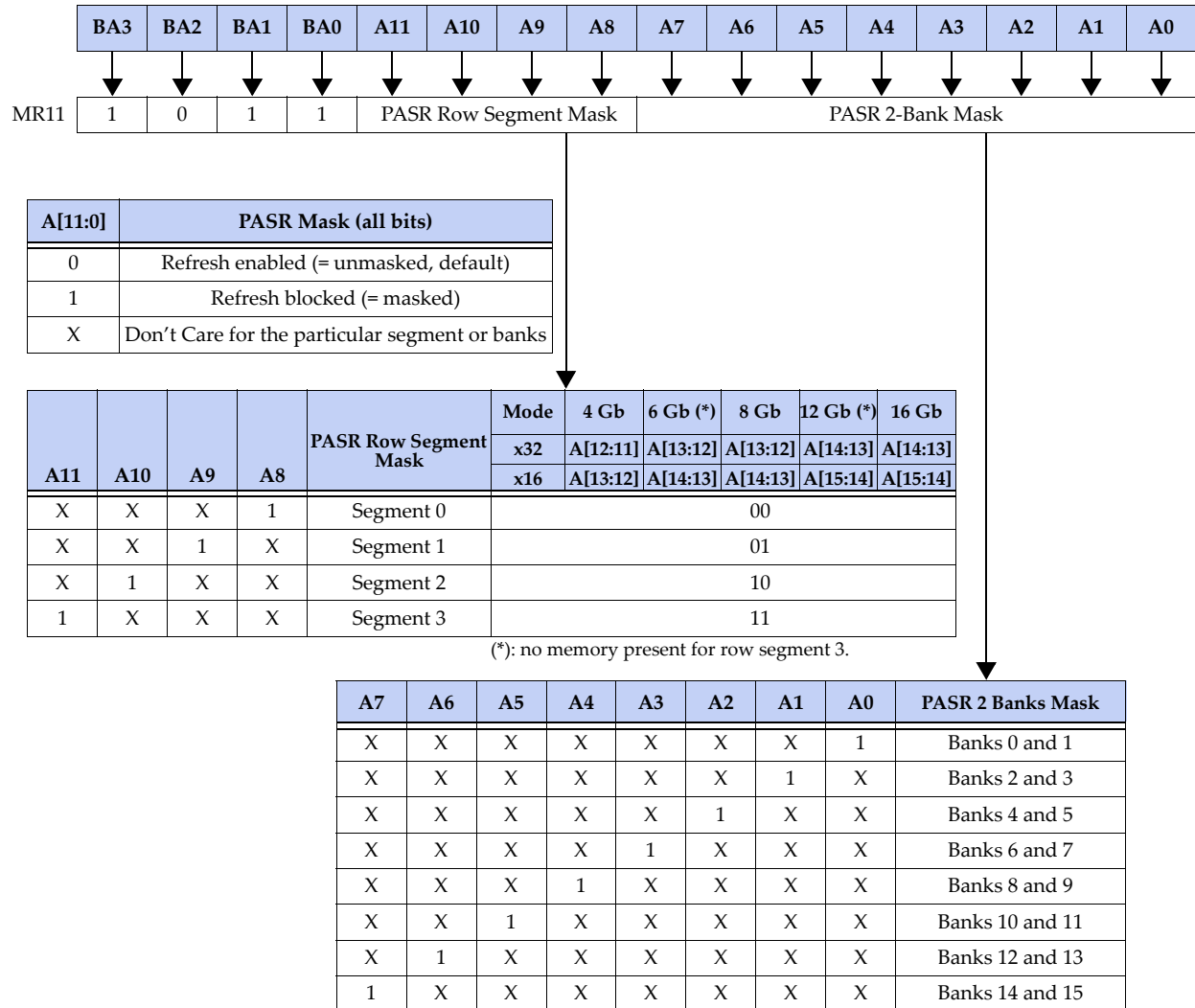


Figure 33 — Mode Register 11 (MR11) Definition

Partial Array Self Refresh (PASR)

Bits A[11:8] define the row segment mask and bits A[7:0] define the 2 banks mask for the Partial Array Self Refresh (PASR) feature. The default 0 setting enables the refresh, and the 1 setting blocks the refresh for the selected row segment or 2 banks. An example of how the bits can be used to mask banks and row segments from refresh can be found in the Partial Array Self Refresh (PASR) clause.

4.13 MODE REGISTERS 12 TO 14 (MR12, MR13, MR14)

MR12, MR13, and MR14 is reserved for vendor specific features. The registers are programmed via the MRS command with BA[3:0] = 1100, 1101 and 1110, respectively.

4.14 MODE REGISTER 15 (MR15)

MR15 controls address training mode and access to Mode Registers 0 to 14 (MRE) as shown in Figure 34. The register is programmed via the MRS command with BA[3:0] = 1111.

MR15 is a special register that operates in SDR addressing mode and latches data on the rising edge of CK_t. Therefore nothing is latched on the rising edge of CK_c as shown in Figure 34. Increased address setup and hold times are assumed to ensure the MRS command to this register is successful while address training (ADT) has not taken place and the integrity of DDR addresses may not be guaranteed.

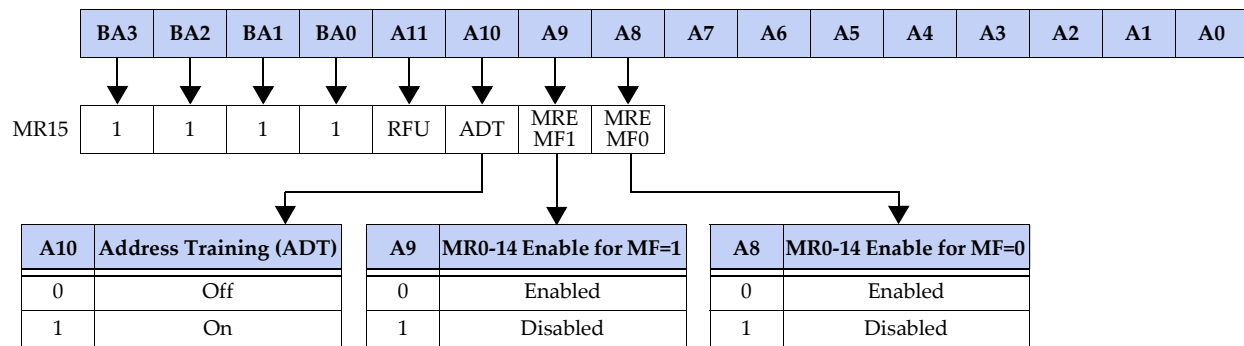


Figure 34 — Mode Register 15 (MR15) Definition

Address Training (ADT)

Address training mode is enabled and disabled with bit A10.

Mode Register 0-14 Enable (MRE)

When disabled by bit A8 (for devices configured as MF=0) or bit A9 (for devices configured as MF=1), the device will ignore any MRS command to registers MR0 to MR14 as shown in Figure 35. MRS commands to MR15 are not affected and are always executed. This function allows for the individual configuration of two devices sharing a common address bus.

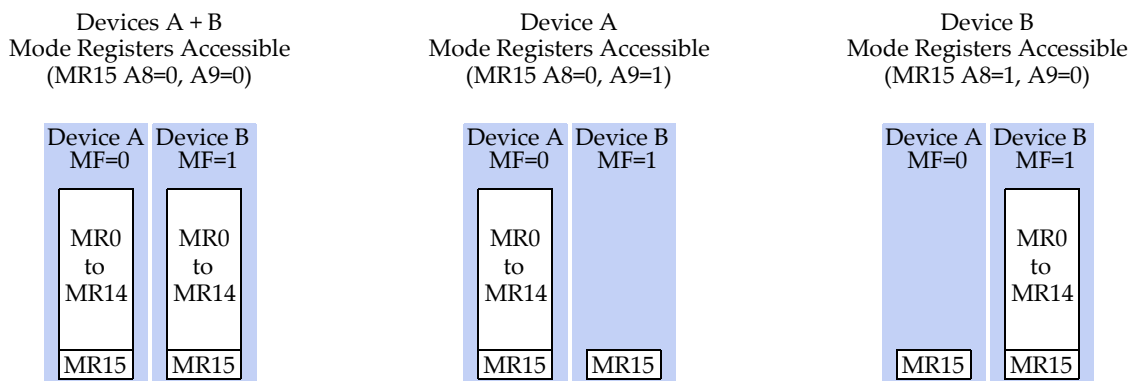


Figure 35 — Mode Register Enable

5 DEVICE INITIALIZATION

5.1 POWER-UP SEQUENCE

GDDR5X SGRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The mode registers do not have reset default values, except for ADD/CMD, CK, WCK and data termination, ABI, the EDC hold pattern and PASR. If the mode registers are not set during the initialization sequence, it may lead to unspecified operation.

1. Apply power to V_{PP} . Apply power to V_{DD} at the same time or after power is applied to V_{PP} . Apply power to V_{DDQ} at the same time or after power is applied to V_{DD} . V_{PP} must be equal to or higher than V_{DD} at all times the device is powered up.
2. Apply V_{REFC} at same time or after power is applied to V_{DDQ} , or pull the V_{REFC} pin Low to select internal V_{REFC} .
3. The voltage levels on all signal pins must be less than or equal to V_{DD} and V_{DDQ} on one side and must be larger than or equal to V_{SS} on the other side.
4. Assert $RESET_n$ Low to ensure all drivers are in High-Z and all ODT are off. Maintain $RESET_n$ Low for a minimum time of t_{INIT1} .
5. Assert and hold NOP command. Assert CKE_n Low or High for the desired ADD/CMD and CK ODT at least a time of t_{AT5} before $RESET_n$ is pulled High. At the same time pull EDC1 (with MF=0; pin is EDC2 with MF=1) High for x32 mode or Low for x16 mode. Drive CK_t , WCK_t to static Low level, and CK_c , WCK_c to static High level.
6. After $RESET_n$ is pulled High, maintain CKE_n and EDC1 (with MF=0; pin is EDC2 with MF=1) stable for a minimum time of t_{ATH} .
7. Pull CKE_n Low after t_{ATH} is satisfied. The device performs the initial impedance calibration during this time; this will be done without external clocks. Latest after t_{INIT2} the device enables the CK and ADD/CMD ODT as determined by CKE_n in steps 5 and 6.
8. Provide a stable CK clock for a minimum of t_{INIT3} cycles.
9. Issue a PRECHARGE ALL command followed by NOP commands until t_{RP} is satisfied.
10. Issue MRS command to MR15 to set the GDDR5X SGRAM into address training mode (optional).
11. Complete address training (optional).
12. Issue MRS command to read the Vendor ID.
13. Issue MRS command to set WCK termination values.
14. Provide stable WCK clocks.
15. Issue MRS commands to the mode registers in any order to select QDR or DDR operating mode, PLL/DLL on/off mode, the position of the WCK2CK alignment point, and to set $WLMrs$, $RLMrs$, $CRCWL$ and $CRCRL$ to appropriate values. All these features must be programmed before WCK2CK training, and t_{MRD} must be met during this procedure.
16. Issue two REFRESH commands followed by NOP until t_{RFC} is satisfied.
17. After any necessary training sequences such as WCK2CK training, READ training (LDFF, RDTR) and WRITE training (WRTR, RDTR), the device is ready for normal operation.

Table 11 — Address/Command and CK ODT

CKE_n AT RESET_n HIGH TRANSITION	VALUE
Low	$ZQ/2 = 60\ \Omega$
High	$ZQ = 120\ \Omega$