

JEDEC STANDARD

High Bandwidth Memory DRAM (HBM1, HBM2)

JESD235D

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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HIGH BANDWIDTH MEMORY (HBM) DRAM

(From JEDEC Board Ballot JCB-20-10, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories, under item number 1797.99L, Rev. 4.20).

1 Scope

The HBM DRAM is tightly coupled to the host compute die with a distributed interface. The interface is divided into independent channels. Each channel is completely independent of one another. Channels are not necessarily synchronous to each other. The HBM DRAM uses a wide-interface architecture to achieve high-speed, low power operation. Each channel interface maintains a 128 bit data bus operating at double data rate (DDR).

2 Features

- 256 bit prefetch per memory read and write access
- $BL = 2$ and 4
- 128 DQ width + optional ECC pin support/channel
- Legacy mode and Pseudo Channel (PC) mode operation; 64 DQ width for PC mode
- Differential clock inputs (CK_t/CK_c) for command/address
- Double data rate (DDR) command/address. Row Activate commands require two cycles, all other commands require one cycle
- Semi-independent row and column command interfaces allowing Activates/Precharges to be issued in parallel with Read/Writes.
- Data referenced to unidirectional differential data strobes $RDQS_t/RDQS_c$ and $WDQS_t/WDQS_c$. One strobe pair each per DWORD
- Up to 8 channels / device
- Channel density of 1 Gb to 16 Gb
- 8, 16, 32 or 48 banks per channel; varies by device density/channel
- Bank grouping supported
- 2 KB page size per channel
- DBIac support configurable via MRS
- Data mask for masking write data per byte
- Self refresh modes
- I/O voltage 1.2 V
- DRAM core voltage 1.2 V, independent of I/O voltage
- Unterminated data/address/cmd/clk interfaces
- Temperature sensor with 3-bit encoded range output

3 Organization

The HBM DRAM is optimized for high-bandwidth operation to a stack of multiple DRAM devices across a number of independent interfaces called channels. It is anticipated that each DRAM stack will support up to 8 channels. Figure 1 shows an example stack containing 4 DRAM dies, each die supporting 2 channels. Each die contributes additional capacity and additional channels to the stack (up to a maximum of 8 channels per stack).

Each channel provides access to an independent set of DRAM banks. Requests from one channel may not access data attached to a different channel. Channels are independently clocked, and need not be synchronous.

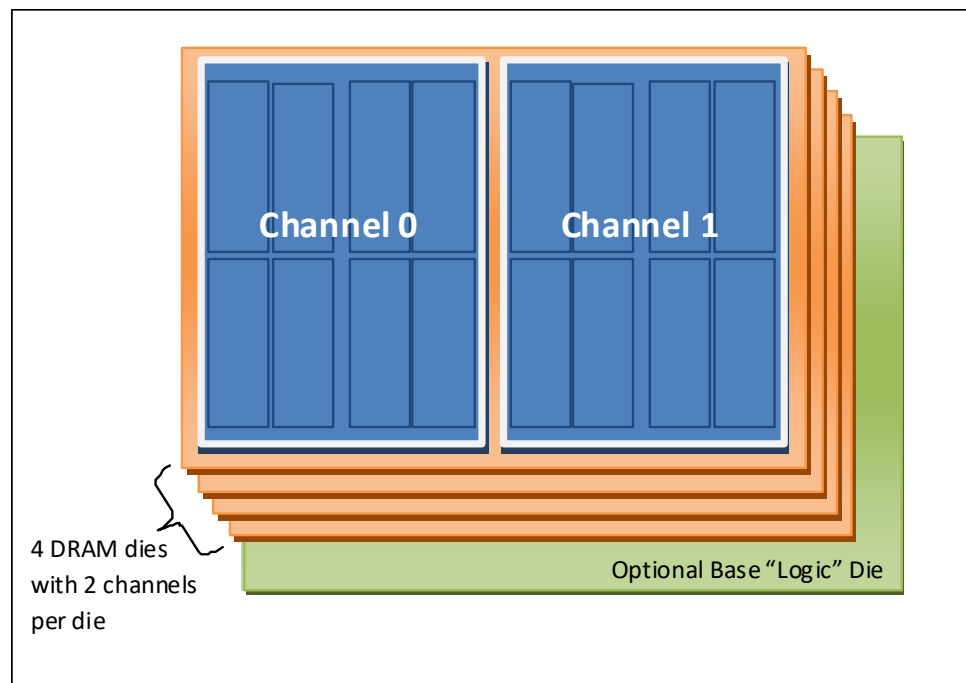


Figure 1 — General Overview of a DRAM Die Stack with Channels

The DRAM vendor may choose to require an optional interface die that sits at the bottom of the stack and provides signal redistribution and other functions. The vendor may choose to implement many of the logic functions typically found on DRAM die on this logic die. This standard does not explicitly require nor prohibit such a solution.

The division of channels among the DRAM dies within a stack is left to the vendor. The example above, with the memory for two channels implemented on each die, is not a required organization. Organizations are permitted where the memory for a single channel is distributed among multiple dies; however, all accesses within a single channel must have the same latency for all accesses. Similarly, vendors may develop products where each memory die can flexibly support 1, 2, or 4 channels – enabling 8-channel configurations with stacks of 2 to 8 dies while keeping all data for a given channel on one die.

Since each channel is independent, much of this standard will describe a single channel. Where signal names are involved, families of signals belonging to a given channel will have the suffix a, b, ..., h for channels a through h. If no suffix is present, the signal(s) being described are generic instances of the various per-channel signals.

3.1 Channel Definition

Each channel consists of an independent command and data interface. RESET_n, IEEE1500 test port and power supply signals are common to all channels. A channel provides access to a discrete pool of memory; no channel may access the memory storage for a different channel.

Each channel interface provides an independent interface to a number of banks of DRAM of a defined page size. See [HBM Channel Addressing](#).

3.1.1 Summary of Per-Channel Signals

[Table 1](#) outlines the signals required for each channel, and [Table 2](#) adds global signals that are required once per HBM device. See also [Table 82](#) for 15 additional global signals associated with the IEEE1500 test access port.

Table 1 — Single Channel Signal Count

Function	# uBumps	Notes
Data	128	DQ[127:0]
Column Command/Address	8 or 9	C[7:0] or C[8:0]
Row Command/Address	6 or 7	R[5:0] or R[6:0]
DBI	16	1 DBI per 8 DQs
DM	16	1 DM per 8 DQs
PAR	4	1 PAR per 32 DQs
DERR	4	1 DERR per 32 DQs
Strobes	16	1 RDQS_t/RDQS_c, WDQS_t/WDQS_c per 32 DQs
Clock	2	CK_t/CK_c
CKE	1	CKE
AERR	1	AERR
Redundant Data	8	RD[7:0]
Redundant Row	1	RR
Redundant Column	1	RC
Total	212 or 214	

Table 2 — Global Signal Count

Function	# uBumps	Notes
Reset	1	RESET_n
TEMP[2:0]	3	TEMP[2:0]
CATTRIP	1	Catastrophic Temperature Sensor
Total	5	

3.1.2 Legacy Mode and Pseudo Channel Mode

HBM DRAM defines two modes of operation depending on channel density. The mode support is fixed by design and is indicated on bits [17:16] of the `DEVICE_ID` wrapper register.

3.1.2.1 Legacy Mode (HBM1)

Legacy mode provides 256 bit prefetch per memory Read and Write access when the burst length (BL) is set to 2. Address bit BA4 is a “Don’t Care” in this mode. Devices supporting legacy mode are also referred to as HBM1.

3.1.2.2 Pseudo Channel Mode (HBM2)

Pseudo channel (PC) mode divides a channel into two individual sub-channels of 64 bit I/O each, providing 256 bit prefetch per memory read and write access for each pseudo channel. Devices supporting PC mode are also referred to as HBM2. PC mode requires that the burst length (BL) is set to 4. Each read or write access may internally be executed as two seamless array accesses or a single array access, depending on DRAM vendor’s implementation. Both implementations are equivalent for the memory controller as they result in the same prefetch per Read and Write access.

Both pseudo channels operate semi-independent: they share the channel’s row and column command bus as well as CK and CKE inputs, but decode and execute commands individually as illustrated in [Figure 2](#). Address BA4 is used to direct commands to either to pseudo channel 0 (PC0, BA4 = 0) or pseudo channel 1 (PC1, BA4 = 1). Power-down and self refresh are common to both pseudo channels due to the shared CKE pin.

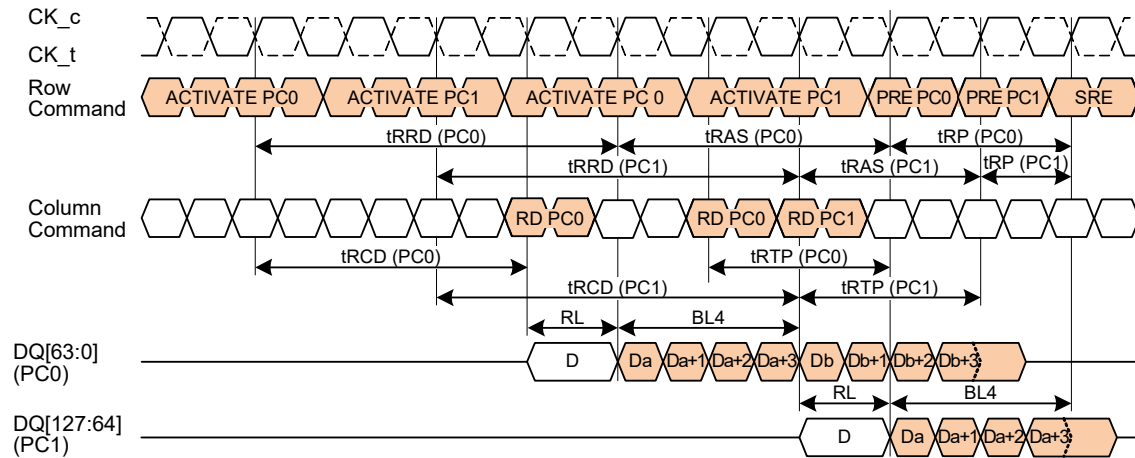
Array access timings as listed in the table below are applicable for each individual pseudo channel. For example, an ACTIVATE to PC0 can be followed by an ACTIVATE to PC1 as shown in [Figure 2](#). However a subsequent ACTIVATE to PC0 can only be done after t_{RRD} (PC0). For commands that are common to both pseudo channels (PDE, PDX, SRE, SRX and MRS) it is required that the respective timing conditions are met by both pseudo channels when issuing that command. PC mode requires that burst length is set to 4. Both pseudo channels also share the channel’s mode registers.

All I/O signals of `DWORD0` and `DWORD1` are associated with pseudo channel 0, and all I/O signals of `DWORD2` and `DWORD3` with pseudo channel 1.

Table 3 — Array Access Timings Counted Individually Per Pseudo Channel

Array Timing Group	Timing Parameters
Row Access Timings	t_{RC} , t_{RAS} , t_{RCDRD} , t_{RCDWR} , t_{RRDL} , t_{RRDS} , t_{FAW} , t_{RTPL} , t_{RTPS} , t_{RP} , t_{WR}
Column Access Timings	t_{CCDL} , t_{CCDS} , t_{CCDR} , t_{WTRL} , t_{WTRS} , t_{RTW}
Refresh Timings	t_{RFC} , t_{RFCB} , t_{RREFD} , t_{REFI} , t_{REFISB} , t_{RTW}

3.1.2.2 Pseudo Channel Mode (HBM2) (cont'd)



1. PC0 = pseudo channel 0 (BA4 = 0); PC1 = pseudo channel 1 (BA4 = 1).
2. RL = 1 is shown as an example. Other timings parameters (tMRD, tRRD, tRAS, tRP, tRTP) are not to scale.
3. Self refresh entry (SRE) requires that tRP is satisfied in both pseudo channels.

Don't Care

Figure 2 — Pseudo Channel Mode Operation

3.1.3 Dual Command Interfaces

To enable higher performance, HBM DRAMs exploit the increase in available signals in order to provide semi-independent row and column command interfaces for each channel. These interfaces increase command bandwidth and performance by allowing read and write commands to be issued simultaneously with other commands like activates and precharges. See [Commands](#).

3.2 Addressing

Table 4 — HBM Channel Addressing

Legacy Mode ⁶							Notes
Density per Channel	1 Gb	2 Gb	4 Gb				
Prefetch Size (bits)	256	256	256				
Row Address	RA[12:0]	RA[13:0]	RA[13:0]				
Column Address	CA[5:0]	CA[5:0]	CA[5:0]				
Bank Address	BA[2:0]	BA[2:0]	BA[3:0]				
Page Size	2 KB	2 KB	2 KB				
Refresh	8K/32 ms	8K/32 ms	8K/32 ms				
Refresh Period	3.9 us	3.9 us	3.9 us				
Density Code	0001	0010	0011				11
Pseudo Channel (PC) Mode ^{5,6}							Notes
Density per Channel	2 Gb	4 Gb	6 Gb	8 Gb			
Density per PC	1 Gb	2 Gb	3 Gb	4 Gb			
Prefetch Size per PC (bits)	256	256	256	256			1,3
Row Address	RA[13:0]	RA[13:0]	RA[14:0] ⁹	RA[14:0]			
Column Address	CA[5:1]	CA[5:1]	CA[5:1]	CA[5:1]			
Bank Address	BA[2:0]	BA[3:0]	BA[3:0]	BA[3:0]			
Page Size per PC	1 KB	1 KB	1 KB	1 KB			
Refresh	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms			
Refresh Period	3.9 us	3.9 us	3.9 us	3.9 us			
Density Code	0010	0011	0101	0110			11
Pseudo Channel (PC) Mode ^{5,6}							Notes
Configuration ⁷	8 Gb 8-High	8 Gb 12-High	12 Gb 8-High	12 Gb 12-High	16 Gb 8-High	16 Gb 12-High	
Density per Channel	8 Gb	12 Gb	12 Gb	18 Gb	16 Gb	24 Gb	
Density per PC	4 Gb	6 Gb	6 Gb	9 Gb	8 Gb	12 Gb	
Prefetch Size per PC (bits)	256	256	256	256	256	256	
Row Address	RA[13:0]	RA[13:0]	RA[14:0] ⁹	RA[14:0] ⁹	RA[14:0]	RA[14:0]	
Column Address	CA[5:1]	CA[5:1]	CA[5:1]	CA[5:1]	CA[5:1]	CA[5:1]	
Bank Address	SID, BA[3:0]	SID[1:0], BA[3:0] ¹⁰	SID, BA[3:0]	SID[1:0], BA[3:0] ¹⁰	SID, BA[3:0]	SID[1:0], BA[3:0] ¹⁰	
Page Size per PC	1 KB	1 KB	1 KB	1 KB	1 KB	1 KB	
Refresh	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	
Refresh Period	3.9 us	3.9 us	3.9 us	3.9 us	3.9 us	3.9 us	
Density Code	0100	1001	1000	1011	1010	1100	

Table 4 — HBM Channel Addressing (cont'd)

NOTE 1	Prefetch size and page size reflect the effective addressing along with row and column commands. Both do not include the optional ECC bits as described in 6.2.2.
NOTE 2	The burst order of a BL2 burst is fixed for Reads and Writes, and the HBM device does not assign a column address bit to distinguish between the first and second UI of a BL2 burst. A memory controller may internally assign such a column address bit but that column address bit is not transmitted to the HBM device. BL2 bursts are supported in legacy mode only.
NOTE 3	The burst order of a BL4 burst in PC mode is fixed for Reads and Writes, and the HBM device does not assign column address bits to distinguish between the four UI of a BL4 burst. A memory controller may internally assign such column address bits but those column address bits are not transmitted to the HBM device. PC mode requires that the burst length is set to 4 (BL4) in MR3 OP7.
NOTE 4	Page Size = $2^{\text{COLBITS}} \times (\text{Prefetch Size} / 8)$; where COLBITS is the number of column address bits. Page size and prefetch size are per channel in legacy mode, and per pseudo channel in PC mode.
NOTE 5	In PC mode, an additional address bit BA4 is provided for row and column commands to direct commands either to pseudo channel 0 (BA4 = 0) or pseudo channel 1 (BA4 = 1). See Table 30 and Table 31.
NOTE 6	The HBM device indicates the support of legacy mode and/or PC mode in bits [17:16] of the .
NOTE 7	These configurations are optimized for HBM stacks using 8 or 12 DRAM dies. The stack height of all other configuration is vendor specific.
NOTE 8	SID, SID0, SID1 act as bank address bits in command execution. Specific AC timing parameters or variations on selected timing parameters may be linked to SID. Table 30 and Table 31 and the vendor datasheets should be consulted for details.
NOTE 9	RA[14:13] = 11 is invalid.
NOTE 10	SID[1:0] = 11 is invalid.
NOTE 11	The density code refers to the encoding of the per-channel density in the , bits [79:76].

3.2.1 Bank Groups

The activity within a bank group must be restricted to ensure proper operation of the device for HBM DRAMs operating at frequencies above a certain threshold f_{CKBG} . The banks within a device are divided into four or eight bank groups. The bank group feature is configurable via MRS. The assignment of banks to bank groups is shown in Table 5.

Different timing parameters are specified depending on whether back-to-back accesses are within the same bank group or across bank groups as shown in Table 6.

3.2.1 Bank Groups (cont'd)

Table 5 — Bank Group Assignments

Banks	8 Banks BA[2:0]	16 Banks BA[3:0]	32 Banks SID, BA[3:0]	48 Banks SID[1:0], BA[3:0]
0 and 1	Group A	Group A	Group A	Group A
2 and 3	Group B			
4 and 5	Group C	Group B	Group B	Group B
6 and 7	Group D			
8 to 11	N/A	Group C	Group C	Group C
12 to 15		Group D	Group D	Group D
16 to 19		N/A	Group E	Group E
20 to 23			Group F	Group F
24 to 27			Group G	Group G
28 to 31			Group H	Group H
32 to 35			N/A	Group I
36 to 39				Group J
40 to 43				Group K
44 to 47				Group L

Table 6 — Command Sequences Affected by Bank Groups

Command Sequence	Corresponding AC Timing Parameter			Notes
	Bank Groups Disabled	Bank Groups Enabled		
		Accesses to different bank groups	Accesses within the same bank group	
ACTIVATE to ACTIVATE	t _{RRDS}	t _{RRDS}	t _{RRDL}	
WRITE to WRITE	t _{CCDS}	t _{CCDS}	t _{CCDL}	
READ to READ	t _{CCDS}	t _{CCDS} or t _{CCDR}	t _{CCDL}	
Internal WRITE to READ	t _{WTRS}	t _{WTRS}	t _{WTRL}	
READ to PRECHARGE	t _{RTPS}	—	t _{RTPL}	1
NOTE 1	Parameters t _{RTPS} and t _{RTPL} apply only when READ and PRECHARGE go to the same bank; use t _{RTPS} when Bank Groups are disabled, and t _{RTPL} when Bank Groups are enabled.			
NOTE 2	Parameters t _{CCDR} replaces parameter t _{CCDS} when consecutive READs go to banks with different stack IDs (SID).			

4 Initialization

To power-up and initialize the HBM device into functional operation the sequence in Section 4.1 must be followed. At any time after the power-up initialization, the HBM device may be reset using the sequence in Section 4.2. A limited set of IEEE 1500 port instructions may be used within the initialization sequences, as described in Section 4.3.

The interactions between HBM functional reset and the IEEE 1500 port reset are as follows (also see Section 13):

- Functional reset requires that the IEEE 1500 port also be reset.
- The IEEE 1500 port can be reset at any time without impacting normal operation.
- The IEEE 1500 port may be brought out of reset and a limited set of instructions may be used after a minimum time after RESET_n has been deasserted. See section 4.3.
- If not needed, the IEEE 1500 port may be left in reset (WRST_n = LOW) during normal operation.

4.1 HBM Power-up and Initialization Sequence

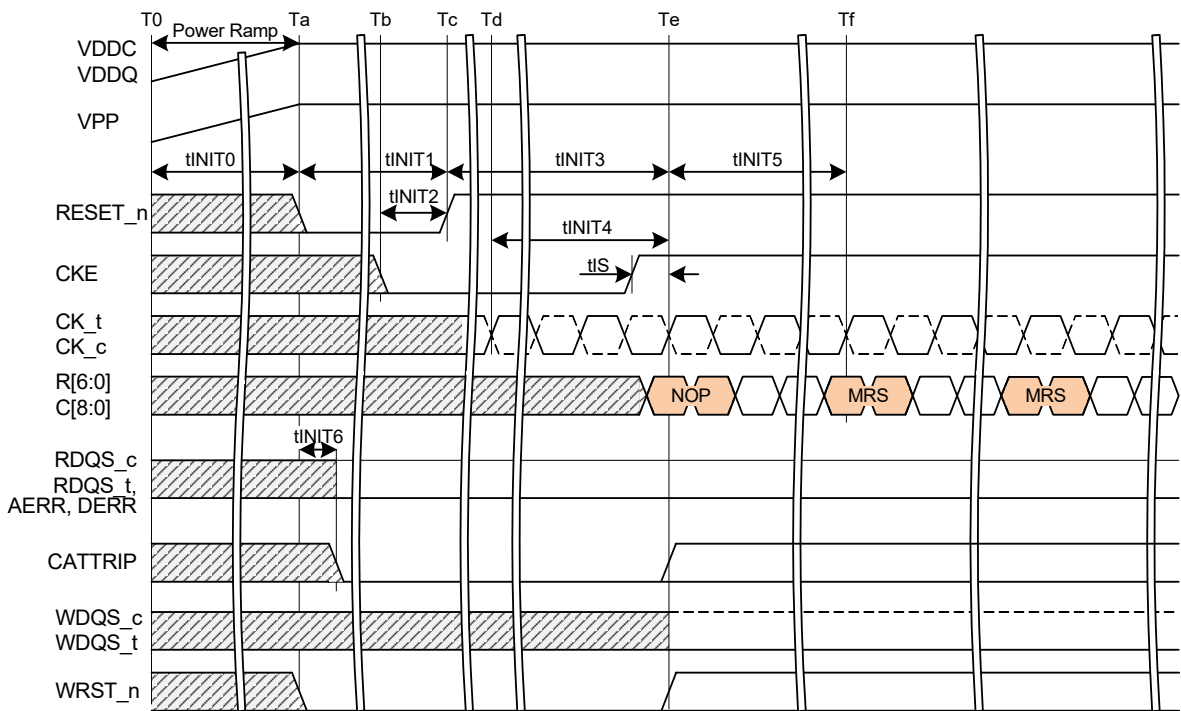
HBM device must be powered up and initialized in a predefined manner. The following sequence and timing must be satisfied for HBM power up and initialization sequence. Also refer to Figure 4.

1. Apply power to the V_{DDC} , V_{DDQ} and V_{PP} supplies. The V_{DDC} supply must be applied before or at the same time as V_{DDQ} . The power supply ramp time between 300 mV and V_{DDC} must be less than or equal to t_{INIT0} . During the power ramp, $V_{DDC} \geq V_{DDQ}$ and $(V_{DDC} - V_{DDQ}) < 0.3$ V. The V_{PP} supply must be applied before or at the same time as V_{DDC} and must be equal to or higher than V_{DDC} at all times. During power supply ramp time t_{INIT0} , RESET_n, WRST_n and all other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z).
2. RESET_n must be driven LOW (below $0.2 \times V_{DDQ}$) before or at the same time when t_{INIT0} expires as shown in Figure 4 (time Ta). WRST_n must be driven LOW before or at the same time as RESET_n. All other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z) at this point. RESET_n must be maintained LOW for a minimum of t_{INIT1} time with stable power. After t_{INIT6} time has elapsed, the HBM device drives RDQS_t and RDQS_c to LOW and HIGH static levels, respectively, and AERR and DERR signals LOW. CKE must be driven LOW a minimum of t_{INIT2} time before RESET_n is driven HIGH.
3. After RESET_n is driven HIGH, CKE must remain LOW for a minimum time of t_{INIT3} . The HBM device resets into the precharged power-down state. During t_{INIT3} , the HBM device will read and apply internal fuse configuration data and perform I/O driver impedance calibration. At the same time the WRST_n signal may be optionally driven HIGH to enable a subset of the IEEE 1500 instructions (see [Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs](#) and [IEEE Standard 1500](#) sections). CATTRIP data must stay LOW from the end of t_{INIT6} to the end of t_{INIT3} and valid data must start after t_{INIT3} .
4. The CK clock shall be started, and stable clocks shall be maintained for minimum of t_{INIT4} time before driving CKE HIGH. Since CKE is a synchronous signal, the corresponding setup time to clock (t_{IS}) must be met. Also, RNOP and CNOP commands must be registered (with t_{IS} / t_{IH} satisfied). After CKE is registered HIGH, a minimum t_{INIT5} time must be satisfied before issuing a first MRS command. At or before the time that CKE is driven HIGH, WDQS_t and WDQS_c must be driven to LOW and HIGH static levels, respectively.
5. Issue all MRS commands to configure the HBM device appropriately for the application setting.
6. The HBM device is now ready for normal operation.

4.1 HBM Power-up and Initialization Sequence (cont'd)

Table 7 — Initialization Timing Parameters

Symbol	Description	Min	Max	Unit
t_{INIT0}	Power supply ramp time	0.01	200	ms
t_{INIT1}	RESET_n signal LOW time at power-up (after stable power)	200	–	us
t_{INIT2}	CKE LOW time before RESET_n deassertion	10	–	ns
t_{INIT3}	CKE and WRST_n LOW time after RESET_n deassertion	500	–	us
t_{INIT4}	Stable clock before CKE HIGH	10	–	nCK
t_{INIT5}	Idle time before first MRS command	200	–	ns
t_{INIT6}	RDQS_t, RDQS_c driven valid and AERR, DERR driven LOW after RESET_n assertion	–	100	ns
$t_{\text{PW_RESET}}$	RESET_n signal LOW time with stable power	1	–	us



1. CATTRIP is valid after t_{INIT3} .

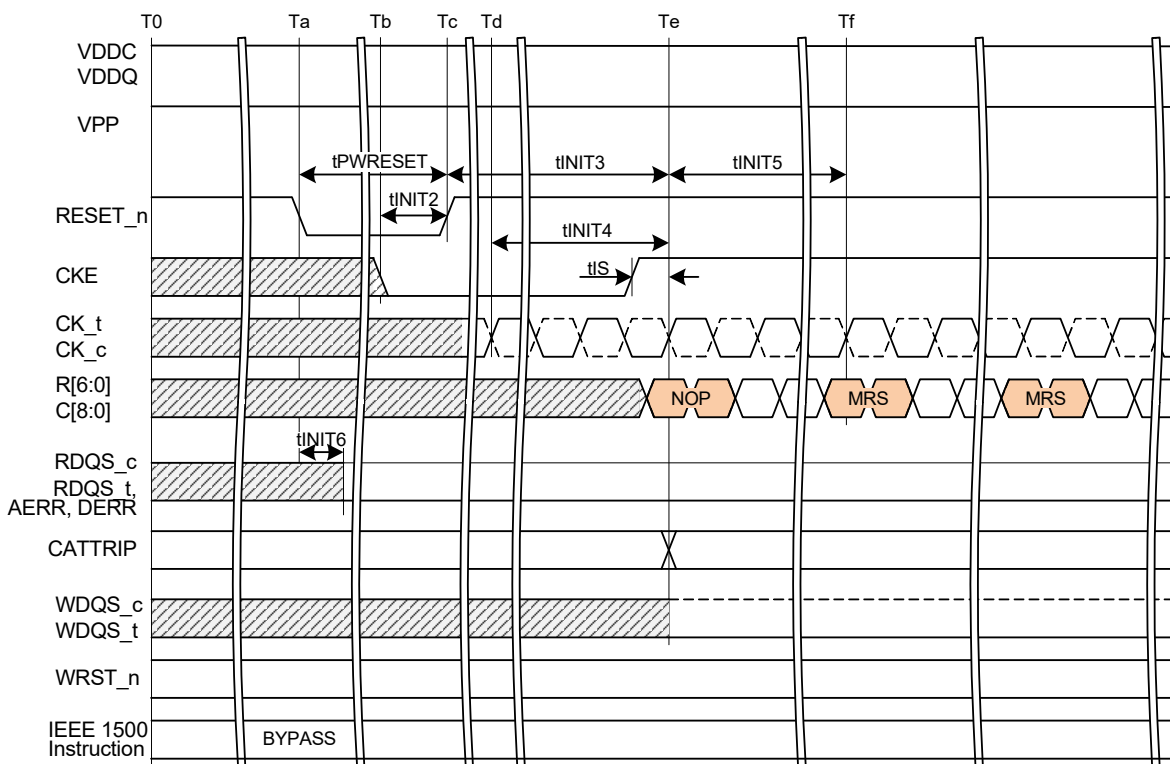
Don't Care

Figure 4 — Power-up and Initialization

4.2 Initialization Sequence with Stable Power

The following sequence must be satisfied to perform a functional reset when power is kept stable at the HBM DRAM. See [Figure 5](#).

1. RESET_n must be driven LOW anytime when a functional reset is needed. WRST_n must be driven LOW before or at the same time as RESET_n. All other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z) at this point. RESET_n must be maintained LOW for a minimum of t_{PW_RESET} . CKE must be driven LOW a minimum of t_{INIT2} time before RESET_n is driven HIGH. Alternately, the IEEE 1500 port HBM_RESET instruction may be used to perform a re-initialization, with RESET_n continuing to be driven HIGH. Refer to [HBM_RESET](#) section.
2. Follow steps 3 to 6 as described in section [HBM Power-up and Initialization Sequence](#). Note that the CATTRIP output is sticky and not cleared by a functional reset.



1. CATTRIP will maintain value as the one before reset until end of t_{INIT3} .

Don't Care

Figure 5 — HBM RESET and Initialization Sequence with Stable Power

4.3 Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs

All IEEE 1500 port instructions are allowed after t_{INIT3} without completing the full initialization sequence.

Figure 6 illustrates usage of the EXTEST and SOFT_LANE_REPAIR instructions within the initialization sequence. This sequence may be applied as part of the power-up or stable-power initialization sequences to check for and correct failed connections on the row and column command buses, which must be correctly driven to RNOP and CNOP as part of the above initialization sequences. DWORD lane repairs are also allowed.

1. At time T_a , RESET_n and WRST_n must be driven LOW.
2. After a minimum time t_{INIT1} (if during an initial power-up sequence) or after $t_{\text{PW_RESET}}$ (if during a stable power initialization sequence) RESET_n shall be driven HIGH. t_{INIT2} must also be met.
3. After t_{INIT3} , WRST_n is driven HIGH. IEEE 1500 port instructions may now be used. (Note that the WRST_n low pulse width t_{WRSTL} is met since t_{WRSTL} is less than the t_{INIT1} or $t_{\text{PW_RESET}}$). Refer to [IEEE1500 Port AC Timing Parameters](#) for timing requirements for operating the IEEE 1500 port, including t_{SWRST} . At this point, defective lane detection and soft lane repair may be executed. EXTEST operations may be applied to identify lanes needing repair. If soft lane repair is needed, SOFT_LANE_REPAIR operations can be applied after another RESET_n toggle, which is required after EXTEST instruction operation. A IEEE 1500 port BYPASS instruction should be applied to return all HBM signals to their normal functional mode after SOFT_LANE_REPAIR operations. Alternately, WRST_n may be driven LOW.
4. The initialization sequence may then continue per steps 4 to 6 of [HBM Power-up and Initialization Sequence](#), as needed.

During the t_{INIT3} period before WRST_n is driven HIGH, the HBM device executes various internal configuration operations, including applying hard lane repairs based on previously fused data. Executing soft lane repair instructions after t_{INIT3} overwrites any previously programmed hard lane repair data. It is suggested that the hard lane repair data is read from the HBM device and merged in any new lane repairs before applying the new soft lane repair operations. Any applicable IEEE 1500 port instructions timings must be met before continuing to time point T_h , such as t_{SLREP} if a SOFT_LANE_REPAIR instruction has been applied.

The EXTEST instructions are not required before applying the soft lane repair(s). Previously determined needed lane repairs may be applied as part of each initialization event.

4.3 Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs (Cont'd)

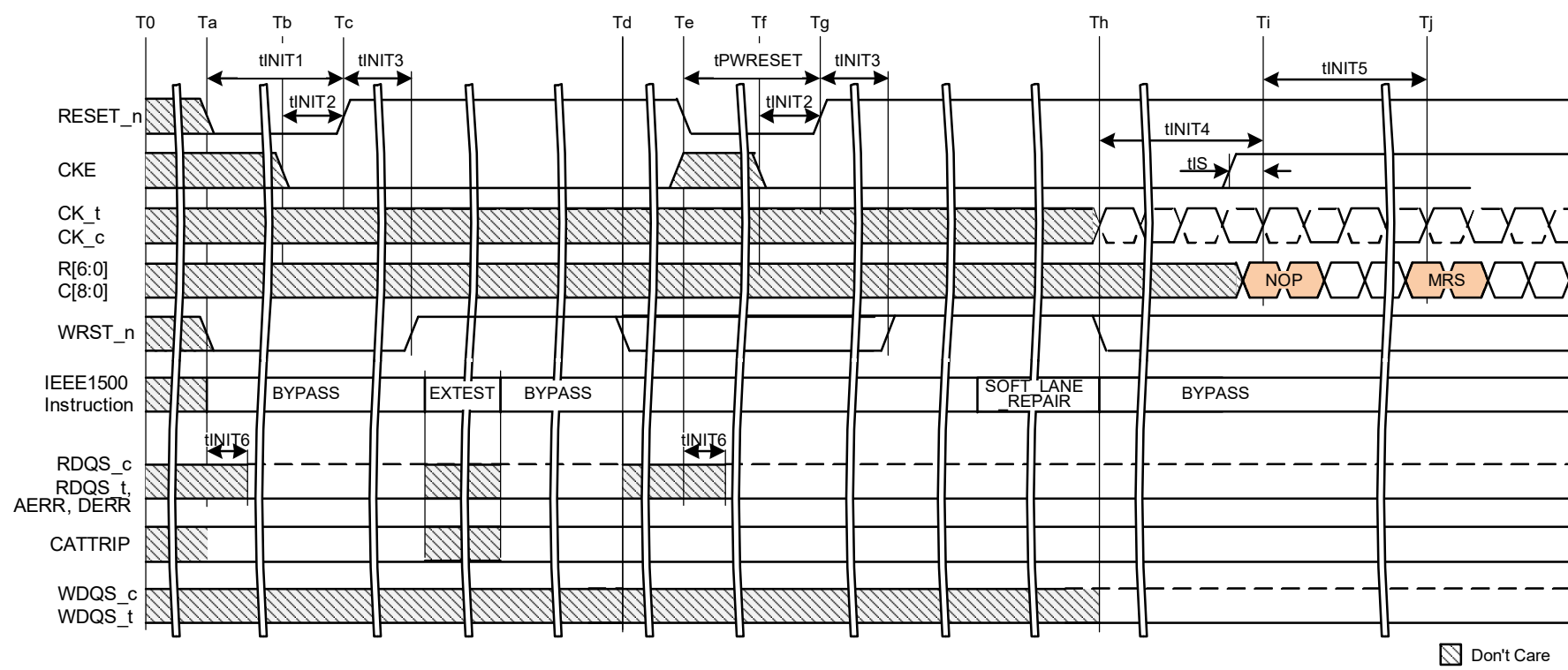


Figure 6 — Initialization Sequence with Lane Repairs

5 Mode Registers

The mode registers define the specific mode of operation for the HBM device. MR0 to MR8 and MR15 are defined as shown in Figure 1. MR9 to MR14 are reserved. Reprogramming the mode registers does not alter the contents of the memory array.

All mode registers are programmed via the [Mode Register Set \(MRS\)](#) command and retain the stored information until they are reprogrammed, chip reset, or until the device loses power. Mode registers must be loaded when all banks are idle and no bursts are in progress; the controller must wait the specified time t_{MOD} before initiating any subsequent operations. Violating either of these requirements results in unspecified operation.

No default states are defined for mode registers except when otherwise noted. Users therefore must fully initialize all mode registers to the desired values upon power-up.

Reserved bits must be programmed to 0.

Table 8 — HBM Mode Register Overview

Mode Register		OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
	BA[3:0]								
MR0 (Table 9)	0000	Test Mode	ADD/CMD Parity	DQ Write Parity	DQ Read Parity	Reserved	TCSR	DBIac Write	DBIac Read
MR1 (Table 10)	0001	Driver Strength			Write Recovery (WR)				
MR2 (Table 11)	0010	Read Latency (RL)					Write Latency (WL)		
MR3 (Table 12)	0011	BL	Bank Group	Active to Precharge (RAS)					
MR4 (Table 15)	0100	Reserved		Extended Read Latency (ERL)	Extended Write Latency (EWL)	Parity Latency (PL)		Write Data Mask (DM) and ECC	
MR5 (Table 16)	0101	TRR	TRR - PS Select	Reserved		TRR Mode BAn			
MR6 (Table 17)	0110	imPRE t _{RP} Value					Reserved		
MR7 (Table 18)	0111	CATTRIP	Reserved	MISR Control			Read Mux Control		Loopback
MR8 (Table 19)	1000	Reserved							DA28 Lockout
MR9	1001	Reserved							
MR10	1010	Reserved							
MR11	1011	Reserved							
MR12	1100	Reserved							
MR13	1101	Reserved							
MR14	1110	Reserved							
MR15 (Table 26)	1111	Reserved					Optional Internal Vref (applies to DQ and ADD/CMD bus)		

5 Mode Registers (cont'd)**Table 9 — Mode Register 0 (MR0)**

Field	Bits	Description	Notes
Test Mode	OP7	0 - Normal operation (default) 1 - Test mode (vendor specific)	
Address, Command Bus Parity for Row, Column Bus	OP6	0 - Disable (default) 1 - Enable	
DQ Bus Write Parity	OP5	0 - Disable (default) 1 - Enable	
DQ Bus Read Parity	OP4	0 - Disable (default) 1 - Enable	
Reserved	OP3	0	
Temperature Compensated Self Refresh (TCSR)	OP2	0 - Disable 1 - Enable (default)	
Write DBIac	OP1	0 - Disable 1 - Enable (default)	
Read DBIac	OP0	0 - Disable 1 - Enable (default)	

Table 10 — Mode Register 1 (MR1)

Field	Bits	Description	Notes
Nominal Driver Strength	OP[7:5]	000 - 6 mA driver (default) 001 - 9 mA driver 010 - 12 mA driver 011 - 15 mA driver 100 - 18 mA driver All other encoding are reserved	1
Write Recovery (WR) (for Auto-Precharge only)	OP[4:0]	00000 - Reserved 00001 - Reserved 00010 - Reserved 00011 - 3 nCK 00100 - 4 nCK 00101 - 5 nCK 00110 - 6 nCK 00111 - 7 nCK 01000 - 8 nCK ... 11111 - 31 nCK	2
NOTE 1 18mA driver encoding is not needed until higher speed operation such as 2 Gbps. NOTE 2 HBM device is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous.			

5 Mode Registers (cont'd)

Table 11 — Mode Register 2 (MR2)

Field	Bits	Description	Bits	Description	Notes
Read Latency (RL)	OP[7:3] MR4 OP5 = 0	00000 - Reserved 00001 - 3 nCK (minimum) 00010 - 4 nCK 00011 - 5 nCK 00100 - 6 nCK 00101 - 7 nCK 00110 - 8 nCK 00111 - 9 nCK ... 11111 - 33 nCK	OP[7:3] MR4 OP5 = 1	00000 - 34 nCK 00001 - 35 nCK 00010 - 36 nCK 00011 - 37 nCK ... 01101 - 47 nCK 01110 - 48 nCK 01111 - Reserved ... 11111 - Reserved	1
Write Latency (WL)	OP[2:0] MR4 OP4 = 0	000 - 1 nCK (minimum) 001 - 2 nCK 010 - 3 nCK 011 - 4 nCK 100 - 5 nCK 101 - 6 nCK 110 - 7 nCK 111 - 8 nCK	OP[2:0] MR4 OP4 = 1	000 - 9 nCK 001 - 10 nCK 010 - 11 nCK 011 - 12 nCK 100 - 13 nCK 101 - 14 nCK 110 - 15 nCK 111 - 16 nCK	1
NOTE 1 HBM device is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous.					

Table 12 — Mode Register 3 (MR3)

Field	Bits	Description	Notes
Burst Length (BL)	OP7	0 - BL2 1 - BL4	2
Bank Group	OP6	0 - Disable 1 - Enable (default)	
Activate to Precharge RAS	OP[5:0]	000000 - Reserved 000001 - Reserved 000010 - Reserved 000011 - 3 nCK 000100 - 4 nCK 000101 - 5 nCK 000110 - 6 nCK 000111 - 7 nCK 001000 - 8 nCK ... 111111 - 63 nCK	1

NOTE 1 HBM device is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous.

NOTE 2 In pseudo channel mode, BL must be set to 4.

5 Mode Registers (cont'd)

Table 13 — MR3 - Burst Type and Burst Order Definition - BL2

Burst Type	Burst Length	Read/Write	Burst Order
Sequential	2	Read	0, 1
		Write	0, 1

Table 14 — MR3 - Burst Type and Burst Order Definition - BL4

Burst Type	Burst Length	Read/Write	Starting Column Address CA0	Burst Order	Notes
Sequential	4	Read	0	0, 1, 2, 3	1,2
			1	2, 3, 0, 1	1,2
		Write	0	0, 1, 2, 3	1,2
			1	2, 3, 0, 1	1,2
NOTE 1	Reads and Write are treated as two consecutive access with BL=2.				
NOTE 2	Burst re-order via address bit CA0 is supported in legacy mode only. The burst order is fixed in pseudo channel mode and address bit CA0 is not defined.				

Table 15 — Mode Register 4 (MR4)

Field	Bits	Description	Notes
Reserved	OP[7:6]	0x00	
Extended Read Latency (ERL)	OP5	see Table 11	
Extended Write Latency (EWL)	OP4	see Table 11	
Parity Latency (PL)	OP[3:2]	00 - 0 nCK 01 - 1 nCK 10 - 2 nCK 11 - 3 nCK	
Write Data Mask (DM) and ECC	OP[1:0]	00 - Enable DM, disable ECC 01 - Reserved (DM and ECC cannot be enabled simultaneously) 10 - Disable DM, disable ECC 11 - Disable DM, enable ECC	

5 Mode Registers (cont'd)

Table 16 — Mode Register 5 (MR5)

Field	Bits	Description	Notes
TRR Mode	OP7	0 - Disable (default) 1 - Enable	
TRR Mode - Pseudo Channel Select	OP6	0 - Enable TRR mode for PC0 1 - Enable TRR mode for PC1	1,2
Reserved	OP[5:4]	00	
TRR Mode - Bank address	OP[3:0]	0000 - Bank 0 ... 1111 - Bank 15	
NOTE 1 Only applicable when MR5 OP7 = 1.			
NOTE 2 Only applicable when DEVICE_ID Wrapper Data Register bits [17:16] = 01.			

Table 17 — Mode Register 6 (MR6)

Field	Bits	Description	Notes
imPRE t_{RP} Value	OP[7:3]	00000 - 2nCK (Minimum) 00001 - 3 nCK 00010 - 4 nCK 00011 - 5 nCK ... 11111 - 33 nCK	1,2
Reserved	OP[2:0]	000	
NOTE 1 HBM device is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous.			
NOTE 2 imPRE is only available in pseudo channel mode. DEVICE_ID Wrapper Data Register bits [17:16] = 01.			

5 Mode Registers (cont'd)

Table 18 — Mode Register 7 (MR7)

Field	Bits	Description	Notes
CATTRIP	OP7	0 - Clear CATTRIP pin (default) 1 - Assert CATTRIP pin to “1”	1
Reserved	OP6	0	
DWORD MISR Control	OP[5:3]	Only applicable if Loopback is enabled in OP0 000 - Preset The DWORD MISR/LFSRs are set to 0xAAAAAh, and the DWORD LFSR_COMPARE_STICKY bits are set to all zeros. 001 - LFSR mode (read direction) 010 - Register mode (read and write directions) DWORD writes are captured directly into the MISR registers without compression. The MISR registers will contain the most recent write data. 011 - MISR mode (write direction) 100 - LFSR Compare mode (write direction)	2
DWORD Read Mux Control	OP[2:1]	Only applicable if Loopback is enabled in OP0 00 - Reserved 01 - Return data from MISR registers (default) 10 - Return data from Rx path sampler 11 - Return LFSR_COMPARE_STICKY (optional)	
DWORD Loopback	OP0	0 - Disable (default) 1 - Enable; enables link testing circuitry. All Writes and Reads will be to/from the MISR. (Does not require any additional Activation to Write/Reads - Column addresses are ignored in this mode.)	
NOTE 1 The CATTRIP pin can be asserted to “1” from any of the channels [a:h] MR7 OP7 bit (logic OR).			
NOTE 2 See HBM Loopback Test Modes for DWORD MISR mode features and usage.			

Table 19 — Mode Register 8 (MR8)

Field	Bits	Description	Notes
Reserved	OP[7:1]	0x00	
DA28 lockout	OP0	0 - Disable (default) 1 - Enable (see DA28 Lockout)	1
NOTE 1 DA28 lockout is defined for channels a and e only. Once enabled, the DA28 lockout can only be cleared when power is removed. The IEEE1500 MODE REGISTER_DUMP_SET instruction cannot be used to set or clear the DA28 lockout bit, but may optionally allow reading the DA28 lockout bit.			

Table 20 — Mode Register 9 (MR9)

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	



5 Mode Registers (cont'd)**Table 21 — Mode Register 10 (MR10)**

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

Table 22 — Mode Register 11 (MR11)

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

Table 23 — Mode Register 12 (MR12)

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

Table 24 — Mode Register 13 (MR13)

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

Table 25 — Mode Register 14 (MR14)

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

Table 26 — Mode Register 15 (MR15)

Field	Bits	Description	Notes
Reserved	OP[7:3]	00000	
Internal Vref	OP[2:0]	Optional HBM feature. HBM may simply ignore these bits if there is no internal Vref generator. If there is internal Vref, these bits are programmed appropriately. Applies to both DQ bus as well as Row/Column address/cmd bus. HBM has only one internal Vref generator across all 8 channels. These bits must programmed identically in all eight mode registers. 000 - $0.50 \times V_{DDQ}$ 001 - $0.46 \times V_{DDQ}$ 010 - $0.42 \times V_{DDQ}$ 011 - $0.38 \times V_{DDQ}$ 100 - $0.54 \times V_{DDQ}$ 101 - $0.58 \times V_{DDQ}$ 110 - $0.62 \times V_{DDQ}$ 111 - $0.66 \times V_{DDQ}$	

6 Operation

6.1 Clocking Overview

The HBM device captures commands and addresses on the row and column buses using a differential clock CK_t/CK_c. Both buses operate at double data rate (DDR).

The HBM device has uni-directional differential Write strobes (WDQS_t/WDQS_c) and Read strobes (RDQS_t/RDQS_c) per 32 DQ (DWORD). The data bus operates at double data rate (DDR).

The following nomenclature is being used throughout this specification:

- a rising CK (or WDQS, RDQS) edge is defined as the crossing of the positive edge of CK_t (or WDQS_t, RDQS_t) and the negative edge of CK_c (or WDQS_c, RDQS_c);
- a falling CK (or WDQS, RDQS) edge is defined as the crossing of the negative edge of CK_t (or WDQS_t, RDQS_t) and the positive edge of CK_c (or WDQS_c, RDQS_c).

6.1 Clocking Overview (Cont'd)

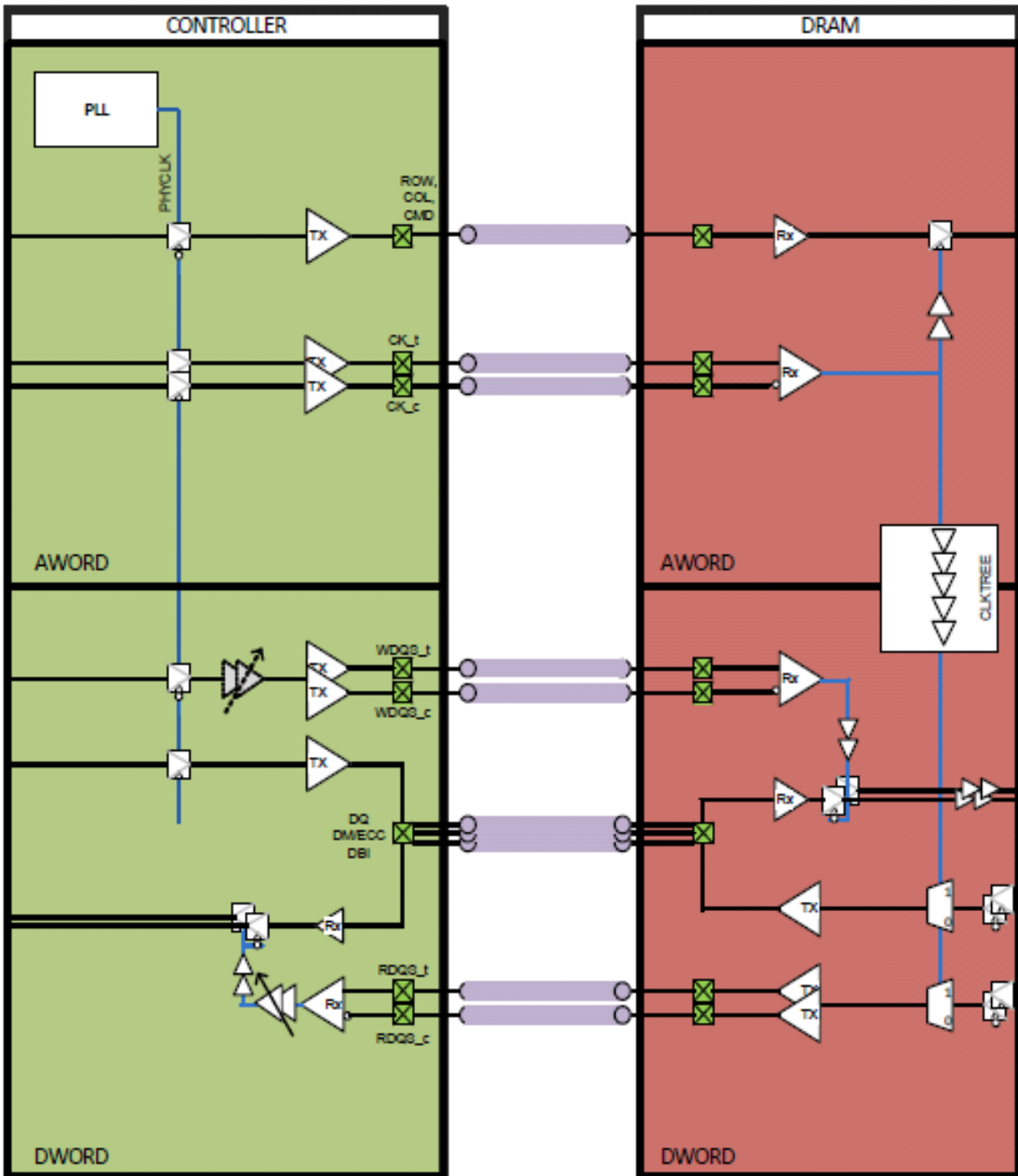


Figure 7 — High Level Block Diagram Example of Clocking Scheme

6.2 HBM Write Data Mask (DM), Data Bus Inversion (DBIac) and ECC

The HBM device supports Write Data Mask (DM), Data Bus Inversion (DBIac) and optionally ECC with byte granularity. One Data Mask (DM) pin and one Data Bus Inversion (DBI) pin per byte are provided as shown in Table 27. DBI is a bi-directional DDR pin and driven or sampled along with the DQ pins for Read and Write operation. DM is a bi-directional DDR pin and driven or sampled along with DQ signals pins for Read or Write operation when used with ECC (see below); the pin is input only and used for Write operations when used with Write Data Mask.

Table 27 — DM, DBI to DQ Correspondence and Even/Odd Byte Groups

DQ	DBI	DM	Even/Odd Byte Group
DQ[7:0]	DBI0	DM0	Even Byte
DQ[15:8]	DBI1	DM1	Odd Byte
DQ[23:16]	DBI2	DM2	Even Byte
DQ[31:24]	DBI3	DM3	Odd Byte
DQ[39:32]	DBI4	DM4	Even Byte
DQ[47:40]	DBI5	DM5	Odd Byte
DQ[55:48]	DBI6	DM6	Even Byte
DQ[63:56]	DBI7	DM7	Odd Byte
DQ[71:64]	DBI8	DM8	Even Byte
DQ[79:72]	DBI9	DM9	Odd Byte
DQ[87:80]	DBI10	DM10	Even Byte
DQ[95:88]	DBI11	DM11	Odd Byte
DQ[103:96]	DBI12	DM12	Even Byte
DQ[111:104]	DBI13	DM13	Odd Byte
DQ[119:112]	DBI14	DM14	Even Byte
DQ[127:120]	DBI15	DM15	Odd Byte

6.2.1 Write Data Mask (DM)

Write data mask (DM) function can be enabled per MR4 OP1 (see Table 15). Write data received on the DQ inputs are masked in case DM is sampled HIGH and DQ input signals are don't care (either valid HIGH or LOW); DQ input signals are valid and write data is written to the DRAM array in case DM is sampled LOW.

Please note that when DQ parity is enabled for Writes, the data inputs are included in the parity calculation regardless whether a byte is masked by DM or not.

Table 28 — Write Data Mask (DM)

Function	DM	DQ
Write Enable	LOW	Valid
Write Inhibit	HIGH	Ignored

6.2.2 Error Correction Code (ECC)

HBM DRAM devices may optionally support ECC (one bit per data byte). The HBM DRAM itself does not compute any ECC. The HBM DRAM provides the additional DRAM cells to store ECC information. ECC bits are not included in parity calculation when Write or Read DQ Parity Function is enabled (see [Table 37](#)). The ECC function can be enabled or disabled per MR4 OP0.

6.2.3 DM & ECC Function Combinations

[Table 29](#) summarizes the DM pin function as configured by MR4 OP[1:0].

Table 29 — DM Pin Function

MR4		Write Data Mask (DM)	Error Correction Code (ECC)	DM Pin Function
OP1	OP0			
0	0	Enabled	Disabled	Input only
0	1	Not allowed		Undefined
1	0	Disabled	Disabled	Hi-Z (input receivers and output drivers turned off)
1	1	Disabled	Enabled	Bi-directional

6.2.4 DBIac Function

DBIac function can be enabled or disabled independently for Write and Read operation per HBM mode register MR0 OP1 and OP0, respectively (see [Table 9](#)).

When both Write and Read DBIac function is disabled in mode register, DBI signal is a don't care for HBM device. HBM DBI input receivers and output drivers are turned off.

6.2.4.1 DBIac Enabled

HBM devices supports byte granular Data Bus Inversion during Write and Read operation. In this standard, the word DBI refers to internal state of the device unless explicitly noted as DBI signal or pin.

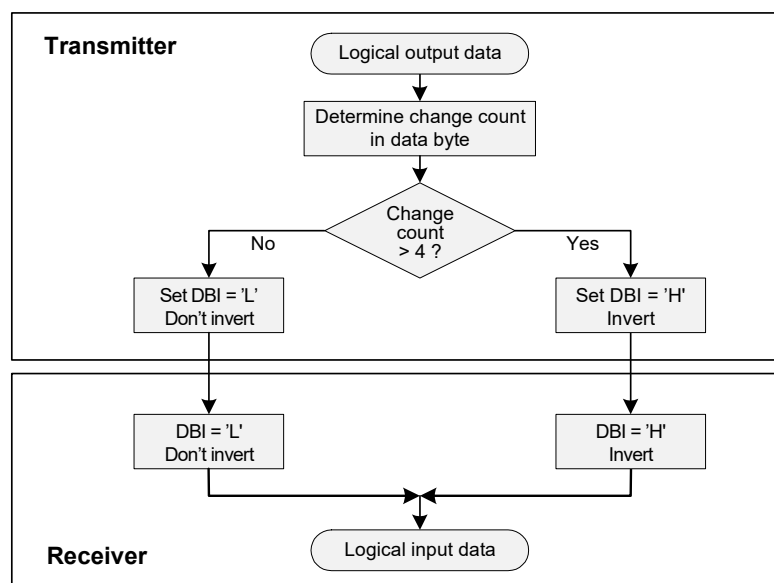


Figure 8 — DBIac Algorithm

6.2.4.1 DBIac Enabled (cont'd)

Write Operation - HBM device inverts Write data received on the DQ inputs in case DBI is sampled HIGH, or leaves the Write data non-inverted in case DBI is sampled LOW. Note that DM input is not affected by the DBIac function.

Read Operation - HBM device counts the number of DQ signals that are transitioning from previous state. Note that DM output is not affected by the DBIac function. See [Read Operation](#) under [DBIac States](#) section for bus pre-condition. The HBM device inverts Read data and sets DBI HIGH when the number of transitioning data bits within a byte is greater than 4, or when the number of transitioning data bits within a byte equals 4 and DBI was High; otherwise the HBM device does not invert the Read data and sets DBI LOW.

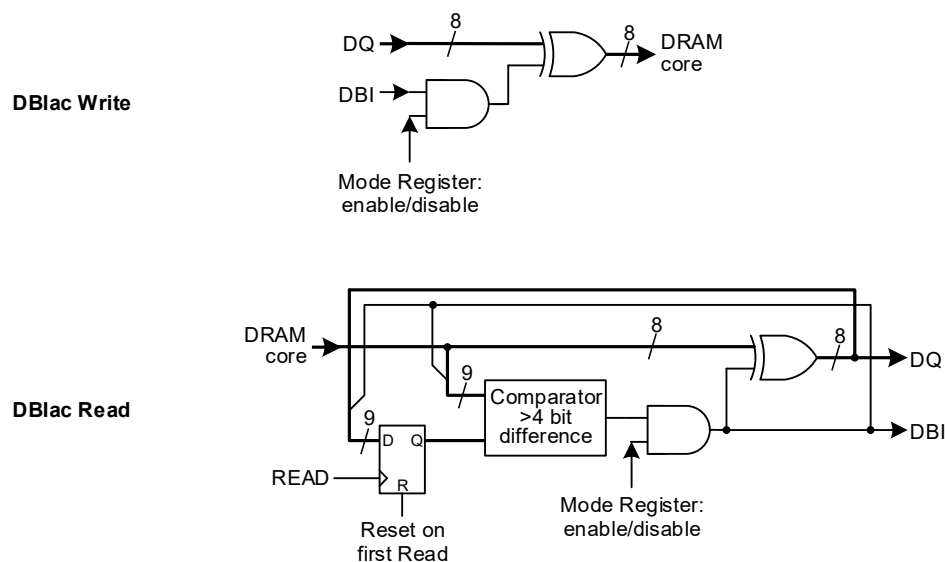


Figure 9 — Example DBIac Logic for Write and Read

6.2.5 DBIac States

The HBM device resets DBIac value to LOW (All eight DQs and DBI signals within a byte group) whenever any of the following four events occur:

- RESET_n signal de-assertion
- The HBM device registers Mode Register Set command (MRS)
- The HBM device registers Read or Read w/AP command after Write command. Note that HBM device is only required to reset DBIac value 1/2 clock prior to Read operation begins and hence it may reset DBIac value anytime before that.
- Self Refresh exit

For all other events or commands registered by the HBM, the DBIac value is not reset to LOW and the HBM device will use its previous value for DBIac calculation.

6.2.5 DBIac States (cont'd)

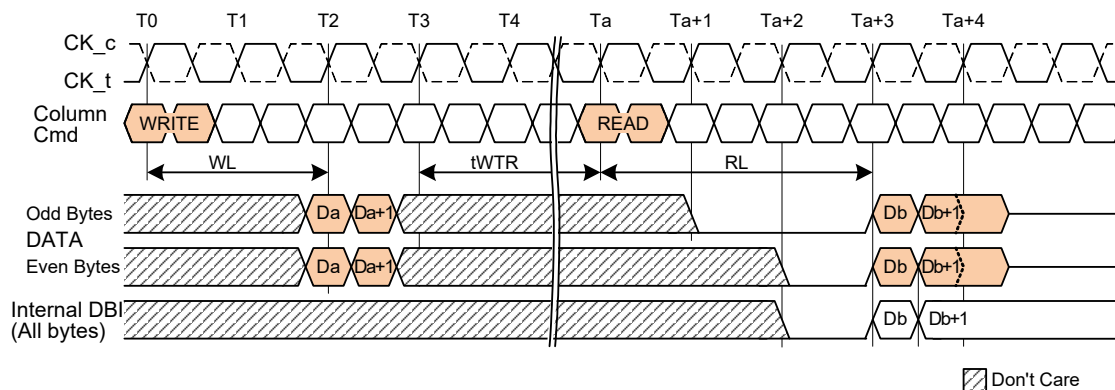


Figure 10 — Write followed by Read Timing; BL=2

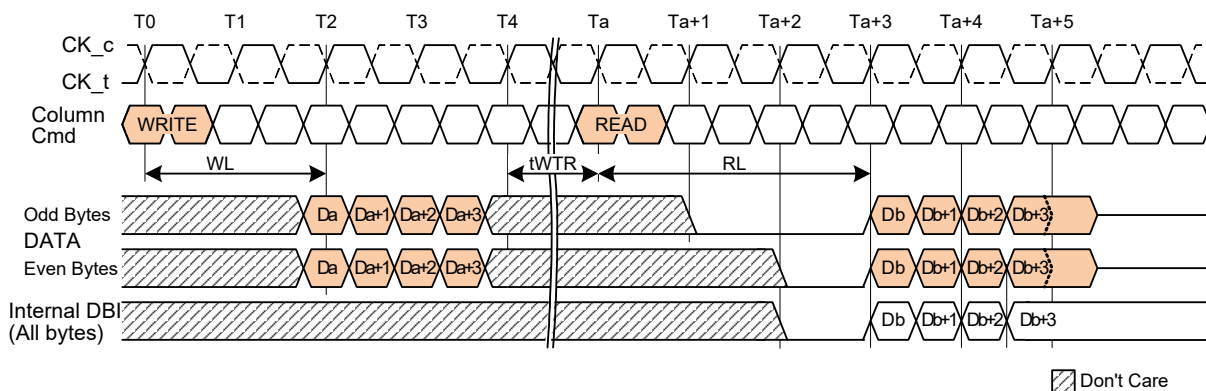


Figure 11 — Write followed by Read Timing; BL=4

6.2.5.1 Read Operation

First Read Command:

When a first Read command is registered after a DBI reset, HBM device pre-conditions the bus to LOW over $2 t_{CK}$ period prior to Read data. HBM drives odd byte signals to LOW $2 t_{CK}$ prior to Read data and even byte signals to LOW $1 t_{CK}$ prior to Read data. When DBIac function is disabled in MR, HBM device does not pre-condition the bus as described. The PAR signal is not included in the DBI calculation and therefore not preconditioned to LOW; its initial state is undefined (LOW or HIGH).

Consecutive Read Commands (Seamless and non-seamless):

Once the Read DQ burst is complete, the HBM device tri-states DBI, DM and all DQ output drivers. However, the HBM device must store the last data-out of all DQ, DM and DBI states and use that to pre-condition the bus prior to Read data and for Read DBIac calculation for any subsequent Read operation barring a condition to DBI reset. For back to back Read operation with a gap, the HBM device pre-conditions all DQ, DM and DBI to last beat of previous burst over $2 t_{CK}$ period prior to Read data. HBM drives Odd byte signals to previous state $2 t_{CK}$ prior to Read data and Even byte signals to previous state $1 t_{CK}$ prior to Read data.

6.2.5.1 Read Operation (cont'd)

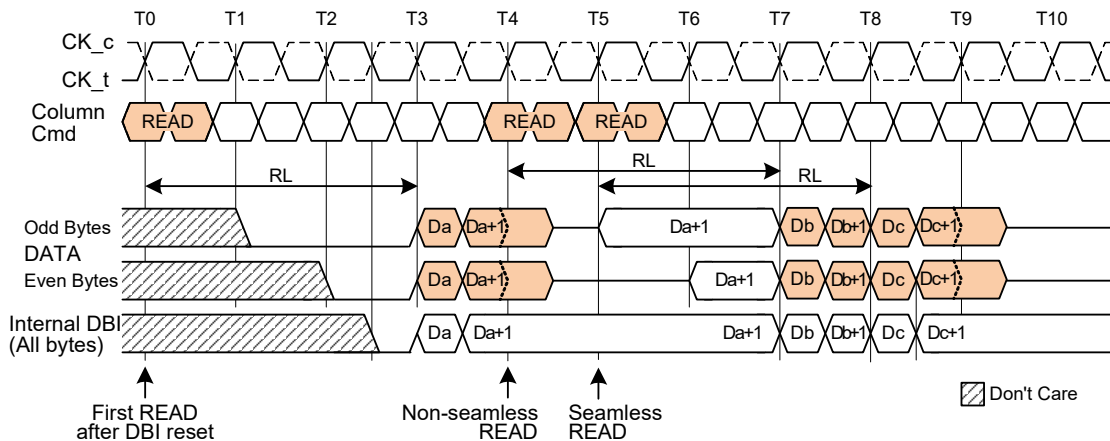


Figure 12 — Read Timing; BL=2

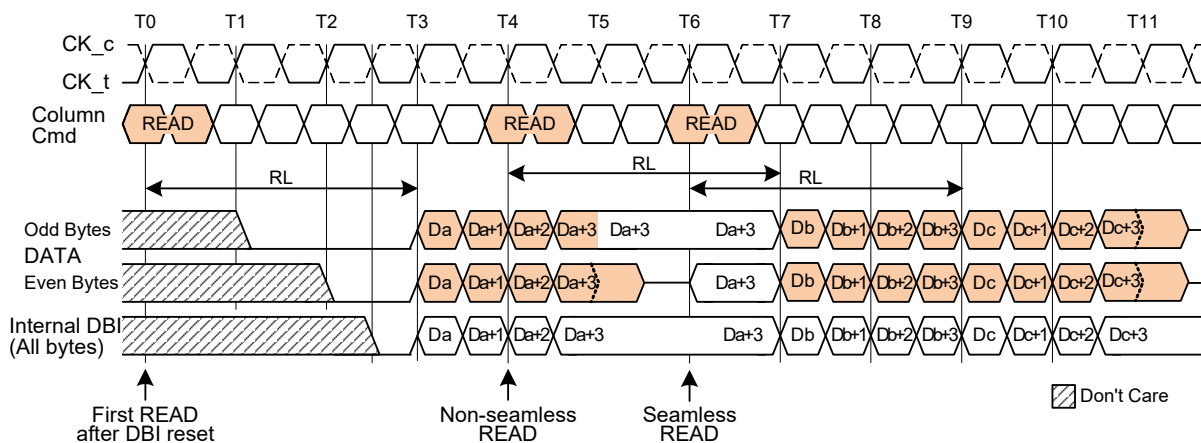


Figure 13 — Read Timing; BL=4

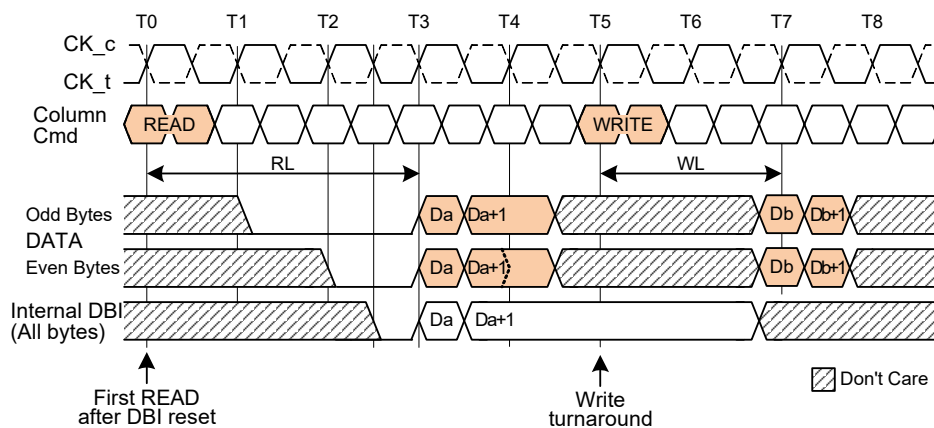


Figure 14 — Read followed by Write Timing; BL=2

6.2.5.1 Read Operation (cont'd)

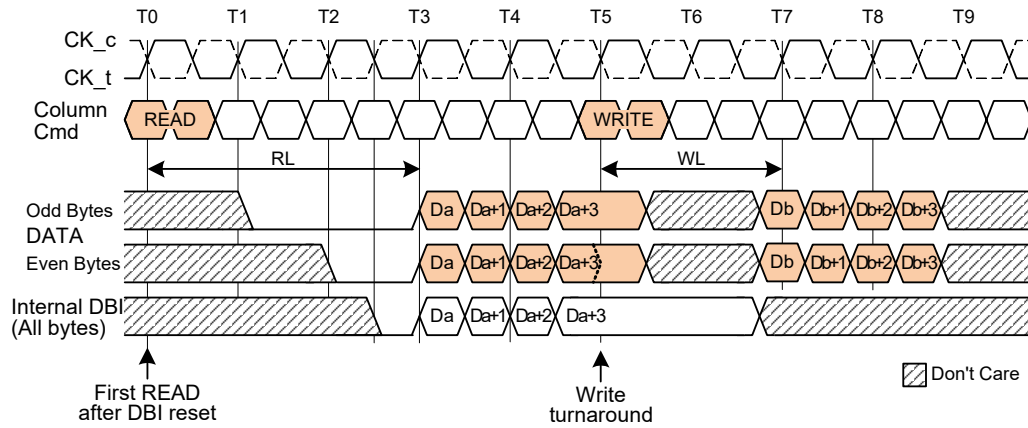


Figure 15 — Read followed by Write Timing; BL=4

6.3 Commands

The HBM DRAM features DDR commands entered on both rising and falling CK clock edges. Row Activate commands require two cycles, other row and column commands require only one cycle.

6.3.1 Command Truth Tables

Table 30 — Row Commands Truth Table

FUNCTION	SYMBOL	CLOCK CYCLE	CKE		R0	R1	R2	R3	R4	R5	R6 ¹¹	NOTES
			(N-1)	(N)								
Row No Operation	RNOP	Rising	H	H	H	H	H	V	V	V	V	1,4,7
		Falling			V	V	PAR	V	V	V	V	
Activate	ACT	Rising	H	H	L	H	V/SID/ SID0	BA0	BA1	BA2	RA14	1,2,3,4, 7,8,9, 10
		Falling			RA11	RA12	PAR	BA4	RA13	BA3	V/SID1	
		Rising			RA5	RA6	RA7	RA8	RA9	RA10	V	
		Falling			RA0	RA1	PAR	RA2	RA3	RA4	V	
Precharge	PRE	Rising	H	H	H	H	L	BA0	BA1	BA2	V/SID1	1,3,4,7, 8,9
		Falling			V	V/SID/ SID0	PAR	BA4	L	BA3	V	
Precharge All	PREA	Rising	H	H	H	H	L	V	V	V	V	1,4,7,8
		Falling			V	V	PAR	BA4	H	V	V	
Single Bank Refresh	REFSB	Rising	H	H	L	L	H	BA0	BA1	BA2	V/SID1	1,3,4,7, 8,9
		Falling			V	V/SID/ SID0	PAR	BA4	L	BA3	V	
Refresh	REF	Rising	H	H	L	L	H	V	V	V	V	1,4,7,8
		Falling			V	V	PAR	BA4	H	V	V	
Power-Down Entry	PDE	Rising	H	L	H	H	H	V	V	V	V	1,4,6,7
		Falling			V	V	PAR	V	V	V	V	
Self Refresh Entry	SRE	Rising	H	L	L	L	H	V	V	V	V	1,4,6,7
		Falling			V	V	PAR	V	V	V	V	
Power-Down & Self Refresh Exit	PDX/ SRX	Rising	L	H	H	H	H	V	V	V	V	1,5,6,7
		Falling			V	V	V	V	V	V	V	
NOTE 1 BA = Bank Address; SID = Stack ID; PAR = Parity Signal; V = Valid Signal (either H or L, but not floating).												
NOTE 2 The unused upper row address bits RA13 and RA14 must be driven to valid signal level depending on the DRAM density; they are evaluated in the parity calculation if the parity function is enabled in the mode register.												
NOTE 3 For 8 bank device, BA3 must be driven to valid signal level; it is evaluated in the parity calculation if the parity function is enabled in the mode register.												
NOTE 4 PAR signal must be driven to valid signal level even if parity function is disabled in DRAM mode register.												
NOTE 5 No Parity checking at Power-Down Exit or Self Refresh Exit command. The HBM device requires RNOP and CNOP commands on Row and Column bus respectively with valid parity if enabled during power-down exit period (t _{XP}) and self refresh exit period (t _{XS}).												
NOTE 6 CKE is a single data rate input and CKE transition from HIGH to LOW or LOW to HIGH is evaluated only with the rising clock edge. Refer to the CKE Truth Table for more details with CKE transitions.												
NOTE 7 All other command encoding not shown in the table for pins R[4,2:0] at the rising clock edge are reserved commands for future use.												
NOTE 8 BA4 applies to only pseudo channel (PC) mode. BA4 = 0 means PC0; BA4 = 1 means PC1. See section Legacy Mode and Pseudo Channel Mode for a detailed explanation of PC mode operation and timing. The pseudo channel not selected by BA4 performs a RNOP.												
NOTE 9 The SID bits act as bank address bits in conjunction with ACT, PRE and REFSB commands, and related timing diagrams shall be interpreted accordingly. PREA and REF commands do not use SID. Input R2 (ACT) or input R1 (PRE, REFSB) is SID for 8-High configurations, and SID0 for 12-High configurations. Input R6 is SID1 for 12-High configurations. The bits are V for all other configurations.												

Table 30 — Row Commands Truth Table (cont'd)

FUNCTION	SYMBOL	CLOCK CYCLE	CKE		R0	R1	R2	R3	R4	R5	R6 ¹¹	NOTES
			(N-1)	(N)								
NOTE 10	Timing parameter t _{FAW} may have two values depending on whether related commands refer to the same or a different SID. Vendor datasheets should be checked for details.											
NOTE 11	Input R6 is only present with HBM2 configurations whose addressing includes the RA14 or SID1 address bit or both (see Table 4). If input R6 is present, input C8 for the column commands (see Table 31) is present as well.											

Table 31 — Column Commands Truth Table

FUNCTION	SYMBOL	CLOCK CYCLE	CKE		C0	C1	C2	C3	C4	C5	C6	C7	C8 ¹⁰	NOTES
			(N-1)	(N)										
Column No Operation	CNOP	Rising	H	H	H	H	H	V	V	V	V	V	V	1,4,5,6
		Falling			V	V	PAR	V	V	V	V	V	V	
Read	RD	Rising	H	H	H	L	H	L	BA0	BA1	BA2	BA3	V/SID1	1,2,3,4,5,6,7,8,9
		Falling			CA0/V/SID/SID0	CA1	PAR	CA2	CA3	CA4	CA5	V/BA4	V	
Read w/ AP	RDA	Rising	H	H	H	L	H	H	BA0	BA1	BA2	BA3	V/SID1	1,2,3,4,5,6,7,8,9
		Falling			CA0/V/SID/SID0	CA1	PAR	CA2	CA3	CA4	CA5	V/BA4	V	
Write	WR	Rising	H	H	H	L	L	L	BA0	BA1	BA2	BA3	V/SID1	1,2,3,4,5,6,7,8
		Falling			CA0/V/SID/SID0	CA1	PAR	CA2	CA3	CA4	CA5	V/BA4	V	
Write w/ AP	WRA	Rising	H	H	H	L	L	H	BA0	BA1	BA2	BA3	V/SID1	1,2,3,4,5,6,7,8
		Falling			CA0/V/SID/SID0	CA1	PAR	CA2	CA3	CA4	CA5	V/BA4	V	
Mode Register Set	MRS	Rising	H	H	L	L	L	OP7	BA0	BA1	BA2	BA3	V	1,2,4,5,6
		Falling			OP0	OP1	PAR	OP2	OP3	OP4	OP5	OP6	V	

NOTE 1 BA = Bank Address; SID = Stack ID; PAR = Parity Signal; V = Valid Signal (either H or L, but not floating).

NOTE 2 CA0 is defined for legacy mode only. In pseudo channel mode the pin is either SID or ignored (V), depending on density.

NOTE 3 All pins must be driven to a valid signal level even if an address (SID, BA4, BA3, CA0) is not defined for a specific density, or if parity is disabled in the mode register.

NOTE 4 Parity is evaluated on all pins if the parity function is enabled in the mode register.

NOTE 5 CKE transition from HIGH to LOW or LOW to HIGH must be accompanied with a Column No Operation (CNOP) command. Refer to CKE Truth Table for more details with CKE transitions.

NOTE 6 All other command encodings not shown in the table for pins C[3:0] at the rising clock edge are reserved commands for future use.

NOTE 7 BA4 applies to only pseudo channel (PC) mode. BA4 = 0 means PC0; BA4 = 1 means PC1. See Section [Legacy Mode and Pseudo Channel Mode](#) for detailed explanation of pseudo channel mode operation and timing. The pseudo channel not selected by BA4 performs a CNOP.

NOTE 8 The SID bits act as bank address bit in conjunction with READ and WRITE commands, and related timing diagrams shall be interpreted accordingly. The MRS command does not use SID. Input C0 is SID for 8-High configurations, and SID0 for 12-High configurations. Input C8 is SID1 for 12-High configurations. The bits are V for all other configurations.

NOTE 9 HBM configurations using the SID specify a timing parameter t_{CCDR} for consecutive READs to different SID. Vendor datasheets should be checked for details.

NOTE 10 Input C8 is only present with HBM2 configurations whose addressing includes the RA14 or SID1 address bit or both (see Table 4). If input C8 is present, input R6 for the row commands (see Table 30) is present as well.

6.3.1 Command Truth Tables (cont'd)

Table 32 — CKE Truth Table

CURRENT STATE	CKE		ROW COMMAND	ACTION	NOTES
	PREVIOUS CYCLE (N-1)	CURRENT CYCLE (N)			
Power-Down	L	L	X	Maintain Power-Down	1,4,6,7
	L	H	RNOP	Power-Down Exit	1,2,3,8
Self Refresh	L	L	X	Maintain Self Refresh	1,4,9
	L	H	RNOP	Self Refresh Exit	1,2,3,8
Bank(s) Active	H	L	RNOP	Active Power-Down Entry	2,3,6,7
Precharging	H	L	RNOP	Power-Down Entry	2,3,6,7
Refreshing	H	L	RNOP	Power-Down Entry	2,3,6,7
All Banks Idle	H	L	RNOP	Precharge Power-Down Entry	2,3,6,7
	H	L	REF	Self Refresh Entry	2,4,5,9

NOTE 1 X = Don't care (command decoder disabled).

NOTE 2 CKE is a single data rate input and CKE transition from HIGH to LOW or LOW to HIGH is evaluated only with the rising edge of CK.

NOTE 3 With CKE transition from HIGH to LOW or LOW to HIGH, CNOP commands must be registered on column bus.

NOTE 4 In power-down state (either active or precharge) and self refresh state, row and column bus signals are X (Don't care; either HIGH or LOW or floating).

NOTE 5 Self refresh mode can only be entered from all banks idle state. Idle state is defined as all banks are closed (t_{RP} , t_{DAL} , etc. satisfied), no data bursts are in progress, CKE is HIGH and all timing from previous operations are satisfied as well as all Self refresh exit and power-down exit timing parameters are satisfied.

NOTE 6 The power-down state (either active or precharge) does not perform any refresh operation.

NOTE 7 In power-down mode, clocks may be turned off after t_{CKSRE} .

NOTE 8 Clocks must be valid and stable t_{CKSRX} time prior to power-down and self refresh exit.

NOTE 9 After self refresh entry, clocks may be turned off after t_{CKSRE} .

6.3.2 Row Commands

6.3.2.1 Row No Operation Command (RNOP)

The ROW NO OPERATION (RNOP) command as shown in Figure 16 is used to instruct the HBM device to perform a NOP as row command; this prevents unwanted row commands from being registered during idle or wait states. Operations already in progress are not affected.

Parity is evaluated on all R[6:0] or R[5:0] inputs when the parity calculation is enabled in the Mode Register.

RNOP is assumed on subsequent timing diagrams unless other row commands are explicitly shown.

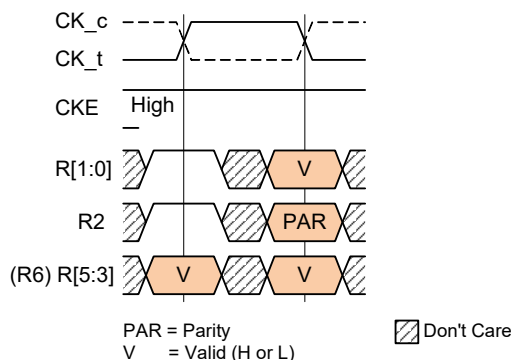


Figure 16 — RNOP Command

6.3.2.2 Bank and Row ACTIVATE Command (ACT)

Before a READ or WRITE command can be issued to a bank, a row in that bank must be opened. This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated. Once a row is open, a READ or WRITE command could be issued to that row, subject to the t_{RCD} specification.

The ACTIVATE command is a 2-cycle command as shown in Figure 17. The actual bank and row activation is initiated with the second clock cycle; therefore all relevant timing parameters refer to this second clock cycle as shown in subsequent timing diagrams.

Parity is evaluated on all R[6:0] or R[5:0] inputs separately on both clock cycles of the ACT command when the parity calculation is enabled in the Mode Register.

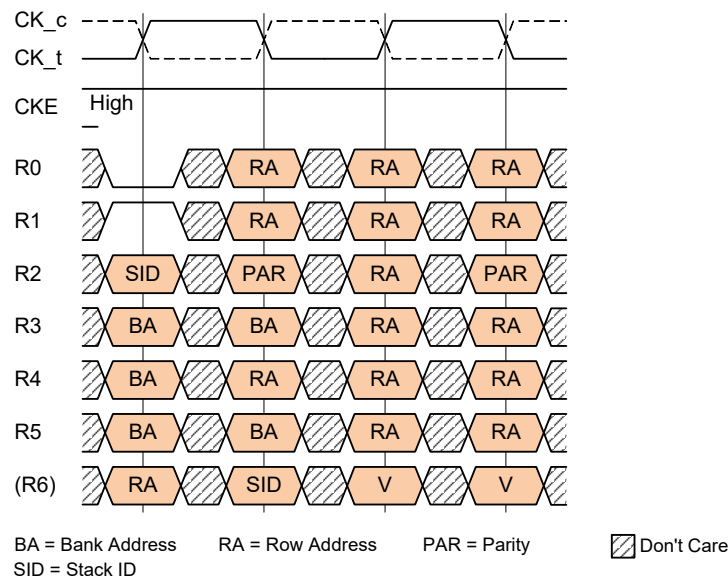
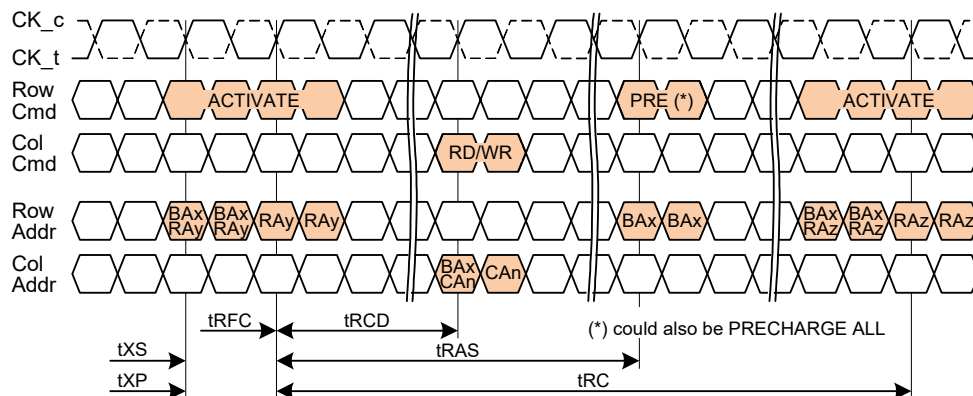


Figure 17 — ACTIVATE Command

A subsequent ACTIVATE command to another row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by t_{RC} , as shown in Figure 18. A minimum time t_{RAS} must have elapsed between opening and closing a row.



1. BAx = bank address x; RAy,z = row address y,z; CAn = column address n.
2. t_{RCD} = t_{RCDRD} or t_{RCDWR} , depending on command.
3. An ACTIVATE command is allowed ($t_{XP} + 1$ tCK) after power-down exit, and ($t_{XS} + 1$ tCK) after self refresh exit.

Figure 18 — Bank and Row Activation Command Cycle

6.3.2.2 Bank and Row ACTIVATE Command (ACT) (cont'd)

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by t_{RRD} . The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Precharge) is issued to the bank.

6.3.2.2.1 Bank Restrictions

There is a need to limit the number of bank activations in a rolling window to ensure that the instantaneous current supplying capability of the device is not exceeded. To reflect the short term capability of the HBM device's current supply, the parameter t_{FAW} (four activate window) is defined: no more than 4 banks may be activated in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW} (ns) by t_{CK} (ns) and rounding up to next integer value. As an example of the rolling window, if (t_{FAW}/t_{CK}) rounds up to 25 clocks, and an ACTIVATE command is issued at clock T0, no more than three further ACTIVATE commands may be issued at clocks T1 through T24 as illustrated in Figure 19.

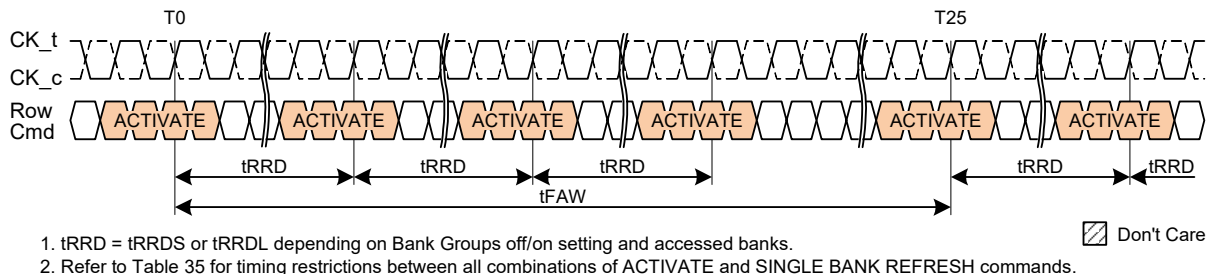


Figure 19 — Multiple Bank Activations

6.3.2.3 Bank and Row ACTIVATE Command (ACT) - Implicit Precharge

For devices operating in pseudo channel mode, a subsequent ACTIVATE command to another row in the same bank can be issued without closing the previous row. If a row is open and a new row within the bank is activated, the DRAM will internally issue a PRE command (imPRE) after the 2nd clock to precharge the row. After the imPRE command time has elapsed as set by MR6 (see Table 17), the requested ACTIVATE command is issued internally.

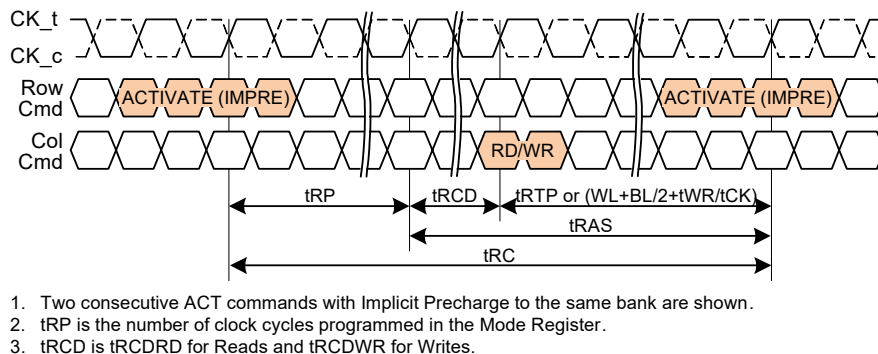


Figure 20 — imPRE to imPRE Timing

In the case of an imPRE to a row, a READ or WRITE to that row can be issued after $t_{RP} + t_{RCD}$. The minimum time interval between successive ACTIVATE commands to the same bank is defined by t_{RC} as shown in Figure 21. A minimum time t_{RAS} must have elapsed between actual opening and closing a row (closing can be done by either imPRE or external PRE command).

6.3.2.3 Bank and Row ACTIVATE Command (ACT) - Implicit Precharge (cont'd)

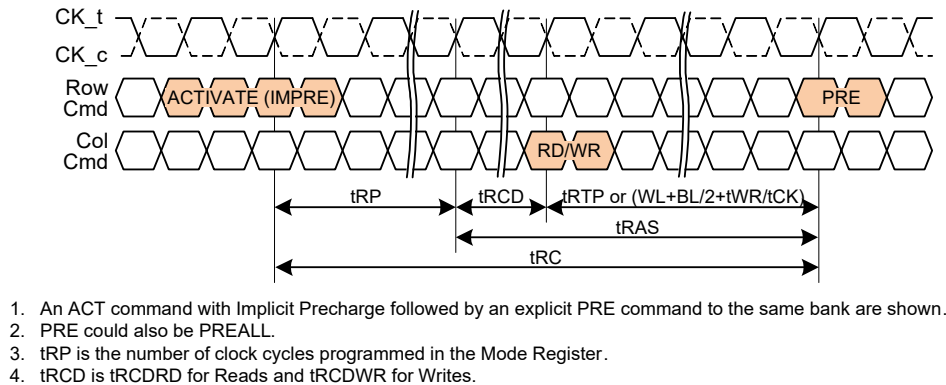


Figure 21 — imPRE to Explicit PRE

ACTIVATE to ACTIVATE times to different banks is limited by the t_{RRD} spec. For back to back activates to banks with open rows or back to back activates to banks with no open rows, t_{RRD} applies. For back to back ACTIVATE first to a bank with an open row and then an ACTIVATE to a bank that is idle (closed), the ACTIVATE to ACTIVATE time is $t_{RRD} + t_{RP}$ to allow for the first bank to complete its internal precharge shown in Figure 22. For back to back ACTIVATE first to a bank that is idle (closed) and then an ACTIVATE to a bank that has an open row, the ACTIVATE to ACTIVATE time is $\text{MAX}\{(t_{RRD} - t_{RP}), 4 t_{CK}\}$ shown in Figure 23.

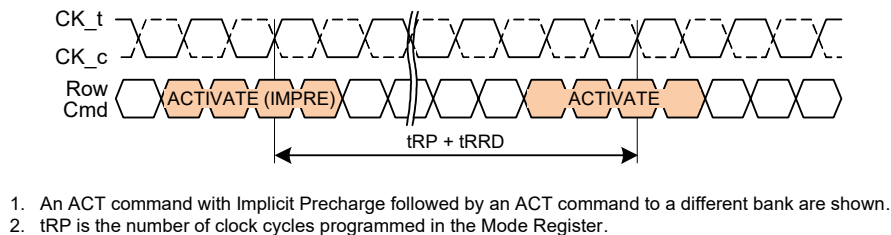


Figure 22 — imPRE to ACTIVATE

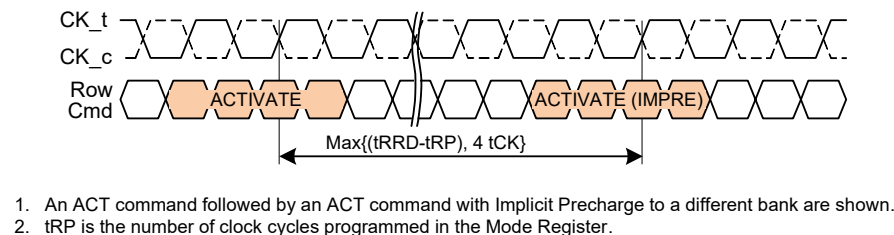


Figure 23 — ACTIVATE to imPRE

There is a limit to the number of concurrent imPRE commands. If an ACTIVATE command triggers an imPRE, a subsequent ACTIVATE command to a different bank with an already open row can be issued within the t_{RP} time of the previous imPRE. Only four concurrent imPRE commands can occur, meaning that the minimum interval between a first and a fifth consecutive imPRE command is given by $(t_{RP} + t_{RRD})$ as shown in Figure 24.

6.3.2.3 Bank and Row ACTIVATE Command (ACT) - Implicit Precharge (cont'd)

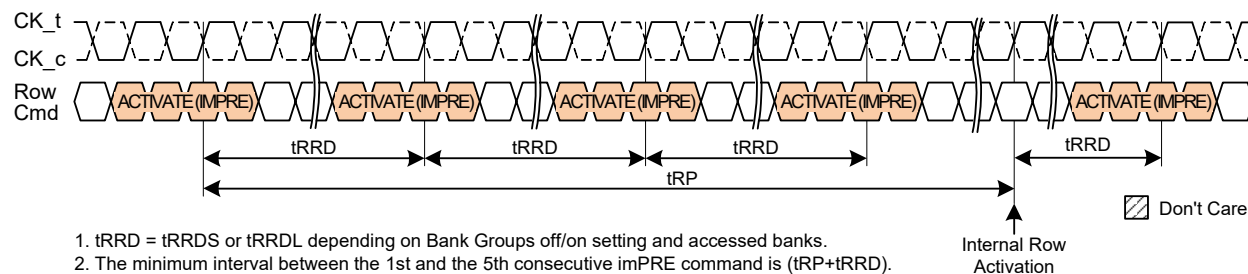


Figure 24 — Concurrent Activations with Implicit Precharge

An explicit PRE command can be issued to yet a different bank with one or two ongoing imPRE commands. PREALL cannot be issued with ongoing imPRE commands.

6.3.2.4 Precharge Command (PRE/PREALL)

The PRECHARGE command is used to deactivate the open row in a particular bank (PRE) or the open rows in all banks (PREALL). The bank(s) will be in idle state and available for a subsequent row access a specified time t_{RP} after the PRECHARGE command is issued.

Parity is evaluated with the PRECHARGE command when the parity calculation is enabled in the Mode Register.

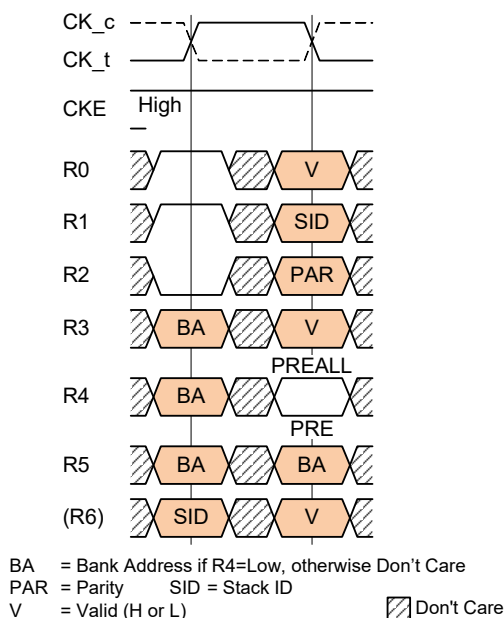


Figure 25 — PRECHARGE Command

Input R4 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, bank addresses BA[3:0] select the bank. Otherwise the bank addresses are treated as “Don't Care”.

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

6.3.2.4.1 AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit PRECHARGE command. Auto Precharge is nonpersistent meaning that it is enabled or disabled along for each individual READ or WRITE command.

For read bursts an auto precharge of the bank and row that is addressed with the READ command begins t_{RTP} after the READ command was issued or after t_{RAS} has been met, with t_{RAS} as programmed in clock cycles in the RAS field of Mode Register MR3 OP[5:0].

For write bursts an auto precharge of the bank and row that is addressed with the WRITE command begins $WL + BL/2 + WR$ clock cycles after the WRITE command was issued or after t_{RAS} has been met, with WR as programmed in clock cycles in the WR field of MR1 OP[4:0] (Table 10) and t_{RAS} as programmed in clock cycles in the RAS field of MR3 OP[5:0] (Table 12).

Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for READ or WRITE commands. A precharge resulting from a READ or WRITE with Auto Precharge may occur in parallel with an explicit PRECHARGE or PREALL command.

6.3.2.4.1 AUTO PRECHARGE (cont'd)

Table 33 — Precharge and Auto Precharge Timings

FROM COMMAND	TO COMMAND	MINIMUM DELAY BETWEEN “FROM COMMAND” TO “TO COMMAND”	UNIT	NOTE
READ	PRECHARGE (same bank)	t_{RTP}	nCK	5
	PRECHARGE (different bank)	0	nCK	4
	PREALL	t_{RTP}	nCK	5
	WRITE or WRITE w/ AP (any bank)	t_{RTW}	ns	
	READ or READ w/ AP (any bank)	t_{CCD}	nCK	6
READ w/ AP	PREALL	t_{RTP}	nCK	5
	PRECHARGE (different bank)	0	nCK	4
	ACTIVATE or REFRESH SINGLE BANK (same bank)	$t_{RTP} + RU(t_{RP}/t_{CK})$	nCK	2,5
	WRITE or WRITE w/ AP (same bank)	Illegal		
	WRITE or WRITE w/ AP (different bank)	t_{RTW}	ns	
	READ or READ w/ AP (same bank)	Illegal		
	READ or READ w/ AP (different bank)	t_{CCD}	nCK	6
WRITE	PRECHARGE (same bank)	$WL + BL/2 + RU(t_{WR}/t_{CK})$	nCK	2,7
	PRECHARGE (different bank)	0	nCK	4
	PREALL	$WL + BL/2 + RU(t_{WR}/t_{CK})$	nCK	2,7
	WRITE or WRITE w/ AP (any bank)	t_{CCD}	nCK	6
	READ w/ AP (same bank)	$WL + BL/2 + MAX[RU(t_{WR}/t_{CK}) - t_{RTP}, t_{WTR}]$	nCK	2,5,7,8
	READ (same bank)	$WL + BL/2 + t_{WTR}$	nCK	7,8
	READ or READ w/ AP (different bank)	$WL + BL/2 + t_{WTR}$	nCK	7,8
WRITE w/ AP	PREALL	$WL + BL/2 + RU(t_{WR}/t_{CK})$	nCK	2,7
	PRECHARGE (different bank)	0	nCK	4
	ACTIVATE or REFRESH SINGLE BANK (same bank)	$WL + BL/2 + WR + RU(t_{RP}/t_{CK})$	nCK	2,7
	WRITE or WRITE w/ AP (same bank)	Illegal		
	WRITE or WRITE w/ AP (different bank)	t_{CCD}	nCK	6
	READ or READ w/ AP (same bank)	Illegal		
	READ or READ w/ AP (different bank)	$WL + BL/2 + t_{WTR}$	nCK	7,8
PRECHARGE	PRECHARGE (same bank)	1	nCK	
	PREALL	1	nCK	3
PREALL	PRECHARGE or PREALL	1	nCK	3

NOTE 1 A command issued during the minimum delay time is illegal.

NOTE 2 RU = round up to next integer.

NOTE 3 PREALL is treated as a NOP for a bank when that bank is already idle or in the process of being precharged.

NOTE 4 READ or WRITE and PRECHARGE commands may be issued simultaneously.

NOTE 5 t_{RTP} could either be t_{RTPS} or t_{RTPL} .NOTE 6 t_{CCD} could either be t_{CCDS} or t_{CCDL} ; for READs, t_{CCD} could also be t_{CCDR} .

NOTE 7 WL = write latency. BL = burst length.

NOTE 8 t_{WTR} could either be t_{WTRS} or t_{WTRL} .

6.3.2.5 REFRESH Command (REF)

The REFRESH command is used during normal operation of the HBM device. The command is received on the row command inputs R[6:0] or R[5:0] as shown in Figure 26 and requires a CNOP command on the column command inputs C[8:0] or C[7:0].

Parity is evaluated with the REFRESH command when the parity calculation is enabled in the Mode Register.

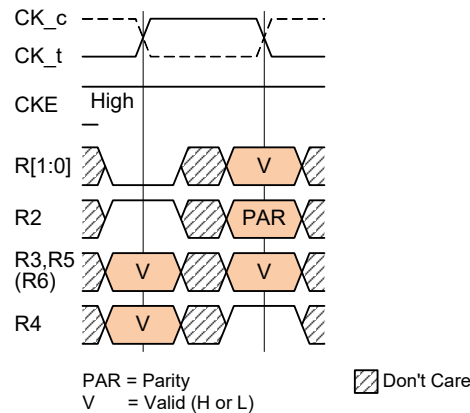
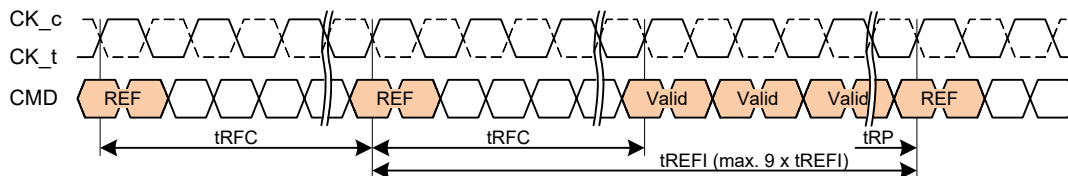


Figure 26 — REFRESH Command

The REFRESH command is nonpersistent, so it must be issued each time a refresh is required. A minimum time t_{RFC} is required between two REFRESH commands or a REFRESH command and any subsequent access command after the refresh operation. All banks must be precharged with t_{RP} satisfied prior to the REFRESH command. The banks are in idle state after completion of the REFRESH command.

The refresh addressing is generated by an internal refresh controller. This makes the address bits “Don’t Care” during a REFRESH command.



1. Only RNOP and CNOP commands allowed after REFRESH command registered until t_{RFC} expires.
2. The time interval between two REFRESH commands may be extended to a maximum of $9 \times t_{REFI}$.

Figure 27 — Refresh Cycle

In general, the HBM device requires REFRESH cycles at an average periodic interval of t_{REFI} . To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 REFRESH commands can be postponed during operation of the HBM device, meaning that at no point in time more than a total of 8 REFRESH commands are allowed to be postponed. In case that 8 REFRESH commands are postponed in a row, the resulting maximum interval between the surrounding REFRESH commands is limited to $9 \times t_{REFI}$ (see Figure 28). A maximum of 8 additional REFRESH commands can be issued in advance (“pulled in”), with each one reducing the number of regular REFRESH commands required later by one. Note that pulling in more than 8 REFRESH commands in advance does not further reduce the number of regular REFRESH commands required later, so that the resulting maximum interval between two surrounding REFRESH commands is limited to $9 \times t_{REFI}$ (see Figure 29). At any given time, a maximum of 16 REFRESH commands can be issued within $2 \times t_{REFI}$.

6.2.3.5 REFRESH Command (REF) (cont'd)

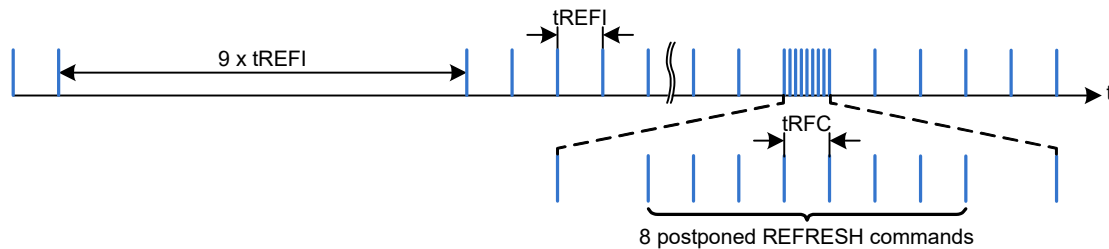


Figure 28 — Postponing Refresh Commands (Example)

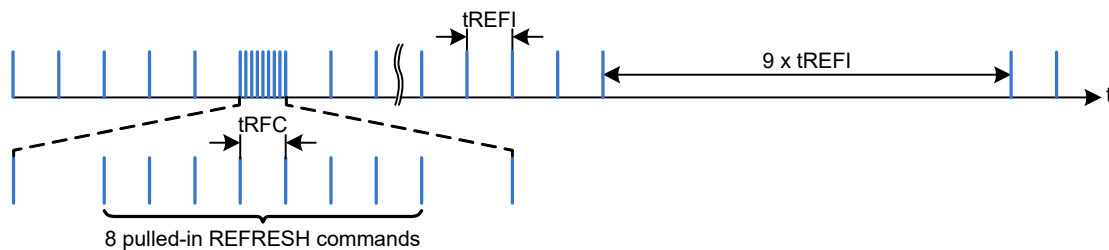


Figure 29 — Pulling-In Refresh Commands (Example)

Self refresh mode may be entered with a maximum of eight REFRESH commands being postponed. After exiting self refresh mode with one or more REFRESH commands postponed, additional REFRESH commands may be postponed to the extent that the total number of postponed REFRESH commands (before and after the self refresh) will never exceed eight. During self refresh mode, the number of postponed or pulled-in REFRESH commands does not change.

6.3.2.6 SINGLE BANK REFRESH Command (REFSB)

The SINGLE BANK REFRESH command provides an alternative solution for the refresh of the HBM device. The command initiates a refresh cycle on a single bank while accesses to other banks including writes and reads are not affected. The command is received on the row command inputs R[6:0] or R[5:0] as shown in [Figure 30](#).

Parity is evaluated with the SINGLE BANK REFRESH command when the parity calculation is enabled in the Mode Register.

6.3.2.6 SINGLE BANK REFRESH Command (REFSB) (cont'd)

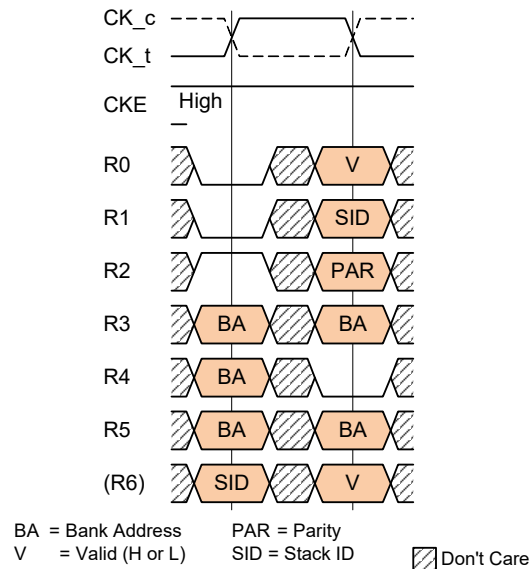
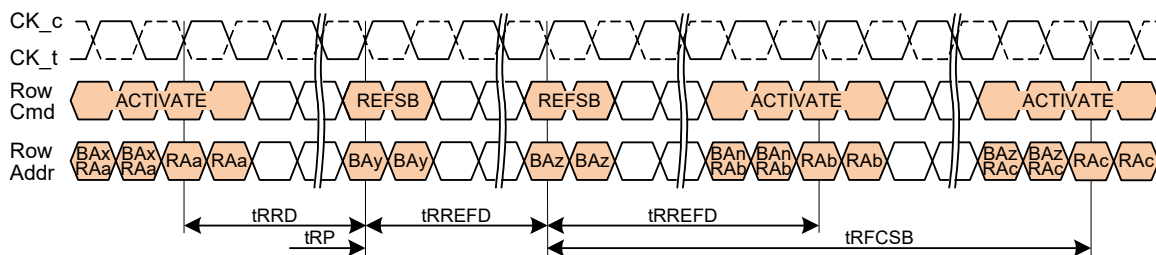


Figure 30 — SINGLE BANK REFRESH Command

The SINGLE BANK REFRESH command is nonpersistent, so it must be issued each time a refresh is required.

A minimum time t_{RRD} is required between an ACTIVATE command and a SINGLE BANK REFRESH command to a different bank. A minimum time t_{RREFD} is required between any two SINGLE BANK REFRESH commands (see below for an exception requiring t_{RFCSB}), and between a SINGLE BANK REFRESH command and an ACTIVATE command to a different bank as shown in Figure 31. A minimum time t_{RFCSB} is required between a SINGLE BANK REFRESH command and an access command to the same bank that follows. The selected bank must be precharged with t_{RP} satisfied prior to the SINGLE BANK REFRESH command. The bank is in idle state after completion of the SINGLE BANK REFRESH command.



1. BAn,x,y,z = bank address n,x,y,z ; RAa,b,c = row address a,b,c .
2. t_{RRD} timing must be met between ACTIVATE commands and REFSB command to different banks.
3. t_{RREFD} timing must be met between consecutive REFSB commands to different banks, and between a REFSB command followed by an ACTIVATE command to the different bank.
4. t_{RFCSB} timing must be met between a REFSB command followed by an ACTIVATE command to the same bank.

Figure 31 — Single Bank Refresh Command Cycle

6.3.2.6 SINGLE BANK REFRESH Command (REFSB) (cont'd)

The row address for each bank is provided by internal refresh counters. This makes the row address bits “Don’t Care” during SINGLE BANK REFRESH commands.

A SINGLE BANK REFRESH command to one of the 8, 16, 32 or 48 (32 or 48 banks for HBM configurations with SID) banks can be issued in any order. After all banks have been refreshed using the SINGLE BANK REFRESH command and after waiting for at least t_{RCSB} , the controller can issue another set of SINGLE BANK REFRESH commands in the same or different order. However, it is illegal to send another SINGLE BANK REFRESH command to a bank unless all banks have been refreshed using the SINGLE BANK REFRESH command. The controller must track the bank being refreshed by the SINGLE BANK REFRESH command.

The bank count is synchronized between the controller and the HBM device by resetting the bank count to zero. Synchronization can occur upon exit from reset state or by issuing a REFRESH or SELF REFRESH ENTRY command. Both commands may be issued at any time even if a preceding sequence of SINGLE BANK REFRESH commands has not completed cycling through all banks.

The example in Table 34 (with 16 banks shown as an example) shows two full sets of REFSB commands with the bank counter reset to 0 and the refresh counter incremented after 16 REFSB commands each. The 3rd set of REFSB commands is interrupted by the REFRESH command which resets the bank counter to 0 and performs refreshes to all banks indicated by the refresh counter.

Table 34 — Refresh Counter Increments

COUNT	SUB-COUNT	COMMAND	BANK ADDR	REFRESH BANK	BANK COUNTER	REFRESH COUNTER
0	0	Reset, REFRESH or SRE command			To 0	
1	1	REFSB	0000	0	0 to 1	n
2	2	REFSB	0001	1	1 to 2	
3	3	REFSB	0010	2	2 to 3	
4	4	REFSB	0011	3	3 to 4	
...						
15	15	REFSB	1110	14	14 to 15	
16	16	REFSB	1111	15	15 to 0	
17	1	REFSB	0100	4	0 to 1	n + 1
18	2	REFSB	0111	7	1 to 2	
19	3	REFSB	1011	11	2 to 3	
20	4	REFSB	0110	6	3 to 4	
...						
31	15	REFSB	1100	12	14 to 15	
32	16	REFSB	0001	1	15 to 0	
33	1	REFSB	0010	2	0 to 1	n + 2
34	2	REFSB	1001	9	1 to 2	
35	3	REFSB	0000	0	2 to 3	
36	0	REFRESH	V	all	To 0	n + 2
37	1	REFSB	1010	10	0 to 1	n + 3
38	2	REFSB	0101	5	1 to 2	
...						

