

JEDEC STANDARD

Reliability Qualification of Power Amplifier Modules

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Foreword

A unique application of semiconductor integrated circuits is within a module. Modules are sometimes referred to as a system-in-package (SIP) or hybrid. For the purpose of this document, we define a *module* as an assembly that integrates multiple semiconductor die within one package. Such a module is not restricted to semiconductors – it can also contain passive devices that include components such as resistors, capacitors, inductors, filters, and couplers that are either built-in to the substrate or added as Surface Mount Devices. Another unique aspect of a Laminate-based Power Amplifier Module (PAM) is the application of Compound Semiconductors. To further refine the classification of modules, we have specifically selected amplification to be the core function. But amplification is not necessarily the only function. Switching, power control, power detection, signal reception, filtering, and ESD suppression may be other functions performed within a module. Additionally, many of the functions may be employed over various frequencies and at various output power levels – such that these functions are arranged in a parallel fashion within the module. A typical module application is a Power Amplifier Module (PAM) used at or near the “front-end” of a cellular phone or mobile device. PAMs are an enabling component of cell phones that transmit signals with high efficiency, linearity, and reliability in a manner that is yet unmatched by monolithic devices. A typical PAM consists of a substrate, which may be a leadframe material, but is more commonly a ceramic or laminate multi-layer base. Upon the base, the aforementioned die and components are mounted, and all components are encapsulated, using packaging materials, such as an epoxy, most commonly formed by a transfer mold process. Hermetic versions of PAMs utilize ceramic substrates and lids or caps that seal the various components within. Even though similar types of modules have been utilized for semiconductors in the past, the use of Compound Semiconductors, with a laminate substrate, for relatively high power dissipation wireless application at radio frequencies (RF) is seemingly unique.

Introduction

This standard is intended to identify a core set of qualification tests that apply specifically for Power Amplifier Modules and their primary application in mobile devices such as cellular phones.

There is a substantial amount of confusion and inefficiency in module reliability testing that is driven by:

- a) frequent attempts to apply silicon standards to compound semiconductor modules, and
- b) lack of ability to steer customers away from the silicon oriented standards that have dominated the industry for years.

This standard is intended to describe specific stresses and failure mechanisms that are specific to compound semiconductors and power amplifier modules. It is intended to establish more meaningful and efficient qualification testing.

RELIABILITY QUALIFICATION OF POWER AMPLIFIER MODULES

(From JEDEC Board Ballot JCB-14-09, formulated under the cognizance of the JC-14.7 Task Group on a Power Amplifier Module Standard)

1 Scope

This standard describes a baseline set of acceptance tests for use in qualifying power amplifier modules as an individual new product, a product family, or as products in a process which is being changed. These tests are capable of stimulating and precipitating semiconductor device, internal component, laminate, and packaging failures. The objective is to precipitate failures in an accelerated manner compared to use conditions. Failure rate projections usually require larger sample sizes than are called out in qualification testing and durations or stresses which would exacerbate normal wearout. For guidance on projecting failure rates, refer to JESD85 *Methods for Calculating Failure Rates in Units of FITs*. This qualification standard is not aimed at extreme use conditions such as military applications, automotive under-the-hood applications, or uncontrolled avionics environments, nor does it address 2nd level reliability considerations, which are addressed in JEP150.

This set of tests should not be used indiscriminately. Each qualification project should be examined for:

- a) Any potential new and unique failure mechanisms.
- b) Any situations where these tests/conditions may induce invalid or overstress failures.

If it is known or suspected that failures either are due to new mechanisms or are uniquely induced by the severity of the test conditions, then the application of the test condition as stated is not recommended. Alternatively, new mechanisms or uniquely problematic stress levels should be addressed by building an understanding of the mechanism and its behavior with respect to accelerated stress conditions (Ref. JESD91 *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms*.)

Another alternative qualification method is described in JESD94 *Application Specific Qualification using Knowledge Based Test Methodology*. This technique involves establishing the (worst case) use conditions and tailoring the stress methods, stress levels, and durations to match the use conditions.

Since the assembly is considered an integral part of the power amplifier module, this standard includes the applicable package-related stresses. However, if special consideration of assembly-level effects is necessary, then guidance from JEP150, Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components, is recommended.

2 Reference documents

J-STD-020, Joint IPC/JEDEC Standard, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Devices*.
JP-001, *Foundry Process Qualification Guidelines* (Wafer Fabrication Manufacturing Sites).
JESD22 Series, *Reliability Test Methods for Packaged Devices*
JESD46, *Guidelines for User Notification of Product/process Changes by Semiconductor Suppliers*.
JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*.
JESD69, *Information Requirements for the Qualification of Silicon Devices*.
JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components*.
JESD78, *IC Latch-Up Test*.
JESD85, *Methods for Calculating Failure Rates in Units of FITs*.
JESD86, *Electrical Parameters Assessment*.
JESD94, *Application Specific Qualification using Knowledge Based Test Methodology*.
JESD91, *Methods for Developing Acceleration Models for Electronic Component Failure Mechanisms*.
JEP122, *Failure Mechanisms and Models for Semiconductor Devices*.
JEP150, *Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components*.
JESD226, RFBL – Test Method for RF Biased Lifetesting

3 General requirements

3.1 Objective

The objective of this procedure is to ensure that the power amplifier module to be qualified meets a generally accepted set of stress test driven qualification requirements. Qualification is aimed at components used in commercial or industrial operating environments.

3.2 Qualification family

While this specification may be used to qualify an individual component, it is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs. Interactive effects of the semiconductor and package shall be considered in applying family designations.

3.3 Lot requirements

Test samples shall comprise representative samples from the qualification family. Manufacturing variability and its impact on reliability shall be assessed. Where applicable, the test samples will be composed of approximately equal numbers from at least three (3) nonconsecutive lots. Other appropriate means may be used to evaluate manufacturing variability. Sample size and pass/fail requirements are listed in Table 1 and Table 2. Table A and Table B give guidance on translating pass/fail requirements to larger sample sizes.