

JEDEC STANDARD

High Bandwidth Memory DRAM (HBM3)

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HIGH BANDWIDTH MEMORY DRAM (HBM3)**Contents**

	Pages
1 Scope	1
2 Features	1
3 Organization	2
3.1 Channel Definition	3
3.1.1 Summary of Per-Channel Signals	3
3.1.2 Pseudo Channel	4
3.1.3 Dual Command Interfaces.....	5
3.2 Channel Addressing	6
3.2.1 Bank Groups.....	7
3.3 Simplified State Diagram	8
4 Initialization	9
4.1 HBM3 Power-up and Initialization Sequence.....	9
4.2 Controlled Power-off Sequence	11
4.3 Initialization Sequence with Stable Power	12
4.4 Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs and Channel Disable	12
5 Mode Registers.....	16
6 Operation.....	26
6.1 HBM3 Clocking Overview	26
6.1.1 WDQS-to-CK Alignment Training	28
6.2 HBM3 Data Bus Inversion (DBIac).....	30
6.2.1 Data Bus Inversion (DBIac).....	30
6.2.1.1 Internal DBIac State with Read.....	31
6.3 Commands.....	34
6.3.1 Command Truth Tables.....	35
6.3.2 Row Commands	37
6.3.2.1 Row No Operation (RNOP) Command.....	37
6.3.2.2 ACTIVATE (ACT) Command.....	38
6.3.2.3 PRECHARGE (PREpb) and PRECHARGE ALL (PREab) Commands	41
6.3.2.4 Rounding Rules for Row Access Timings	45
6.3.2.5 REFRESH Command (REFab).....	46
6.3.2.6 PER-BANK REFRESH Command (REFpb).....	48
6.3.2.7 Refresh Management (RFM).....	52
6.3.2.8 Adaptive Refresh Management (ARFM)	54
6.3.3 Column Commands	56
6.3.3.1 Column No Operation (CNOP).....	56
6.3.3.2 Read Command (RD, RDA)	57
6.3.3.3 Write Command (WR, WRA).....	67
6.3.3.4 Mode Register Set (MRS) Command	75
6.3.4 Power-Mode Commands.....	77
6.3.4.1 Power-Down (PDE, PDX)	77
6.3.4.2 Self Refresh (SRE, SRX)	83
6.4 Parity	87
6.4.1 Command/Address Parity	87
6.4.2 Data Parity.....	90

Contents (cont'd)

6.5	Clock Frequency Change Sequence	94
6.6	Temperature Compensated Refresh Reporting	94
6.6.1	Temperature Compensated Refresh Trip Points.....	94
6.6.2	Catastrophic Temperature Sensor	94
6.7	Interconnect Redundancy Remapping.....	95
6.7.1	AWORD Remapping	95
6.7.1.1	Row Command Bus – Remapping Table	95
6.7.1.2	Column Command Bus – Remapping Table.....	96
6.7.1.3	AWORD Remapping Examples.....	96
6.7.2	DWORD Remapping	97
6.7.2.1	DWORD Remapping Table	98
6.7.2.2	DWORD Remapping Example	99
6.8	HBM3 Loopback Test Modes	101
6.8.1	HBM3 Polynomial Structure.....	102
6.8.1.1	AWORD MISR Polynomial.....	102
6.8.1.2	DWORD MISR Polynomial.....	103
6.8.2	General Loopback Modes Features and Behavior.....	103
6.8.3	AWORD and DWORD Write MISR Modes	108
6.8.3.1	Test Method for AWORD (Write) MISR Mode	108
6.8.3.2	Test Method for DWORD Write MISR Mode.....	109
6.8.4	AWORD and DWORD Write Register Modes.....	109
6.8.4.1	Test Method for AWORD (Write) Register Mode.....	109
6.8.4.2	Test Method for DWORD Write Register Mode	110
6.8.5	DWORD Read Register Mode	111
6.8.5.1	Test Method for DWORD Read Register Mode	111
6.8.6	DWORD LFSR Mode (Read direction)	112
6.8.6.1	Test Method for DWORD LFSR Mode (Read direction).....	112
6.8.7	AWORD and DWORD Write LFSR Compare Modes	113
6.8.7.1	Test method for AWORD (Write) LFSR Compare Mode	114
6.8.7.2	Test Method for DWORD Write LFSR Compare mode.....	114
6.9	On-die DRAM ECC	115
6.9.1	ECC Overview	115
6.9.2	HBM3 On-die ECC Requirements.....	116
6.9.3	DRAM Fault Isolation Requirements.....	116
6.9.4	Error Check and Scrub (ECS)	116
6.9.5	On-die ECC Transparency Protocol.....	120
6.9.6	ECC Engine Test Mode.....	121
6.10	WOSC	125
6.10.1	WDQS Interval Oscillator.....	125
6.10.2	tWDQS2DQ_I Offset due to Temperature and Voltage Variation	129
6.11	DCA and DCM.....	130
6.11.1	Duty Cycle Adjuster (DCA).....	130
6.11.2	Duty Cycle Monitor (DCM).....	132
6.12	Self Repair.....	134
7	Operating Conditions	138
7.1	Absolute Maximum DC Rating.....	138
7.2	Recommended DC Operating Condition	138

Contents (cont'd)

7.3	Operating Temperature	139
8	Electrical Characteristics and DQ/CA Rx	140
8.1	Leakage Current	140
8.2	Capacitance	140
8.3	DQ Rx Voltage and Timing	141
8.4	AWORD Signaling	145
8.5	CK and WDQS Input Signaling	145
8.6	Midstack Signaling.....	147
8.7	Transmit Driver Currents	147
8.8	Output Timing Reference Load.....	147
8.9	Output Voltage Level	148
8.10	Output Rise and Fall Time	148
8.11	Overshoot/Undershoot	149
9	IDD Specification.....	150
9.1	IDD and IPP Specification Parameters and Test Conditions	150
9.2	IDD and IPP Specifications.....	159
9.3	IDD6 Specification.....	159
10	AC Timings	160
11	Package (Die) Specification	167
11.1	Signals	167
11.2	MicroBump Positions.....	169
11.3	HBM3 Stack Height.....	170
11.4	HBM3 Bump Map.....	170
12	HBM DRAM Assembly	201
13	Test and Boundary Scan.....	201
13.1	Direct Access (DA) Test Port.....	201
13.1.1	DA Test Port Lockout	202
13.2	IEEE Standard 1500	202
13.2.1	Interaction Between DA Test Port and IEEE1500 Test Access Port	202
13.2.2	IEEE1500 Test Access Port I/O Signals	203
13.2.3	IEEE1500 Test Access Port Functional Description	203
13.3	Wrapper Data Register (WDR) Types	206
13.3.1	Read Only (R) Wrapper Data Registers	206
13.3.2	Write Only (W) Wrapper Data Registers	206
13.3.3	Read and Write (R/W) Wrapper Data Registers	206
13.3.4	WDR Reset State.....	206
13.4	IEEE1500 Test Access Port Instruction Encodings	207
13.5	Test Instructions	208
13.5.1	BYPASS.....	210
13.5.2	EXTEST_RX and EXTEST_TX.....	211
13.5.3	HBM_RESET.....	215
13.5.4	MBIST.....	216
13.5.5	SOFT_REPAIR.....	217
13.5.6	HARD_REPAIR	219
13.5.7	DWORD_MISR.....	220
13.5.8	AWORD_MISR.....	222
13.5.9	CHANNEL_ID.....	224

Contents (cont'd)

13.5.10	AWORD_MISR_CONFIG	224
13.5.11	DEVICE_ID	225
13.5.12	TEMPERATURE.....	229
13.5.13	MODE_REGISTER_DUMP_SET	230
13.5.14	READ_LFSR_COMPARE_STICKY	231
13.5.15	SOFT_LANE_REPAIR and HARD_LANE_REPAIR	233
13.5.16	CHANNEL_DISABLE	236
13.5.17	CHANNEL TEMPERATURE.....	237
13.5.18	WOSC_RUN and WOSC_COUNT	240
13.5.19	ECS Error Log.....	241
13.5.20	HS_REP_CAP.....	243
13.5.21	SELF_REP and SELF_REP_RESULTS.....	244
13.6	Interaction with Mission Mode Operation	246
13.7	IEEE1500 Test Port AC Timing Parameters.....	247
13.8	Boundary Scan	253
Annex A	– (Informative) Differences between JESD238A and JESD238	254

Tables

Table 1	– Single Channel Signal Count	3
Table 2	– Global Signal Count	3
Table 3	– Array Access Timings Counted Individually Per Pseudo Channel	4
Table 4	– HBM3 Channel Addressing	6
Table 5	– Bank Group Assignments.....	7
Table 6	– Command Sequence Affected by Bank Groups	7
Table 7	– Initialization Timing Parameters.....	10
Table 8	– Power Ramp Conditions.....	10
Table 9	– Power Supply Conditions.....	11
Table 10	– HBM3 Mode Register Overview	17
Table 11	– Mode Register 0 (MR0)	18
Table 12	– Mode Register 1 (MR1)	18
Table 13	– Mode Register 2 (MR2)	19
Table 14	– Mode Register 3 (MR3)	19
Table 15	– Mode Register 4 (MR4)	19
Table 16	– Mode Register 5 (MR5)	20
Table 17	– Mode Register 6 (MR6)	20
Table 18	– Mode Register 7 (MR7)	21
Table 19	– DWORD MISR Read and Write Operations in Loopback Test Mode (MR7 OP0=1).....	22
Table 20	– Mode Register 8 (MR8)	22
Table 21	– Mode Register 9 (MR9)	23
Table 22	– Mode Register 10 (MR10)	23
Table 23	– Mode Register 11 (MR11)	24
Table 24	– Mode Register 12 (MR12)	24
Table 25	– Mode Register 13 (MR13)	24
Table 26	– Mode Register 14 (MR14)	25
Table 27	– Mode Register 15 (MR15)	25
Table 28	– Phase Detector and DERR Signal Behavior	28
Table 29	– DBI(ac) Truth Table	31

Contents (cont'd)

Table 30 – Row Commands Truth Table	35
Table 31 – Column Commands Truth Table.....	36
Table 32 – Options for issuing PREab and PREpb commands	37
Table 33 – Precharge and Auto Precharge Timings	44
Table 34 – Refresh Counter Increments (Example for HBM3 Configurations with 16 Banks)	50
Table 35 – Refresh and Per-Bank Refresh Command Scheduling Requirements	51
Table 36 – Mode Register Definition for Adaptive RFM Levels.....	54
Table 37 – RFM Commands Perceived by HBM3 DRAM	55
Table 38 – Signal Groups for Read Data De-Skew	66
Table 39 – Signal Groups for Write Data De-Skew	74
Table 40 – Pin State Description in Power Down.....	80
Table 41 – Pin State Description in Self Refresh.....	86
Table 42 – Command/Address Parity Function Table.....	87
Table 43 – Data Parity Function Table.....	91
Table 44 – Temperature Compensated Refresh Trip Points.....	94
Table 45 – AWORD - Row Command Bus Remapping.....	95
Table 46 – AWORD - Column Command Bus Remapping	96
Table 47 – Original Lane Assignment - Channel a - AWORD Column Repair.....	96
Table 48 – Remapped Lane Assignment - Channel a - AWORD Column Repair.....	96
Table 49 – Original Lane Assignment - Channel a - AWORD Row Repair	97
Table 50 – Remapped Lane Assignment - Channel a - AWORD Row Repair	97
Table 51 – DWORD Remapping (1 Byte).....	98
Table 52 – Original DWORD Lane Assignment - Channel a – Byte [1:0]	99
Table 53 – Remapped DWORD Lane Assignment - Channel a – Byte [1:0].....	99
Table 54 – MISR Function Table	102
Table 55 – ECS Modes	117
Table 56 – t_{ECSint} per Stack (ECS independent of SID).....	118
Table 57 – Error Overwrite Priority Rules to Handle Multiple Error Logging	119
Table 58 – Transparency Attributes and Their Access/Control Mechanism	120
Table 59 – Severity Encodings on the SEV pins	120
Table 60 – Severity Transmission on READ	120
Table 61 – ECC Engine Test Modes	121
Table 62 – Example of Error Vectors and Corresponding Severity	123
Table 63 – WDQS Oscillator Matching Error Specification.....	129
Table 64 – DCA Maximum Offset and Step Size.....	130
Table 65 – DCM Measurement Result.....	132
Table 66 – SELF_REP Instruction vs Stack Height	134
Table 67 – SELF_REPAIR Timings	135
Table 68 – SELF_REP – Expected DRAM Behavior When Resources Shared	136
Table 69 – Absolute Maximum DC Ratings.....	138
Table 70 – Recommended DC Operating Condition.....	138
Table 71 – Operating Temperature.....	139
Table 72 – Input Leakage Current.....	140
Table 73 – Input/Output Capacitance.....	140
Table 74 – Input Receiver Voltage Level Specification.....	142
Table 75 – AWORD Receiver Voltage Level Specification	145
Table 76 – CK and WDQS Input Voltage Level Specification.....	145

Contents (cont'd)

Table 77 – Differential Input Level for WDQS_t, WDQS_c	146
Table 78 – Differential Input Slew Rate Definition for WDQS_t, WDQS_c	146
Table 79 – Midstack Parameter Specification	147
Table 80 – Transmit Driver Current Specification	147
Table 81 – Output Voltage Level	148
Table 82 – Overshoot/Undershoot Specification for AWORD and DWORD Signals	149
Table 83 – Basic IDD/IDDQ/IPP/IDDQL Measurement Conditions	151
Table 84 – Example of Timings used for IDD Measurement-Loop Pattern	153
Table 85 – IDD0 Measurement-Loop Pattern	154
Table 86 – IDD4R Measurement-Loop Pattern	155
Table 87 – IDD4W Measurement-Loop Pattern	156
Table 88 – IDD5P Measurement-Loop Pattern	157
Table 89 – IDD7 Measurement-Loop Pattern	158
Table 90 – IDD and IPP Specification Example	159
Table 91 – IDD6 Specification	159
Table 92 – Timings Parameters (Part 1)	160
Table 93 – Timings Parameters (Part 2)	162
Table 94 – I/O Signal Description	167
Table 95 – Geometric Parameters of the Staggered MicroBump Pattern	169
Table 96 – HBM3 Stack Height	170
Table 97 – Legend	170
Table 98 – HBM3 Bump Map Footprint – Geographical Overview (not to scale)	171
Table 99 – HBM3 Bump Map Footprint : Columns 1 to 36	172
Table 100 – HBM3 Bump Map Footprint : Columns 37 to 74	177
Table 101 – HBM3 Bump Map Footprint : Columns 75 to 90	182
Table 102 – HBM3 Bump Map Footprint : Columns 91 to 118	187
Table 103 – HBM3 Bump Map Footprint : Columns 119 to 148	194
Table 104 – Direct Access (DA) Pin Allocation	201
Table 105 – Test Access Port Signal Status	203
Table 106 – IEEE1500 Test Port Signal List and Description	203
Table 107 – WIR Channel Selection Definition	207
Table 108 – Instruction Register Encodings	208
Table 109 – BYPASS Wrapper Data Register	210
Table 110 – Wrapper Boundary Register (WBR)	212
Table 111 – HBM_RESET Wrapper Data Register	215
Table 112 – RESET_n and HBM_RESET Truth Table	216
Table 113 – MBIST Wrapper Data Register	216
Table 114 – SOFT_REPAIR Wrapper Data Register	218
Table 115 – HARD_REPAIR Wrapper Data Register	219
Table 116 – DWORD_MISR Wrapper Data Register	220
Table 117 – AWORD_MISR Wrapper Data Register	223
Table 118 – CHANNEL_ID Wrapper Data Register	224
Table 119 – AWORD_MISR_CONFIG Wrapper Data Register	225
Table 120 – DEVICE_ID Wrapper Data Register	226
Table 121 – TEMPERATURE Wrapper Data Register	229
Table 122 – MODE_REGISTER_DUMP_SET Wrapper Data Register	230
Table 123 – READ_LFSR_COMPARE_STICKY Wrapper Data Register	232

Contents (cont'd)

Table 124 – LANE_REPAIR Wrapper Data Register.....	234
Table 125 – CHANNEL_DISABLE Wrapper Data Register	237
Table 126 – CHANNEL_TEMPERATURE Wrapper Data Register.....	238
Table 127 – WOSC_RUN Wrapper Data Register.....	240
Table 128 – WOSC_COUNT Wrapper Data Register	240
Table 129 – ECS Error Log Wrapper Data Register	242
Table 130 – HS_REP_CAP Wrapper Data Register	243
Table 131 – SELF_REP Wrapper Data Register.....	245
Table 132 – SELF_REP_RESULTS Wrapper Data Register	245
Table 133 – IEEE1500 Port Instruction Interactions	246
Table 134 – IEEE1500 Test Port AC Timings.....	247

Figures

Figure 1 — General Overview of a DRAM Die Stack with Channels	2
Figure 2 — Pseudo Channel Operation.....	5
Figure 3 — Simplified State Diagram.....	8
Figure 4 — Power-up and Initialization.....	11
Figure 5 — HBM3 RESET and Initialization Sequence with Stable Power	12
Figure 6 — Initialization Sequence with Lane Repair or Channel Disable	14
Figure 7 — Initialization Sequence with Channel Disable.....	15
Figure 8 — Aligned WDQS Internal Divider Example	26
Figure 9 — Clocking and Interface Relationship Write to Read Timing.....	27
Figure 10 — High Level Block Diagram Example of Clocking Scheme	27
Figure 11 — DERR Signal Behavior in WDQS-to-CK Alignment Training.....	29
Figure 12 — DBIac Algorithm.....	30
Figure 13 — Example DBIac Logic for Write and Read	31
Figure 14 — Internal DBIac State Reset for Write to Read	32
Figure 15 — Bus Preconditioning and DBI States for Read	33
Figure 16 — RNOP command	38
Figure 17 — ACTIVATE Command.....	39
Figure 18 — Bank and Row Activation Command Cycle	40
Figure 19 — Multiple Bank Activations	41
Figure 20 — PRECHARGE (PREpb) Command	42
Figure 21 — PRECHARGE ALL (PREab) Command.....	42
Figure 22 — REFRESH Command (REFab)	46
Figure 23 — REFRESH Cycle.....	47
Figure 24 — Postponing Refresh Commands (Example)	47
Figure 25 — Per-Bank Refresh Command (REFpb).....	48
Figure 26 — Per-Bank Refresh Command Cycle.....	49
Figure 27 — Sets of Per-Bank Refresh Commands	49
Figure 28 — Refresh Management (RFMab) and Per-Bank Refresh Management (RFMpb) Commands....	52
Figure 29 — CNOP Command	56
Figure 30 — READ Command	57
Figure 31 — Clock to RDQS and Data Out Timings	59
Figure 32 — Single Read Burst with BL=8.....	60
Figure 33 — Seamless Read Bursts with BL=8	61

Contents (cont'd)

Figure 34 — Non-Seamless Read Bursts with $t_{CCD}=3$ and $BL=8$	62
Figure 35 — Non-Seamless Read Burst with $t_{CCD}=4$ and $BL=8$	63
Figure 36 — Read to Write	64
Figure 37 — Read to Precharge	65
Figure 38 — Write Command.....	67
Figure 39 — Clock to WDQS and Data Input Timings	68
Figure 40 — Single Write Burst with $BL=8$	69
Figure 41 — Seamless Write Bursts with $BL=8$	70
Figure 42 — Non-Seamless Write Bursts	71
Figure 43 — Write to Read	72
Figure 44 — Write to Pre-charge	73
Figure 45 — Mode Register Set Command (MRS).....	75
Figure 46 — Mode Register Set Timings	76
Figure 47 — Power-Down Entry Command	77
Figure 48 — Power-Down Entry and Exit.....	79
Figure 49 — READ or READ with Auto Precharge to Power-Down Entry Timing.....	80
Figure 50 — WRITE or WRITE with Auto Precharge to Power-Down Entry Timing.....	81
Figure 51 — MODE REGISTER SET to Power-Down Entry Timing	81
Figure 52 — ACTIVATE to Power-Down Entry Timing.....	82
Figure 53 — REFRESH or PER-BANK REFRESH to Power-Down Entry Timing	82
Figure 54 — PRECHARGE to Power-Down Entry Timing.....	82
Figure 55 — Self-Refresh Entry Command.....	83
Figure 56 — Self-Refresh Entry and Exit.....	85
Figure 57 — Enabling and Disabling Command/Address Parity	87
Figure 58 — Single Command/Address Parity Error.....	88
Figure 59 — Separated Command/Address Parity Errors.....	88
Figure 60 — Consecutive Command/Address Parity Errors.....	89
Figure 61 — Write Parity Errors with $PL = 2$	91
Figure 62 — Write Parity Alignment with $PL = 2$	92
Figure 63 — Write Parity Alignment with $PL = 4$	92
Figure 64 — Read Parity Alignment with $PL = 2$	93
Figure 65 — Read Parity Alignment with $PL = 4$	93
Figure 66 — Example Signal Paths with Lane Repair	100
Figure 67 — MISR Features Block Diagram of HBM3.....	101
Figure 68 — Example of 4 bit MISR-LFSR implementing $f(x) = X^4 + X^3 + 1$	102
Figure 69 — AWORD MISR Modes Preamble Clock Filter Behavior.....	107
Figure 70 — DWORD Write MISR Modes Behavior	108
Figure 71 — DWORD Read LFSR Modes Behavior	112
Figure 72 — LFSR Compare Mode Block Diagram.....	113
Figure 73 — On-die ECC Overview Diagram Example	115
Figure 74 — ECS operation timing.....	118
Figure 75 — ECS CEs Output Enable Timing for SEV Signaling	121
Figure 76 — The Block Diagram of On-die ECC Engine and Path for ECC Engine Test Mode	122
Figure 77 — Timing Diagram of ECC Engine Test Mode	124
Figure 78 — Oscillator offset ($WOSC_{offset(V)}$)	127
Figure 79 — Oscillator offset ($WOSC_{offset(T)}$)	128
Figure 80 — Duty Cycle Adjuster Range	130

Contents (cont'd)

Figure 81 — Relationship Between WDQS Waveform and DCA Code Change (Example).....	131
Figure 82 — Example Sequence for WDQS Duty Cycle Correction	133
Figure 83 — Self Repair Flowchart	137
Figure 84 — DQ Receiver Mask.....	141
Figure 85 — Across Pin V_{REFD} Voltage Variation.....	141
Figure 86 — DQ to WDQS Timings ($t_{WDQS2DQ_I}$, $t_{DQ2DQtra_I}$ and $t_{DQ2DQter_I}$) at DRAM Pins Referenced from the Internal Latch.....	143
Figure 87 — Read Data Timing Definitions of $t_{DQ2DQtra_O}$, $t_{DQ2DQter_O}$, and $t_{DQSQtra_O}$	144
Figure 88 — CA Single Pulse Amplitude and Pulse Width	145
Figure 89 — CK Single Pulse	146
Figure 90 — Differential Input Slew Rate Definition for WDQS_t, WDQS_c	146
Figure 91 — Timing Reference Load	147
Figure 92 — Output Rise and Fall Definition.....	148
Figure 93 — Overshoot, Undershoot Definition.....	149
Figure 94 — Measurement Setup for IDD and IPP Measurements	151
Figure 95 — Staggered MicroBump Pattern	169
Figure 96 — MicroBump Pillar Diameter	169
Figure 97 — DA Port Connection Diagram For Multiple HBM3 DRAM Devices.....	202
Figure 98 — IEEE Std. 1500 Logic Diagram	204
Figure 99 — WIR Channel Select Logic Diagram	204
Figure 100 — IEEE1500 Port Operation	205
Figure 101 — RESET_n and HBM_RESET Logic	215
Figure 102 — Registers Associated with Lane Repair Instructions.....	235
Figure 103 — Channel Disable Instruction.....	236
Figure 104 — Example Channel Configuration 1	239
Figure 105 — Example Channel Configuration 2	239
Figure 106 — IEEE1500 Port Input and Output Timings.....	250
Figure 107 — IEEE1500 EXTEST_RX and EXTEST_TX Instruction Related Timings.....	250
Figure 108 — IEEE1500 SOFT_REPAIR and HARD_REPAIR Instruction Related Timings.....	250
Figure 109 — IEEE1500 Soft_Lane_Repair And Hard_Lane_Repair Instruction Related Timings	251
Figure 110 — IEEE1500 DWORD_MISR / AWORD_MISR Instruction Related Timings	251
Figure 111 — IEEE1500 CHANNEL_ID Instruction Related Timings.....	251
Figure 112 — IEEE1500 MODE_REGISTER_DUMP_SET Instruction Related Timings	252

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HIGH BANDWIDTH MEMORY (HBM3) DRAM

(From JEDEC Board Ballot JCB-22-56, formulated under the cognizance of the JC-42.2 Subcommittee on DRAM Memories, item number 1837.98A).

1 Scope

The HBM3 DRAM is tightly coupled to the host compute die with a distributed interface. The interface is divided into independent channels. Each channel is completely independent of one another. Channels are not necessarily synchronous to each other. The HBM3 DRAM uses a wide-interface architecture to achieve high-speed, low power operation. Each channel interface maintains a 64 bit data bus operating at double data rate (DDR).

2 Features

- 256 bit prefetch per memory read and write access
- BL = 8
- 64 DQ width + ECC/SEV pins support / channel
- Pseudo Channel (PC) mode operation; 32 DQ width for PC mode
- Differential clock inputs (CK_t/CK_c) for command/address
- Double data rate (DDR) command/address. Row Activate commands require one-and-a-half-cycle, all other row commands require a half-cycle except for PDE, SRE with one cycle. Column command require only one cycle
- Semi-independent row and column command interfaces allowing Activates/Precharges to be issued in parallel with Read/Writes
- Data referenced to unidirectional differential data strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c. One strobe pair each per DWORD
- Up to 16 channels / device
- Channel density of 2 Gb to 32 Gb
- 16, 32, 48, or 64 banks per channel; varies by device density / channel
- Bank grouping supported
- 1 KB page size per pseudo channel (PC)
- DBIac support configurable via MRS
- Self refresh modes
- I/O voltage 1.1 V, Tx driver voltage 0.4 V
- DRAM core voltage 1.1 V, independent of I/O voltage
- Unterminated data/address/command/clock interfaces
- Unmatched data interfaces
- Temperature sensor with 2-bit encoded range output

3 Organization

The HBM3 DRAM is optimized for high-bandwidth operation to a stack of multiple DRAM devices across a number of independent interfaces called channels. It is anticipated that each DRAM stack will support up to 16 channels. Figure 1 shows an example stack containing 4 DRAM dies, each die supporting 4 channels. Each die contributes additional capacity and additional channels to the stack (up to a maximum of 16 channels per stack).

Each channel provides access to an independent set of DRAM banks. Requests from one channel may not access data attached to a different channel. Channels are independently clocked, and need not be synchronous.

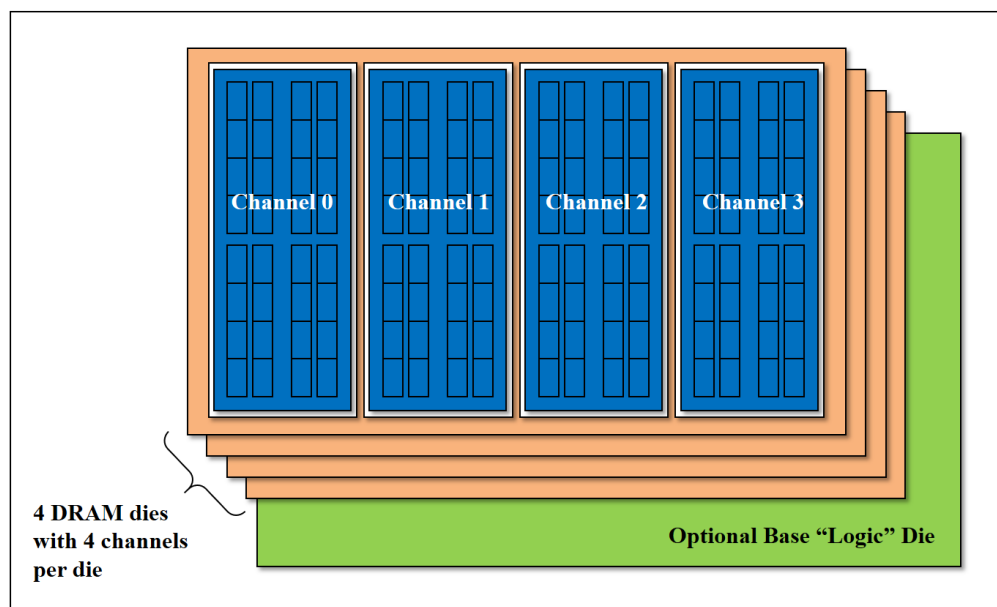


Figure 1 — General Overview of a DRAM Die Stack with Channels

The DRAM vendor may choose to require an optional interface die that sits at the bottom of the stack and provides signal redistribution and other functions. The vendor may choose to implement many of the logic functions typically found on DRAM die on this logic die. This standard does not explicitly require nor prohibit such a solution.

The division of channels among the DRAM dies within a stack is left to the vendor. Figure 1, with the memory for four channels implemented on each die, is not a required organization. Organizations are permitted where the memory for a single channel is distributed among multiple dies; however, all accesses within a single channel must have the same latency for all accesses. Similarly, vendors may develop products where each memory die can flexibly support 1, 2, 4 or 8 channels – enabling 16-channel configurations with stacks of 4 to 16 dies while keeping all data for a given channel on one die.

Since each channel is independent, much of this standard will describe a single channel. Where signal names are involved, families of signals belonging to a given channel will have the suffix a, b, ..., p for channels a through p. If no suffix is present, the signal(s) being described are generic instances of the various per-channel signals.

3.1 Channel Definition

Each channel consists of an independent command and data interface. RESET_n, IEEE1500 test port and power supply signals are common to all channels. A channel provides access to a discrete pool of memory; no channel may access the memory storage for a different channel. Each channel interface provides an independent interface to a number of banks of DRAM of a defined page size. See Channel Addressing.

3.1.1 Summary of Per-Channel Signals

Table 1 outlines the signals required for each channel, and Table 2 adds global signals that are required once per HBM3 device.

Table 1 — Single Channel Signal Count

Function	Number of Microbumps	Notes
Data	64	DQ[63:0]
Column command/ Address	8	C[7:0]
Row command/ Address	10	R[9:0]
DBI	8	1 DBI per 8 DQs
ECC	4	2 ECC per 32 DQs
SEV	4	2 SEV per 32 DQs
DPAR	2	1 PAR per 32 DQs
APAR	1	1 PAR per AWORD
DERR	2	1 DERR per 32 DQs
Strobe	8	1 RDQS_t/RDQS_c, WDQS_t/WDQS_c per 32 DQs
Clock	2	CK_t/CK_c
AERR	1	AERR per AWORD
Redundant Data	4	RD[3:0]
Redundant Address	1	Redundant row/ column
RFU	1	1 RFU per AWORD
Total	120	

Table 2 — Global Signal Count

Function	Number of Microbumps	Description	Notes
Reset	2	RESET_n	1
Temp	2	TEMP[1:0]	
WRCK	2	IEEE1500 Clock	1
WRST_n	2	IEEE1500 Reset	1
WSI	2	IEEE1500 Serial Input	1
SelectWIR	2	IEEE1500 Select WIR	1
CaptureWR	2	IEEE1500 Capture WR	1
ShiftWR	2	IEEE1500 Shift WR	1
UpdateWR	2	IEEE1500 Update WR	1
WSO	32	2 IEEE1500 Serial Output Per Channels[a:p]	1
CATTRIP	2	Catastrophic Temperature Sensor	1
Total	52		2
NOTE 1 Duplicate microbumps for link redundancy			
NOTE 2 Excluding MRFU[1:0] from count			

3.1.2 Pseudo Channel

Pseudo channel (PC) divides a channel into two individual sub-channels of 32 bit I/O each, providing 256 bit prefetch per memory read and write access for each pseudo channel.

Both pseudo channels operate semi-independent: they share the channel's row and column command bus as well as CK and R0 inputs, but decode and execute commands individually as illustrated in Figure 2. Address PC is used to direct commands to either to pseudo channel 0 (PC = 0) or pseudo channel 1 (PC = 1). Power-down and self refresh are common to both pseudo channels.

Array access timings as listed in the table below are applicable for each individual pseudo channel. For example, an ACTIVATE to PC0 can be followed by an ACTIVATE to PC1 as shown in Figure 2. However a subsequent ACTIVATE to PC0 can only be done after t_{RRD} (PC0). For commands that are common to both pseudo channels (PDE, PDX, SRE, SRX and MRS) it is required that the respective timing conditions are met by both pseudo channels when issuing that command. Both pseudo channels also share the channel's mode registers.

All I/O signals of DWORD0 are associated with pseudo channel 0, and all I/O signals of DWORD1 with pseudo channel 1.

Table 3 — Array Access Timings Counted Individually Per Pseudo Channel

Array Timing Group	Notes
Row Access Timings	t_{RC} , t_{RAS} , t_{RCDRD} , t_{RCDWR} , t_{RRDL} , t_{RRDS} , t_{FAW} , t_{RTP} , t_{RP} , t_{WR}
Column Access Timings	t_{CCDL} , t_{CCDS} , t_{CCDR} , t_{WTRL} , t_{WTRS} , t_{RTW}
Refresh Timings	t_{RFC} , t_{RFCPB} , t_{RREFD} , t_{REFI} , t_{REFIPB} , t_{RTW}

3.2 Channel Addressing

Table 4 — HBM3 Channel Addressing

Density per Channel	2 Gb	4 Gb	6 Gb	8 Gb			Note
Density per PC	1 Gb	2 Gb	3 Gb	4 Gb			
Prefetch Size per PC (bits)	256	256	256	256			1, 2
Row Address	RA[12:0]	RA[13:0]	RA[14:0] ⁶	RA[14:0]			
Column Address	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]			
Bank Address	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]			
Page Size per PC	1 KB	1 KB	1 KB	1 KB			3
Refresh Period	3.9 μ s	3.9 μ s	3.9 μ s	3.9 μ s			
Density Code	0000	0100	1000	1100			8
Configuration⁴	8 Gb	8 Gb	8 Gb	16 Gb	16 Gb	16 Gb	Note
	8High	12High	16High	8High	12High	16High	
Density per Channel	4 Gb	6 Gb	8 Gb	8 Gb	12 Gb	16 Gb	
Density per PC	2 Gb	3 Gb	4 Gb	4 Gb	6 Gb	8 Gb	
Prefetch Size per PC (bits)	256	256	256	256	256	256	1, 2
Row Address	RA[12:0]	RA[12:0]	RA[12:0]	RA[13:0]	RA[13:0]	RA[13:0]	
Column Address	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	
Bank Address	SID, BA[3:0]	SID[1:0] ⁷ , BA[3:0]	SID[1:0], BA[3:0]	SID, BA[3:0]	SID[1:0] ⁷ , BA[3:0]	SID[1:0], BA[3:0]	5
Page Size per PC	1 KB	1 KB	1 KB	1 KB	1 KB	1 KB	3
Refresh Period	3.9 μ s	3.9 μ s	3.9 μ s	3.9 μ s	3.9 μ s	3.9 μ s	
Density Code	0001	0010	0011	0101	0110	0111	8
Configuration⁴	24 Gb	24 Gb	24 Gb	32 Gb	32 Gb	32 Gb	Note
	8High	12High	16High	8High	12High	16High	
Density per Channel	12 Gb	18 Gb	24 Gb	16 Gb	24 Gb	32 Gb	
Density per PC	6 Gb	9 Gb	12 Gb	8 Gb	12 Gb	16 Gb	
Prefetch Size per PC (bits)	256	256	256	256	256	256	1, 2
Row Address	RA[14:0] ⁶	RA[14:0] ⁶	RA[14:0] ⁶	RA[14:0]	RA[14:0]	RA[14:0]	
Column Address	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	
Bank Address	SID, BA[3:0]	SID[1:0] ⁷ , BA[3:0]	SID[1:0], BA[3:0]	SID, BA[3:0]	SID[1:0] ⁷ , BA[3:0]	SID[1:0], BA[3:0]	5
Page Size per PC	1 KB	1 KB	1 KB	1 KB	1 KB	1 KB	3
Refresh Period	3.9 μ s	3.9 μ s	3.9 μ s	3.9 μ s	3.9 μ s	3.9 μ s	
Density Code	1001	1010	1011	1101	1110	1111	8

NOTE 1 Prefetch size and page size reflect the effective addressing along with row and column commands. Both do not include the optional ECC bits as described in Section 3.1.

NOTE 2 The burst order is fixed for Reads and Writes, and the HBM device does not assign column address bits to distinguish between the eight UI of a BL8 burst. A memory controller may internally assign such column address bits but those column address bits are not transmitted to the HBM device.

NOTE 3 Page Size = $2^{\text{COLBITS}} * (\text{Prefetch Size} / 8)$; where COLBITS is the number of column address bits. Page size and prefetch size per pseudo channel in Pseudo Channel. MSB of RA is used to select half of open 2 KB page.

NOTE 4 These configurations are optimized for HBM stacks using 8 or 12 or 16 DRAM dies. The stack height of all other configuration is vendor specific.

NOTE 5 SID, SID0, SID1 act as bank address bits in command execution. Specific AC timing parameters or variations on selected timing parameters may be linked to SID. Table 29 and Table 30 and the vendor data sheets should be consulted for details.

NOTE 6 RA[14:13] = 11 is invalid.

NOTE 7 SID[1:0] = 11 is invalid.

NOTE 8 The density code refers to the encoding of per-channel density in DEVICE_ID Wrapper Data Register, bits[27:24].

3.2.1 Bank Groups

The banks within a device are divided into 4 or 8 or 12 or 16 bank groups. The assignment of banks to bank groups is shown in Table 5.

Different timing parameters are specified depending on whether back-to-back accesses are within the same bank group or across bank groups as shown in Table 6.

Table 5 — Bank Group Assignments

Banks	16 Banks BA[3:0]	32 Banks SID, BA[3:0]	48 Banks SID[1:0], BA[3:0]	64 Banks SID[1:0], BA[3:0]
0 and 3	Group A	Group A	Group A	Group A
4 and 7	Group B	Group B	Group B	Group B
8 to 11	Group C	Group C	Group C	Group C
12 to 15	Group D	Group D	Group D	Group D
16 to 19	N/A	Group E	Group E	Group E
20 to 23		Group F	Group F	Group F
24 to 27		Group G	Group G	Group G
28 to 31		Group H	Group H	Group H
32 to 35		N/A	Group I	Group I
36 to 39			Group J	Group J
40 to 43			Group K	Group K
44 to 47			Group L	Group L
48 to 51	N/A	N/A	N/A	Group M
52 to 55				Group N
56 to 59				Group O
60 to 63				Group P

Table 6 — Command Sequence Affected by Bank Groups

Command Sequence	Corresponding Ac Timing Parameter		Notes
	Accesses To Different Bank Groups	Accesses Within Same Bank Group	
ACTIVATE to ACTIVATE	t_{RRDS}	t_{RRDL}	
WRITE to WRITE	t_{CCDS}	t_{CCDL}	
READ to READ	t_{CCDS} or t_{CCDR}	t_{CCDL}	
Internal WRITE to READ	t_{WTRS}	t_{WTRL}	
READ to PRECHARGE	-	t_{RTP}	1
NOTE 1 Parameters t_{RTP} applies only when READ and PRECHARGE go to the same bank.			
NOTE 2 Parameters t_{CCDR} replaces parameter t_{CCDS} when consecutive READs go to banks with different stack IDs (SID).			

3.3 Simplified State Diagram

The state diagram provides a simplified illustration of the allowed state transitions and the related commands to control them. The following operations are either not shown or not fully shown in the diagram:

- state transitions involving more than one bank;
- interactions from the use of IEEE1500 instructions to load mode registers or execute test functions;
- the immediate transition from any state to reset state by asserting RESET_n LOW or by loading the IEEE1500 instructions HBM_RESET;
- the ECS and ECC Engine Test Mode operation;
- DCA and DCM;
- Loopback Test Mode;
- WDQS-to-CK Alignment Training

For a complete description of the device behavior, use the information provided in the state diagram along with the command truth tables and AC timing specifications.

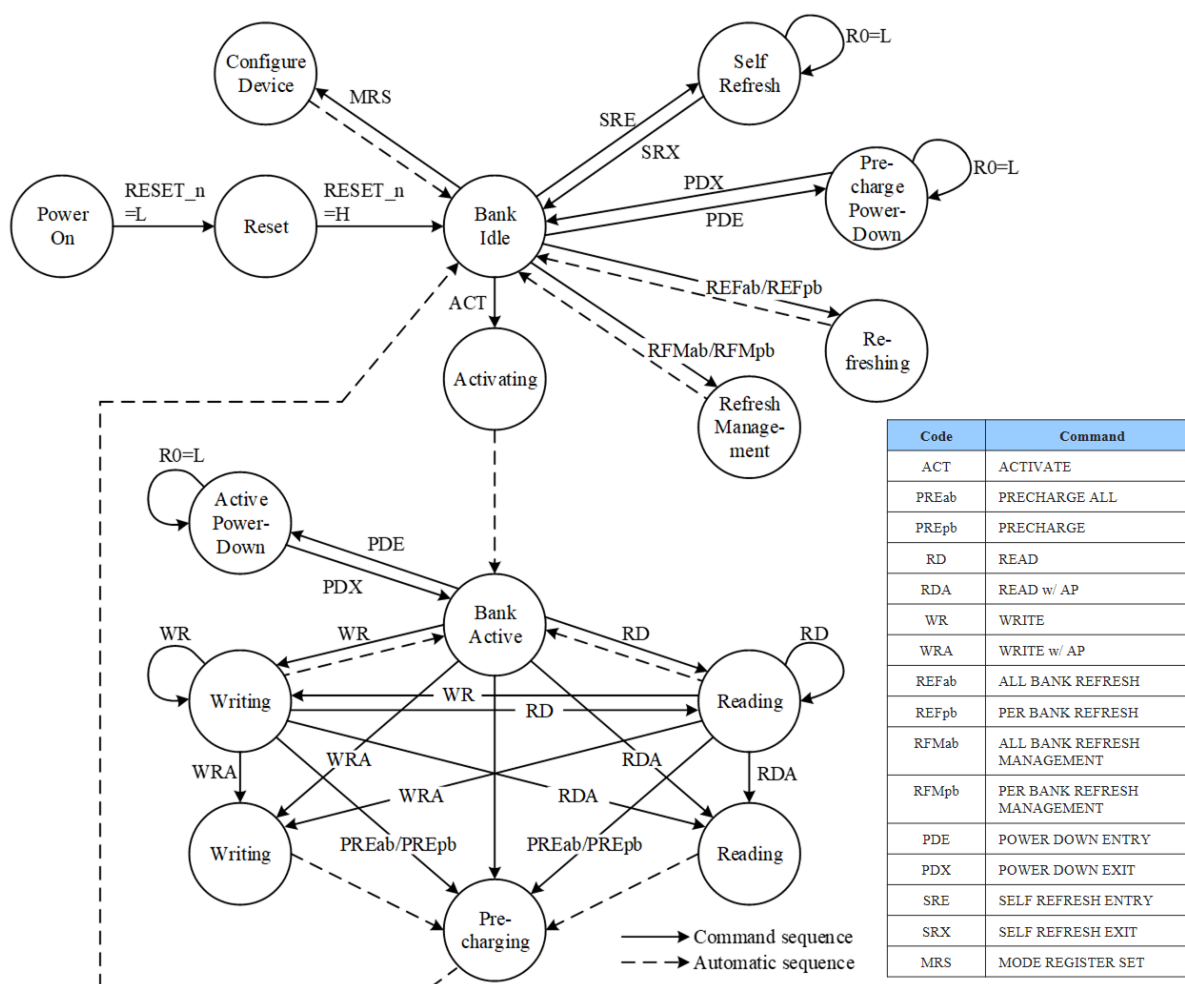


Figure 3 — Simplified State Diagram

4 Initialization

To power-up and initialize the HBM3 device into functional operation, the sequence in clause 4.1 must be followed. At any time after the power-up initialization, the HBM3 device may be reset using the sequence in clause 4.3. A limited set of IEEE 1500 port instructions may be used within the initialization sequences, as described in clause 4.3.

The interactions between HBM3 functional reset and the IEEE 1500 port reset are as follows (also see clause 13.2):

- Functional reset requires that the IEEE 1500 port also be reset.
- The IEEE 1500 port can be reset at any time without impacting normal operation.
- The IEEE 1500 port may be brought out of reset and a limited set of instructions may be used after a minimum time after RESET_n has been deasserted. See clause 4.3.
- If not needed, the IEEE 1500 port may be left in reset (WRST_n = LOW) during normal operation.

4.1 HBM3 Power-up and Initialization Sequence

HBM3 device must be powered up and initialized in a predefined manner. The following sequence and timing must be satisfied for HBM3 power up and initialization sequence. Also refer to Figure 4.

1. Apply power to the V_{DDC} , V_{DDQ} , V_{DDQL} and V_{PP} supplies following the requirements in the Power Ramp Conditions table. V_{PP} must ramp at the same time or earlier than V_{DDC} and V_{DDQ} . V_{DDC} and V_{DDQ} must ramp simultaneously under the same level. V_{DDC} and V_{DDQ} must ramp at the same time or earlier than V_{DDQL} . During power supply ramp time t_{INIT0} , RESET_n, WRST_n and all other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z). After T_a in Figure 4 is reached, V_{DDC} and V_{DDQ} must be greater than $V_{DDQL}-200$ mV.
2. RESET_n and WRST_n must be driven LOW (below $0.2 \times V_{DDQ}$) before or at the same time when t_{INIT0} expires as shown in Figure 4 (time T_a). All other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z) at this point. RESET_n must be maintained LOW for a minimum of t_{INIT1} time with stable power. After t_{INIT6} time has elapsed, the HBM3 device drives RDQS_t and RDQS_c to LOW and HIGH static levels, respectively, and AERR, DERR and CATTRIP signals to LOW.
3. A time t_{INIT2} before RESET_n is pulled HIGH, CK_t and CK_c must be driven to static LOW and HIGH levels, respectively.
4. After RESET_n is driven HIGH, R[3:0] must be driven to PDE state (HIGH, LOW, HIGH, LOW) and C[2:0] must be driven to CNOP state (HIGH, HIGH, HIGH) for a t_{INIT7} time before CK clock is toggled. R[9:4] and C[7:3] are allowed to remain in an undefined state. The HBM3 device resets into the precharged power-down state. During t_{INIT3} , the HBM3 device will read and apply internal fuse configuration data and perform I/O driver impedance calibration. At the same time the WRST_n signal may be optionally driven HIGH to enable a subset of the IEEE 1500 instructions (see Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs and IEEE Standard 1500 clauses). In that case, all other IEEE1500 inputs (WRCK, SelectWIR, ShiftWR, CaptureWR, UpdateWR, WSI) must be driven per IEEE1500 Port Input and Output Timings figure at time t_{WINIT2} before WRST_n is pulled HIGH (see IEEE1500 Test Port AC Timing Parameters). CATTRIP data must stay LOW from the end of t_{INIT6} to the end of t_{INIT3} and valid data must start after t_{INIT3} .

4.1 HBM3 Power-up and Initialization Sequence (cont'd)

5. While R[3:0] and C[2:0] remain driven to PDE state as defined in step 4, the CK clock shall be started and stable clocks shall be maintained for minimum of t_{INIT4} time before driving R[3:0] HIGH. Since R[0] of R[3:0] is a synchronous signal, the corresponding setup time to clock (t_{IS}) must be met. Also, RNOP and CNOP commands must be registered (with t_{IS} / t_{IH} satisfied). After R[3:0] are registered HIGH, a minimum t_{INIT5} time must be satisfied before issuing a first MRS command. At or before the time that R[3:0] are driven HIGH, WDQS_t and WDQS_c must be driven to LOW and HIGH static levels, respectively. A stable CK clock shall be maintained except when a channel is in power-down or self refresh state. See Power-Down and Self Refresh clauses for conditions about stopping and re-starting the CK clock.
6. Issue all MRS commands to configure the HBM3 device appropriately for the application setting.
7. The HBM3 device is now ready for normal operation.

Table 7 — Initialization Timing Parameters

Symbol	Description	Min	Max	Unit
t_{INIT0}	Power supply ramp time	0.01	200	ms
t_{INIT1}	RESET_n signal LOW time at power-up (after stable power)	200		μs
t_{INIT2}	CK_c and CK_t must be driven to HIGH and LOW before RESET_n deassertion	10		ns
t_{INIT3}	Precharged power-down state and WRST_n LOW time after RESET_n deassertion	4		ms
t_{INIT4}	CK clock stable time before R[3:0] HIGH	10		nCK
t_{INIT5}	Idle time before first MRS command	200		ns
t_{INIT6}	RDQS_t, RDQS_c driven valid and AERR, DERR and CATTRIP driven LOW after RESET_n assertion		100	ns
$t_{\text{PW_RESET}}$	RESET_n signal LOW time with stable power	1		μs
t_{INIT7}	R[3:0] and C[2:0] must be driven to PDE and CNOP before CK clock toggling	2		nCK

Table 8 — Power Ramp Conditions

After	Application Condition
T_0	V_{PP} must be greater than V_{DDC} , V_{DDQ}
	V_{DDC} and V_{DDQ} must be greater than $V_{\text{DDQL}} - 200 \text{ mV}$
NOTE 1 T_0 is the point when any power supply first reaches 300 mV NOTE 2 Voltage ramp conditions in this table apply between T_0 and controlled power-off. NOTE 3 T_a is the point at which all supply voltages are within their defined ranges. NOTE 4 Power ramp duration t_{INIT0} ($T_a - T_0$) must not exceed 200 ms.	

4.1 HBM3 Power-up and Initialization Sequence (cont'd)

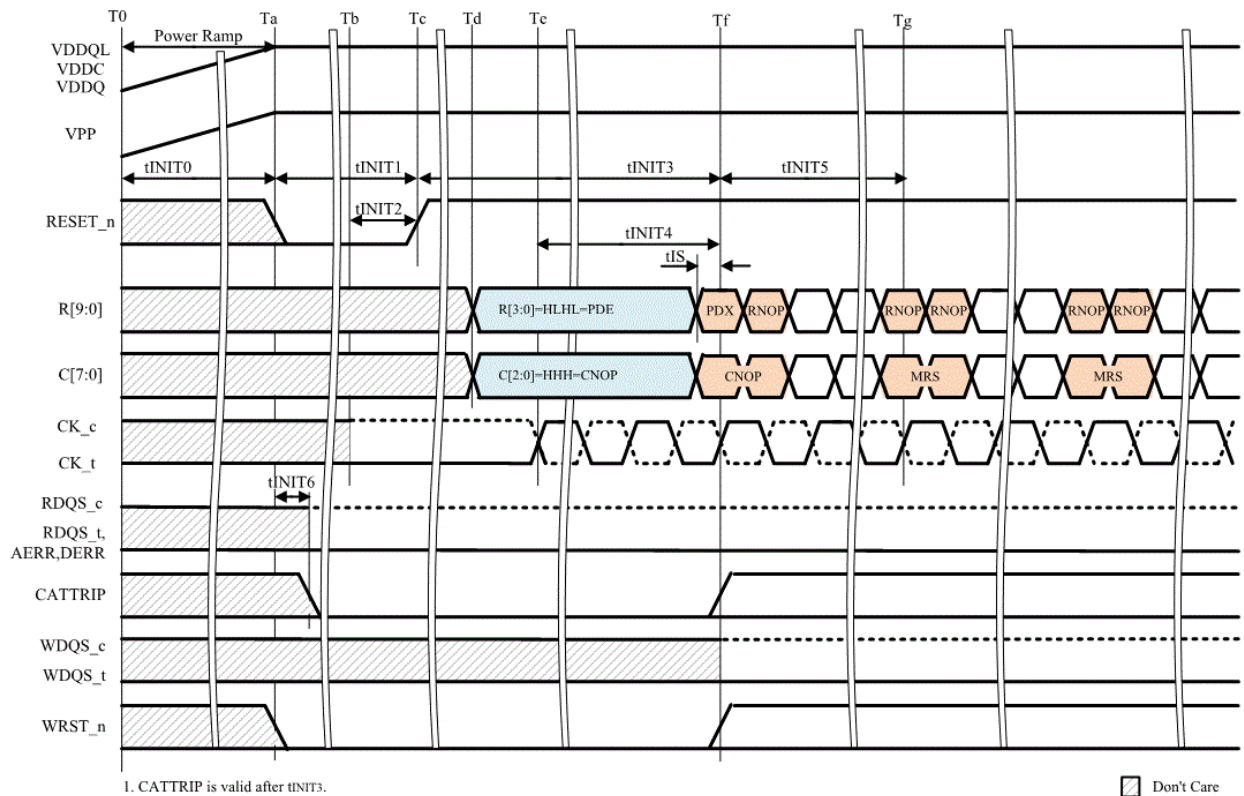


Figure 4 — Power-up and Initialization

4.2 Controlled Power-off Sequence

For a controlled power-off, the conditions in Table 9 must be met.

While powering off, all input levels must be between VSS and VDDQ or VDDQL during voltage ramp to avoid latch-up.

Table 9 — Power Supply Conditions

Between	Application Condition
T _x and T _z	V _{PP} must be greater than V _{DDC} , V _{DDQ}
	V _{DDC} and V _{DDQ} must be greater than V _{DDQL} – 200 mV
NOTE 1 T _x is the point where any power supply drops below the minimum value specified.	
NOTE 2 T _z is the point where all power supplies are below 300 mV. After T _z , the HBM3 device is powered off.	

4.3 Initialization Sequence with Stable Power

Steps 1 and 2 must be satisfied to perform a functional reset when power is kept stable at the HBM3 DRAM. See Figure 5.

1. RESET_n must be driven LOW anytime when a functional reset is needed. All other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z) at this point except WRST_n and CATTRIP as shown in Figure 5. RESET_n must be maintained LOW for a minimum of t_{PW_RESET} . R[3:0] must be driven to PDE state (HIGH, LOW, HIGH, LOW) and C[2:0] must be driven to CNOP state (HIGH, HIGH, HIGH) for a t_{INIT7} time before CK clock is toggled. R[9:4] and C[7:3] are allowed to remain in an undefined state. Alternately, the IEEE 1500 port HBM3_RESET instruction may be used to perform a re-initialization, with RESET_n continuing to be driven HIGH. Refer to HBM_RESET clause.
2. Follow steps 3 to 6 as described in clause HBM3 Power-up and Initialization Sequence. Note that the CATTRIP output is sticky and not cleared by a functional reset.

A time t_{INIT2} before RESET_n is pulled HIGH, CK_t and CK_c must be driven to static LOW and HIGH levels, respectively. See step 3 of the HBM3 Power-up and Initialization Sequence.

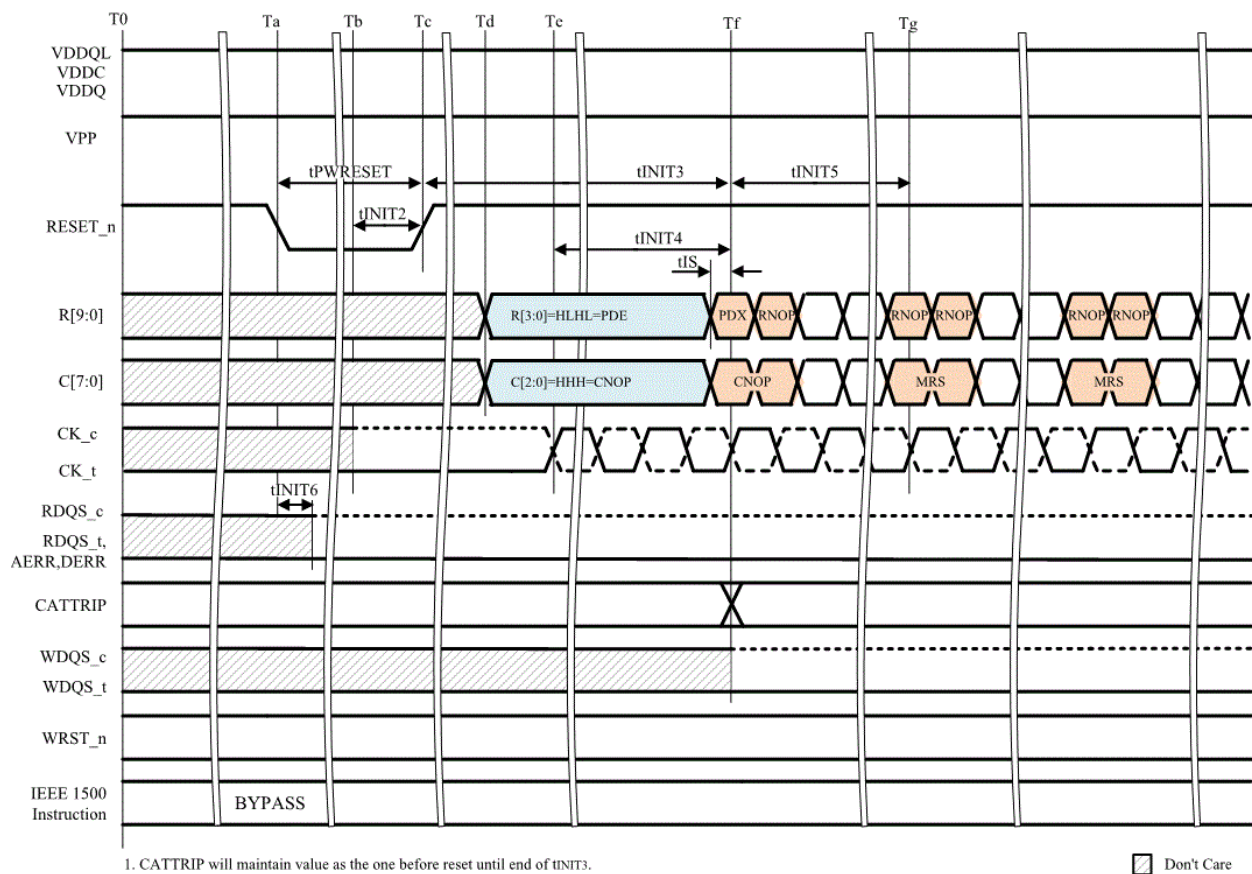


Figure 5 — HBM3 RESET and Initialization Sequence with Stable Power

4.4 Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs and Channel Disable

All IEEE 1500 port instructions are allowed after t_{INIT3} without completing the full initialization sequence.

NOTE 1 After EXTEST operations, another RESET_n toggle may be required.

NOTE 2 R[9:0] and C[7:0] mean logical pin name because those pin's physical location will be changed after soft or hard lane repair.

Figure 6 illustrates usage of the EXTEST and SOFT_LANE_REPAIR instructions and Figure 7 the usage of the CHANNEL_DISABLE instruction within the initialization sequence. These sequence may be applied as part of the power-up or stable-power initialization sequence to check for and correct failed connections on the row and column command buses, which must be correctly driven to RNOP and CNOP as part of this initialization sequence. It may also be used to disable a channel before normal operation mode is entered. DWORD lane repairs are also allowed.

1. At time T_a , RESET_n and WRST_n must be driven LOW.
2. After a minimum time t_{INIT1} (if during an initial power-up sequence) or after t_{PW_RESET} (if during a stable power initialization sequence) RESET_n shall be driven HIGH. t_{INIT2} must also be met.
3. After t_{INIT3} , WRST_n is driven HIGH. IEEE 1500 port instructions may now be used. (Note that the WRST_n low pulse width t_{WRSTL} is met since t_{WRSTL} is less than the t_{INIT1} or t_{PW_RESET}). Refer to IEEE1500 Test Port AC Timing Parameters for timing requirements for operating the IEEE 1500 port, including t_{SWRST} . At this point, a defective channel may be disabled; also, defective lane detection and soft lane repair may be executed. EXTEST operations may be applied to identify lanes needing repair. If soft lane repair is needed, SOFT_LANE_REPAIR and HARD_LANE_REPAIR operations can be applied after another RESET_n toggle, which is required after EXTEST instruction operation. An IEEE 1500 port BYPASS instruction should be applied to return all HBM3 signals to their normal functional mode after SOFT_LANE_REPAIR operations. Alternately, WRST_n may be driven LOW.
4. The initialization sequence may then continue per steps 4 to 6 of HBM3 Power-up and Initialization Sequence, as needed.

During the t_{INIT3} period before WRST_n is driven HIGH, the HBM3 device executes various internal configuration operations, including applying hard lane repairs based on previously fused data. Executing soft lane repair instructions after t_{INIT3} overwrites any previously programmed hard lane repair data. It is suggested that the hard lane repair data is read from the HBM3 device and merged in any new lane repairs before applying the new soft lane repair operations. Any applicable IEEE 1500 port instructions timings must be met before continuing to time point T_h , such as t_{SLREP} if a SOFT_LANE_REPAIR instruction has been applied.

The EXTEST instructions are not required before applying the soft lane repair(s). Previously determined needed lane repairs may be applied as part of each initialization event.

A time t_{INIT2} before RESET_n is pulled HIGH, CK_t and CK_c must be driven to static LOW and HIGH levels, respectively. See step 3 of the HBM3 Power-up and Initialization Sequence.

R[3:0] must be driven PDE state and C[2:0] must be driven CNOP state for a t_{INIT7} time.

4.4 Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs and Channel Disable (cont'd)

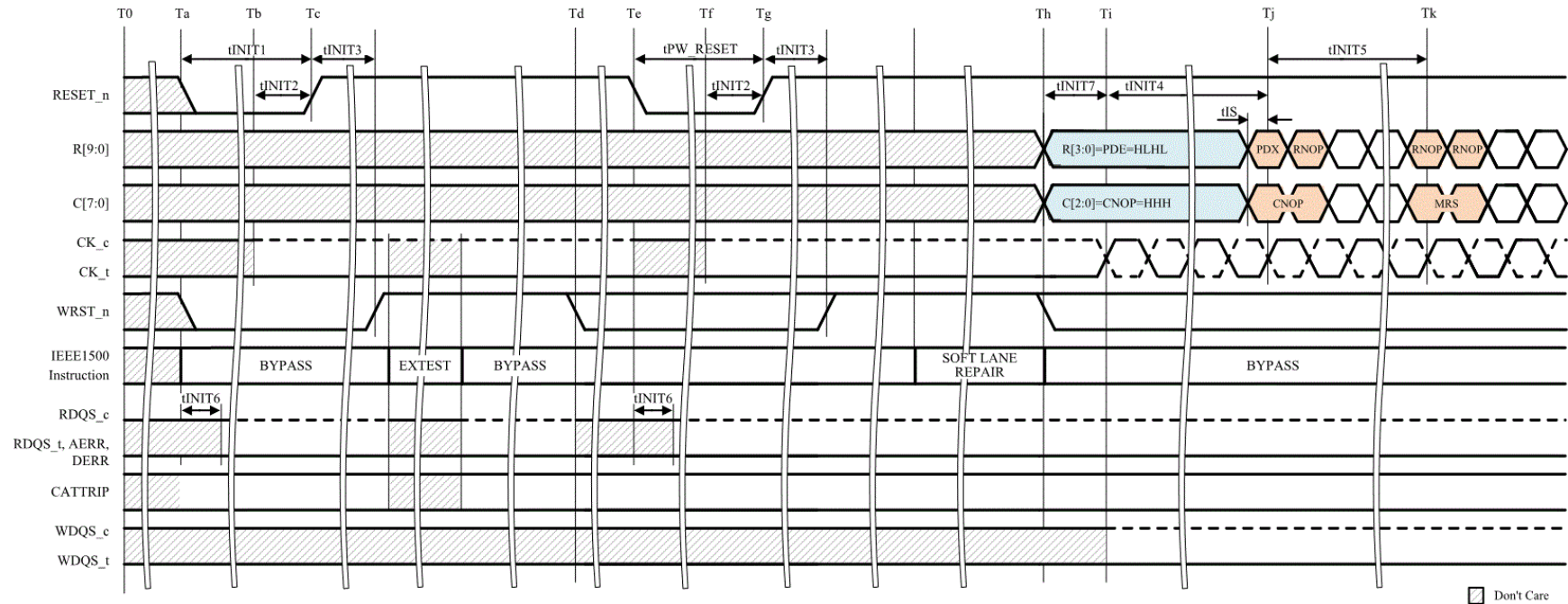
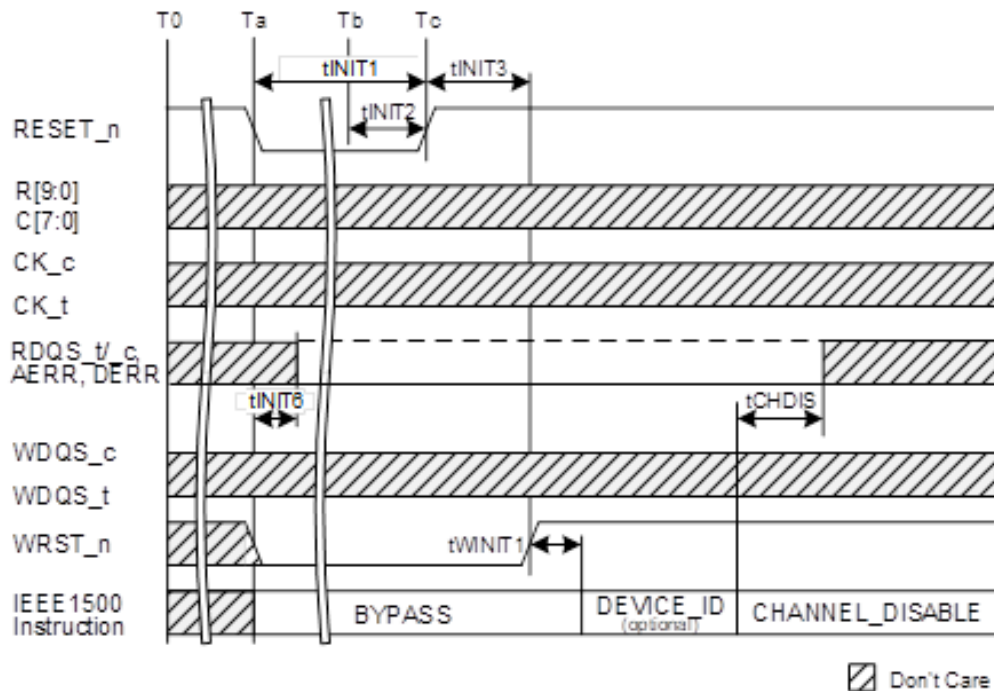


Figure 6 — Initialization Sequence with Lane Repair or Channel Disable

4.4 Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs and Channel Disable (cont'd)



NOTE 1 A disabled channel will turn off all AWORD and DWORD input and output buffers including CK_t/CK_c and WDQS_t/WDQS_c inputs, thus allowing all external signals to float. The CK clock is allowed to be High-Z throughout this initialization sequence.

Figure 7 — Initialization Sequence with Channel Disable

5 Mode Registers

The Mode Registers define the specific mode of operation for the HBM3 DRAM. Sixteen 8-bit wide Mode Registers (MR0 to MR15) are defined as in Table 11 through Table 27. MR10 and MR12 are special mode register and reserved for vendor specific features. Mode Registers are common to both pseudo channels (PC0 and PC1). Reprogramming the Mode Registers does not alter the contents of the memory array.

Mode Registers are programmed via the MODE REGISTER SET (MRS) command and retain the stored information until they are reprogrammed, chip reset, or until the device loses power. Mode Register can also be programmed via the IEEE1500 instruction MODE_REGISTER_DUMP_SET; this instruction can also be used to retrieve the Mode Register content.

Mode Registers must be loaded when all banks are idle and the time t_{RDMRS} from a preceding READ command has elapsed. The controller must wait the specified time t_{MOD} before initiating any subsequent operations. Violating either of these requirements will result in unspecified operation.

No default states are defined for Mode Registers except when otherwise noted. Users therefore must fully initialize all Mode Registers to the desired values upon power-up or after a subsequent chip reset.

When an entire Mode Register is marked as RFU (“Reserved for future use”), then it is considered as not supported by the HBM3 DRAM, and its content is Don’t Care. Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits in these registers must be programmed to 0.

5 Mode Registers (cont'd)

Table 10 — HBM3 Mode Register Overview

Mode Register		OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
	MA[4:0] ¹								
MR0 (Table 11)	00000	Test Mode (TM)	CA Parity (CAPAR)	Write Parity (WPAR)	Read Parity (RPAR)	RFU	TCSR	Write DBI (WDBI)	Read DBI (RDBI)
MR1 (Table 12)	00001	Parity Latency (PL)			Write Latency (WL)				
MR2 (Table 13)	00010	Read Latency (RL)							
MR3 (Table 14)	00011	Write Recovery for Auto Pre-charge (WR)							
MR4 (Table 15)	00100	Activate to Precharge (RAS)							
MR5 (Table 16)	00101	RFU				Read to Auto Precharge (RTP)			
MR6 (Table 17)	00110	RFU		Pullup Driver Strength			Pulldown Driver Strength		
MR7 (Table 18)	00111	CATTRIP	RFU	DWORD MISR Control			RFU	DWORD Read Mux Control	DWORD Loopback
MR8 (Table 20)	01000	RFU		RFM Levels (RFML)		WDQS-to-CK Training (WDQS2CK)	ECS error log auto reset (ECSLOG)	Duty Cycle Monitor (DCM)	DA Port Lockout
MR9 (Table 21)	01001	ECS error Type and Address Reset (ECSRES)	ECS Multi-bit Error Correction (ECSCM)	Auto ECS during Self Refresh (ECSSRF)	Auto ECS via REFab (ECSREF)	Error Vector Pattern (ECCVEC)	Error Vector Input Mode (ECCTM)	Severity Reporting (SEVR)	Meta Data (MD)
MR10 (Table 22)	01010	Reserved for Vendor Specific Features							
MR11 (Table 23)	01011	DCA code for WDQS1 (PC1)				DCA code for WDQS0 (PC0)			
MR12 (Table 24)	01100	Reserved for Vendor Specific Features							
MR13 (Table 25)	01101	RFU							
MR14 (Table 26)	01110	RFU	Reference Voltage for AWORD inputs (VREFCA)						RFU
MR15 (Table 27)	01111	RFU	Reference Voltage for DWORD inputs (VREFD)						RFU
NOTE 1 MA4 is a valid mode register address bit that must be set to 0 for the mode registers defined in this table.									

5 Mode Registers (cont'd)

Table 11 — Mode Register 0 (MR0)

Field	Bits	Description	Notes
Test Mode (TM)	OP7	0 – Normal Operation (Default) 1 – Test Mode (Vendor specific): only to be used by the DRAM manufacturer. No functional operation is specified with test mode enabled.	
Command Address Parity (CAPAR)	OP6	0 – Disabled (Default) 1 – Enabled	1
Write Parity (WPAR)	OP5	0 – Disabled 1 – Enabled	2
Read Parity (RPAR)	OP4	0 – Disabled 1 – Enabled	2
RFU	OP3	0	
Temperature Compensated Self Refresh (TCSR)	OP2	0 – Disabled 1 – Enabled (Default)	
Write DBI (WDBI)	OP1	0 – Disabled 1 – Enabled	3
Read DBI (RDBI)	OP0	0 – Disabled 1 – Enabled	3
NOTE 1 Refer to the Command/Address Parity clause for details regarding CA Parity. NOTE 2 Refer to the Data Parity clause for details regarding Write Parity and Read Parity. NOTE 3 Refer to the Data Bus Inversion (DBIac) clause for details regarding WDBI and RDBI.			

Table 12 — Mode Register 1 (MR1)

Field	Bits	Description	Notes
Parity Latency (PL)	OP[7:5]	000 – 0 nCK 001 – 1 nCK 010 – 2 nCK 011 – 3 nCK 100 – 4 nCK All others – Reserved	1, 2
Write Latency (WL)	OP[4:0]	00100 – 4 nCK 00101 – 5 nCK 00110 – 6 nCK ... 01111 – 15 nCK 10000 – 16 nCK All Others - Reserved	1, 3
NOTE 1 All PL and WL values are optional, however the supported min-to-max ranges must be contiguous. NOTE 2 Refer to the Data Parity clause for details regarding Parity Latency (PL) definition and use with write and read operations. NOTE 3 Refer to the WRITE command clause for details regarding the Write Latency (WL) definitions and use.			

5 Mode Registers (cont'd)

Table 13 — Mode Register 2 (MR2)

Field	Bits	Description	Notes
Read Latency (RL)	OP[7:0]	00000100 – 4 nCK 00000101 – 5 nCK 00000110 – 6 nCK ... 00111110 – 62 nCK 00111111 – 63 nCK All others – Reserved	1, 2
NOTE 1 All RL values are optional, however the supported min-to-max ranges must be contiguous. NOTE 2 Refer to the READ command clause for details regarding the Read Latency (RL) definitions and use.			

Table 14 — Mode Register 3 (MR3)

Field	Bits	Description	Notes
Write Recovery to Auto Precharge (WR)	OP[7:0]	00000100 – 4 nCK 00000101 – 5 nCK 00000110 – 6 nCK ... 00111110 – 62 nCK 00111111 – 63 nCK All others – Reserved	1, 2
NOTE 1 All WR values are optional, however the supported min-to-max range must be contiguous. NOTE 2 WR must be programmed with a value greater than or equal to $RU\{t_{WR}/t_{CK}\}$, where RU stands for round up, t_{WR} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time. If an HBM3 DRAM does not support the mode register definition of t_{WR} in clock cycles, the WR mode register settings will be ignored.			

Table 15 — Mode Register 4 (MR4)

Field	Bits	Description	Notes
Activate to Precharge (RAS)	OP[7:0]	00000100 – 4 nCK 00000101 – 5 nCK 00000110 – 6 nCK ... 00111110 – 62 nCK 00111111 – 63 nCK All others – Reserved	1, 2
NOTE 1 All RAS values are optional, however the supported min-to-max range must be contiguous. NOTE 2 RAS must be programmed with a value greater than or equal to $RU\{t_{RAS}/t_{CK}\}$, where RU stands for round up, t_{RAS} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time. If an HBM3 DRAM does not support the mode register definition of t_{RAS} in clock cycles, the RAS mode register settings will be ignored.			

5 Mode Registers (cont'd)

Table 16 — Mode Register 5 (MR5)

Field	Bits	Description	Notes
RFU	OP[7:4]	0000	
Read to Auto Pre-charge (RTP)	OP[3:0]	0010 – 2 nCK 0011 – 3 nCK 0100 – 4 nCK ... 1110 – 14 nCK 1111 – 15 nCK All others – Reserved	1, 2
NOTE 1 All RTP values are optional, however the supported min-to-max range must be contiguous. NOTE 2 RTP must be programmed with a value greater than or equal to $RU\{t_{RTP}/t_{CK}\}$, where RU stands for round up, t_{RTP} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time. If an HBM3 DRAM does not support the mode register definition of t_{RTP} in clock cycles, the RTP mode register settings will be ignored.			

Table 17 — Mode Register 6 (MR6)

Field	Bits	Description	Notes
RFU	OP[7:6]	00	
Pullup Driver Strength	OP[5:3]	000 – 8 mA 001 – 10 mA 010 – 12 mA (Default) 011 – 14 mA All others – Reserved	1
Pulldown Driver Strength	OP[2:0]	000 – 8 mA 001 – 10 mA 010 – 12 mA (Default) 011 – 14 mA All others – Reserved	1
NOTE 1 Refer to the Transmit Driver Current table for the details.			

5 Mode Registers (cont'd)

Table 18 — Mode Register 7 (MR7)

Field	Bits	Description	Notes
CATTRIP	OP7	0 – CATTRIP pin drives a LOW or HIGH depending on CATTRIP sensor output (Default) 1 – CATTRIP pin drives a static HIGH	1
RFU	OP6	0	
DWORD MISR Control	OP[5:3]	The bits are only evaluated if DWORD Loop-back is enabled in OP0 000 – Preset: the DWORD MISR is preset as described in the HBM3 Loopback Test Modes clause, and all DWORD LFSR_COMPARE_STICKY bits are reset to 0. 001 – LFSR mode (READ direction) 010 – Register mode (WRITE and READ directions): DWORD writes are captured directly into the MISR without compression. The MISR will contain the most recent write data. 011 – MISR mode (WRITE direction) 100 – LFSR Compare mode (WRITE direction) All others - Reserved	2, 3
RFU	OP2	0	
DWORD Read Mux Control	OP1	The bit is only evaluated with READ commands and if DWORD Loopback is enabled in OP0 0 – Return data from DWORD MISR (see OP[5:3]) 1 – Return LFSR_COMPARE_STICKY bits (OP[5:3] is ignored)	2, 3
DWORD Loopback	OP0	0 – Disabled (Default) 1 – Enabled: all Writes and Reads will be to/from the MISR. Notes: a) does not require any row activation b) column addresses associated with WRITE and READ commands are ignored	2
NOTE 1 The CATTRIP pin can be asserted to “HIGH” from any of the channels [a:p] MR7 OP7 bit (logic OR). NOTE 2 See HBM3 Loopback Test Modes for DWORD MISR mode features and use. NOTE 3 Refer to Table 19 for details on DWORD MISR operation with WRITE and READ commands.			

5 Mode Registers (cont'd)

Table 19 — DWORD MISR Read and Write Operations in Loopback Test Mode (MR7 OP0=1)

MR7 OP1	MR7 OP[5:3]	DWORD MISR Operation ¹		Comments
		WRITE	READ	
0	000 (Preset)	Write data are ignored	Read the Preset value (clock-like pattern)	Neither Writes nor Reads alter the MISR content
	001 (LFSR)	Write data are ignored	Generate read data from LFSR	Writes do not alter the MISR content
	010 (Register)	MISR stores the second half (UI 4 to 7) or all data (UI 0 to 7) of the most recent Write from register mode, with only (UI 4 to 7) readable via WDR (see note 2)	Read the MISR content (UI 0 to 3 and repeated for UI 4 to 7, or all data (UI 0 to 7) of the most recent Write (see note 2))	Reads do not alter the MISR content
	011 (MISR)	Write data are accumulated in the MISR		
	100 (LFSR Compare)	Write data are compared against data generated by the LFSR		
1	XXX	Write data are ignored	Read sticky error bits	Neither Writes nor Reads alter the MISR content
NOTE 1 See Loopback Test Modes for DWORD MISR and LFSR features and use. NOTE 2 Depending on implementation, the MISR either stores the second half (UI 4 to 7) or all data (UI 0 to 7) to the most recent Write, and subsequent Reads return either the second half (UI 4 to 7) or all data (UI 0 to 7) to that most recent Write. If a Read shall send identical data regardless of the actual implementation, users should send the same write data on UI 0 to 3 and UI 4 to 7 of the most recent write.				

Table 20 — Mode Register 8 (MR8)

Field	Bits	Description	Notes
RFU	OP[7:6]	00	
RFM Levels (RFML)	OP[5:4]	00 – Default Level (RFM may be required or not) 01 – Level A (RFM is required) 10 – Level B (RFM is required) 11 – Level C (RFM is required)	1
WDQS-to-CK Training (WDQS2CK)	OP3	0 – Disabled (Default) 1 – Enabled	2
ECS error log auto reset (ECSLOG)	OP2	0 – Disabled (Default) 1 – Enabled	
Duty Cycle Monitor (DCM)	OP1	0 – Disabled (Default) 1 – Enabled	
DA Port Lockout	OP0	0 – Access to DA port is enabled (Default) 1 – Access to DA port is locked	3
NOTE 1 The support of Adaptive Refresh Management (ARFM) is optional for the DRAM vendor. HBM3 DRAMs not supporting (ARFM) will define these bits as RFU. RAAIMT, RAAMMT and RAADEC values for default RFM level and RFM levels A to C are set by DRAM vendor and can be read via the IEEE1500 DEVICE_ID WDR. NOTE 2 Refer to the WDQS-to-CK Alignment Training clause for details. NOTE 3 DA Port Lockout bit is defined for channels a and e only. The bit is RFU for all other channels. Once enabled, the bit can only be cleared by powering off the device. The IEEE1500 MODE_REGISTER_DUMP_SET instruction cannot be used to set or clear the bit, but allows reading the bit.			

5 Mode Registers (cont'd)

Table 21 — Mode Register 9 (MR9)

Field	Bits	Description	Notes
ECS Error Type and Address Reset (ECSRES)	OP7	0 – Maintain the ECS error type and address log (Default) 1 – Reset the ECS error type and address log (self-clearing)	1
ECS multi-bit error correction (ECSCEM)	OP6	0 – Correction of multi-bit errors during ECS cycles is disabled 1 – Correction of multi-bit errors during ECS cycles is enabled	
Auto ECS during Self Refresh (ECSSRF)	OP5	0 – Auto ECS during self refresh mode is disabled (Default) 1 – Auto ECS during self refresh mode is Enabled	2
Auto ECS via REFab (ECSREF)	OP4	0 – Auto ECS via REFab command is disabled (Default) 1 – Auto ECS via REFab command is enabled	2, 3
Error Vector Pattern (ECCVEC)	OP3	The bit is only evaluated when ECC Vector Input Mode is enabled in OP2 0 – Codeword 0 (CW0): Data '1' means error bit and data '0' means non-error bit 1 – Codeword 1 (CW1): Data '0' means error bit and data '1' means non-error bit	
Error Vector Input Mode (ECCTM)	OP2	0 – ECC Engine Test Mode is disabled (default) 1 – ECC Engine Test Mode is enabled	
Severity Reporting (SEVR)	OP1	0 – Error severity reporting is disabled and the SEV signals are High-Z 1 – Error severity reporting is enabled. The SEV signals drive error severity information during Reads and otherwise are High-Z.	4
Meta Data (MD)	OP0	0 – ECC signals are disabled. Read and write operations do not include meta data 1 – ECC signals are enabled. Read and write operations include meta data transmitted via ECC pins	
NOTE 1 The bit is self-clearing meaning that it automatically returns back to 0 after the reset function has been issued. NOTE 2 For ECS operation either ECSSRF or ECSREF (or both) must be enabled. NOTE 3 When ECS during REFab is enabled, the host must issue REFab commands at an average rate of t_{ECSint} . NOTE 4 Input data on SEV signals during write operations will be ignored regardless of the SEVR setting.			

Table 22 — Mode Register 10 (MR10)

Field	Bits	Description	Notes
Vendor Specific	OP[7:0]	Vendor Specific	1
NOTE 1 MR10 is reserved for vendor specific features. Refer to the vendor's datasheet for details.			

5 Mode Registers (cont'd)

Table 23 — Mode Register 11 (MR11)

Field	Bits	Description	Notes
DCA code for WDQS1 (PC1)	OP[7:4]	0000 – 0 steps (Default; no correction) 0001 – -1 step 0010 – -2 steps ... 0110 – -6 steps 0111 – -7 steps 1000 – Reserved 1001 – +1 step 1010 – +2 steps ... 1110 – +6 steps 1111 – +7 steps	1, 2
DCA code for WDQS0 (PC0)	OP[3:0]	0000 – 0 steps (Default; no correction) 0001 – -1 step 0010 – -2 steps ... 0110 – -6 steps 0111 – -7 steps 1000 – Reserved 1001 – +1 step 1010 – +2 steps ... 1110 – +6 steps 1111 – +7 steps	1, 2
NOTE 1 Values of 0001 to 0111 decrease the internal WDQS duty cycle, and values of 1001 to 1111 increase the internal WDQS duty cycle.			
NOTE 2 The step size (in ps) is vendor specific and may be non-linear.			

Table 24 — Mode Register 12 (MR12)

Field	Bits	Description	Notes
Reserved for Vendor Specific Features	OP[7:0]	00000000	1
NOTE 1 MR12 is reserved for vendor specific features. Refer to the vendor's datasheet for details.			

Table 25 — Mode Register 13 (MR13)

Field	Bits	Description	Notes
RFU	OP[7:0]	00000000	

5 Mode Registers (cont'd)

Table 26 — Mode Register 14 (MR14)

Field	Bits	Description	Notes
RFU	OP7	0	
Reference voltage for AWORD inputs (VREFCA)	OP[6:1]	000000 – $0.18 \times V_{DDQL}$ 000001 – $0.19 \times V_{DDQL}$... 011111 – $0.49 \times V_{DDQL}$ 100000 – $0.50 \times V_{DDQL}$ (Default) 100001 – $0.51 \times V_{DDQL}$... 111110 – $0.80 \times V_{DDQL}$ 111111 – $0.81 \times V_{DDQL}$	
RFU	OP0	0	
NOTE 1 Refer to the DC and AC Operating Conditions clause for the AWORD input receiver voltage level specification.			

Table 27 — Mode Register 15 (MR15)

Field	Bits	Description	Notes
RFU	OP7	0	
Reference voltage for DWORD inputs (VREFD)	OP[6:1]	000000 – $0.18 \times V_{DDQL}$ 000001 – $0.19 \times V_{DDQL}$... 011111 – $0.49 \times V_{DDQL}$ 100000 – $0.50 \times V_{DDQL}$ (Default) 100001 – $0.51 \times V_{DDQL}$... 111110 – $0.80 \times V_{DDQL}$ 111111 – $0.81 \times V_{DDQL}$	
RFU	OP0	0	
NOTE 1 Refer to the DC and AC Operating Conditions clause for the DWORD input receiver voltage level specification.			

6 Operation

6.1 HBM3 Clocking Overview

The HBM device captures commands and addresses on the row and column buses using a differential clock CK_t/CK_c. Both buses operate at double data rate (DDR).

The HBM device has uni-directional differential Write strobes (WDQS_t/WDQS_c) and Read strobes (RDQS_t/RDQS_c) per 32DQ(DWORD). The data bus operates at double data rate (DDR).

HBM3 utilizes two types of clock with different frequencies. The strobe frequency is twice the frequency of the command clock, requiring an HBM3 to have reset-type clock-divider in the WDQS clock tree (Figure 10). By dividing the WDQS, the operation speed of DRAM internal circuits in WDQS domain is reduced to half. The direction of the internal WDQS/2 transition may vary depending on vendor's choice. Command clock and WDQS are generated from the same PLL and RDQS clock is generated from WDQS. WDQS internal divider is initialized to be a pre-defined internal divider state after Self Refresh exit or Power-up or Power down exit sequence. The sum of preamble and postamble for both READ and WRITE operation is required to be an even number so that the internal divider's state, phase of internal WDQS/2, is maintained. Therefore, HBM3 WDQS does not require a specific sync operation before READ and WRITE operations. WDQS starts toggling before starting WRITE or READ operations for reducing ISI. During inactivity, WDQS/ RDQS are required to be static (WDQS/RDQS_t is Low, WDQS/RDQS_c is High). When WRITE training for unmatched DQ/DQS path, DQ should be shifted to align phase to the point where CK and WDQS are in sync.

The following nomenclature is being used throughout this standard:

- a rising CK (or WDQS, RDQS) edge is defined as the crossing of the positive edge of CK_t (or WDQS_t, RDQS_t) and the negative edge of CK_c (or WDQS_c, RDQS_c);
- a falling CK (or WDQS, RDQS) edge is defined as the crossing of the negative edge of CK_t (or WDQS_t, RDQS_t) and the positive edge of CK_c (or WDQS_c, RDQS_c).

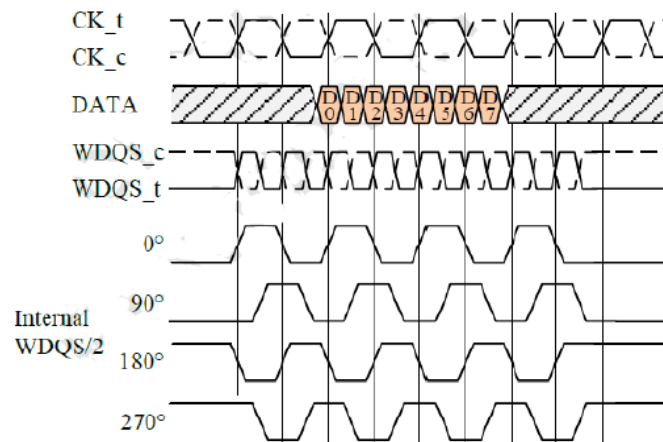
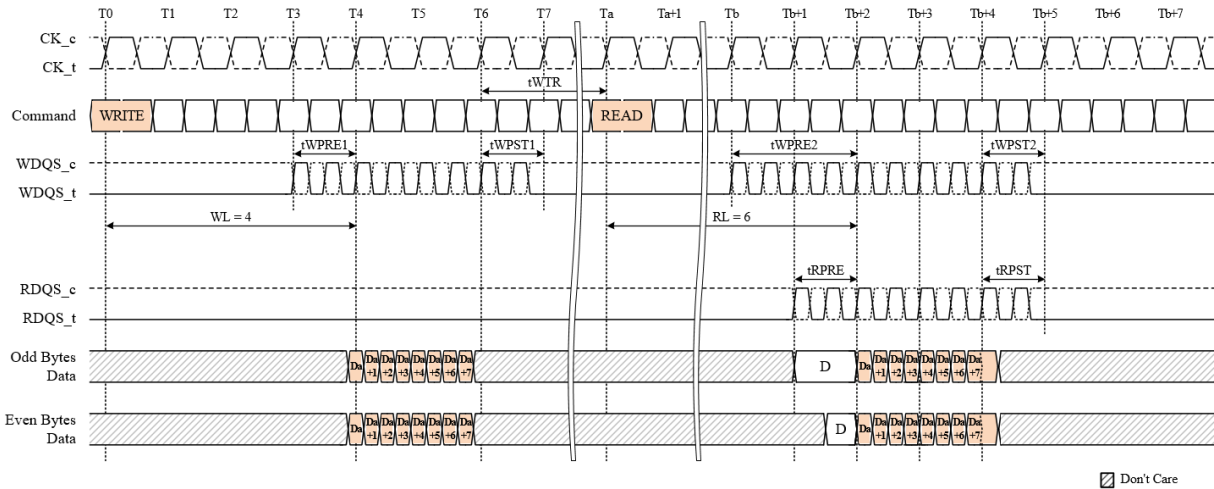


Figure 8 — Aligned WDQS Internal Divider Example

6.1 HBM3 Clocking Overview (cont'd)



NOTE 1 tWPST1 : Write preamble of WDQS, tWPST1 : Write postamble of WDQS

NOTE 2 tWPST2 : Read preamble of WDQS, tWPST2 : Read postamble of WDQS

NOTE 3 tRPST : Read preamble of RDQS, tRPST : Read postamble of RDQS

Figure 9 — Clocking and Interface Relationship Write to Read Timing

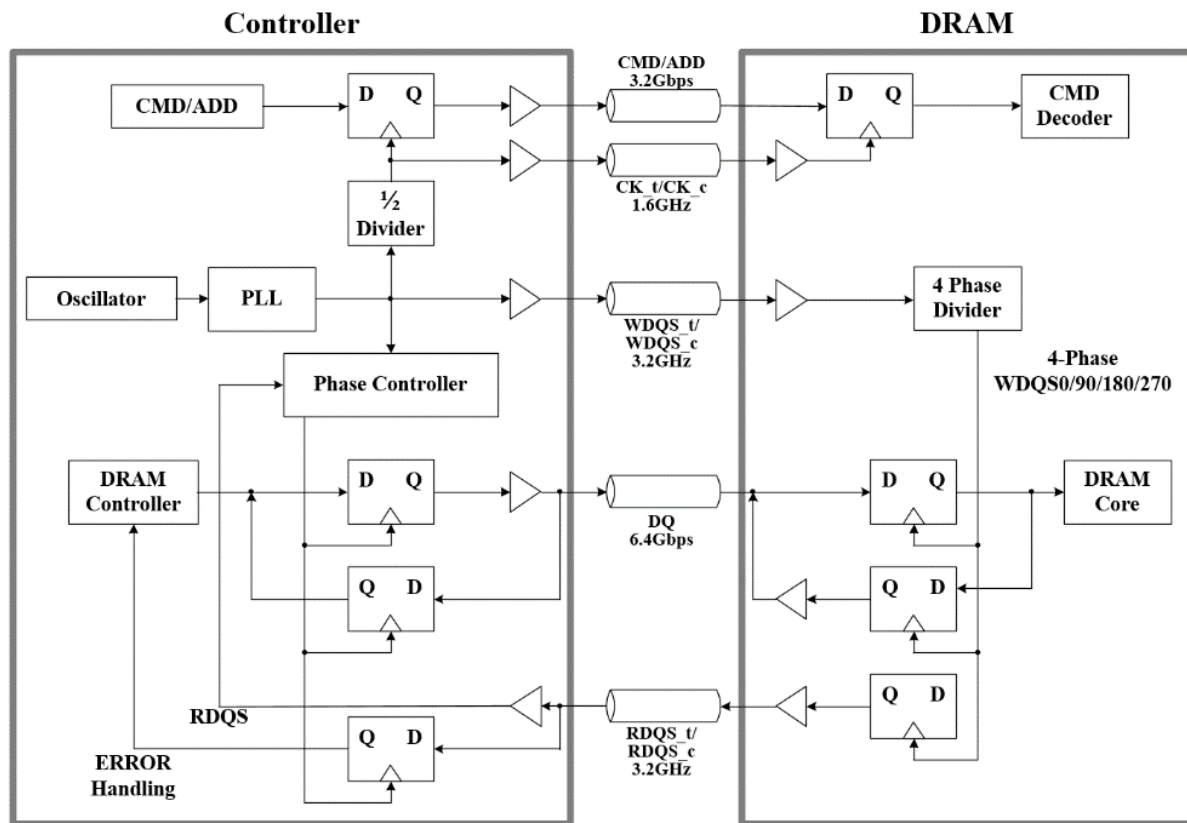


Figure 10 — High Level Block Diagram Example of Clocking Scheme

6.1.1 WDQS-to-CK Alignment Training

WDQS-to-CK alignment training allows the host to observe the phase offset between the WDQS strobes in both PCs and the CK clock to aid in keeping the phase relationship within the limits given by the t_{DQSS} specification. The WDQS2CK bit in MR8 OP3 is associated with this training mode.

WDQS-to-CK alignment training is required to be performed at least once after device initialization if adherence to the t_{DQSS} timing cannot be guaranteed without performing this alignment training. WDQS-to-CK alignment training is not required if the t_{DQSS} timing is met. An effort to further narrow the WDQS-to-CK phase offset by using this training mode will not improve the stable device operation.

Steps 1 through 7 are required for WDQS-to-CK alignment training:

1. Enter WDQS-to-CK alignment training mode by setting the WDQS2CK bit to 1 and wait t_{MOD} . Commands allowed while in this mode are REFab, REFpb, RFMab, RFMpb, RNOP, CNOP and MRS to exit WDQS-to-CK alignment training. Internal current spikes generated by the use of REFab, REFpb, RFMab and RFMpb commands in this mode may negatively impact the training result. Controllers that cannot account for this impact should avoid use of REFab, REFpb, RFMab and RFMpb commands in this mode.
2. Enable both WDQS0 and WDQS1 strobes; keep both strobes constantly running in order to generate a valid read-out at both phase detectors with each CK clock cycle;
3. Slowly sweep the WDQS0 and WDQS1 phases with respect to the CK clock, and monitor both DERR0 and DERR1 signals for the phase detector's result as shown in Table 28 and Figure 11; each phase detector latches the 0° phase of the internally divided WDQS strobe (0° phase) with each rising CK clock edge and provides the result on the DERR0 signal for WDQS0 and the DERR1 signal for WDQS1 after $t_{WDQS2PD}$;
4. After a minimum of 8 WDQS pulses have been received, the strobes may be halted at any time while WDQS-to-CK alignment training mode is enabled; the phase detector does not provide a valid read-out in this case and it's result on the DERR signals should be ignored;
5. The ideal alignment is indicated by the phase detector output transitioning from "early" to "late" when the delay of the WDQS phase is continuously increased;
6. When the phase relationship between WDQS and CK meets the t_{DQSS} specification, stop both WDQS strobes; ensure that the number of WDQS pulses issued while in this training mode is an even number such that the internal WDQS state is back at its reset state once the training has finished. With that, no specific synchronization between CK and WDQS is required for correct write and read operation;
7. Exit WDQS-to-CK alignment training mode by setting the WDQS2CK bit to 0 and wait t_{MOD} .

Table 28 — Phase Detector and DERR Signal Behavior

Internal WDQS/2 (0° Phase) Sampled By CK	WDQS Phase	DERR0 DERR1	Recommended Action
HIGH	Early	HIGH	Increase delay on WDQS
LOW	Late	LOW	Decrease delay on WDQS

6.1.1 WDQS-to-CK Alignment Training (cont'd)

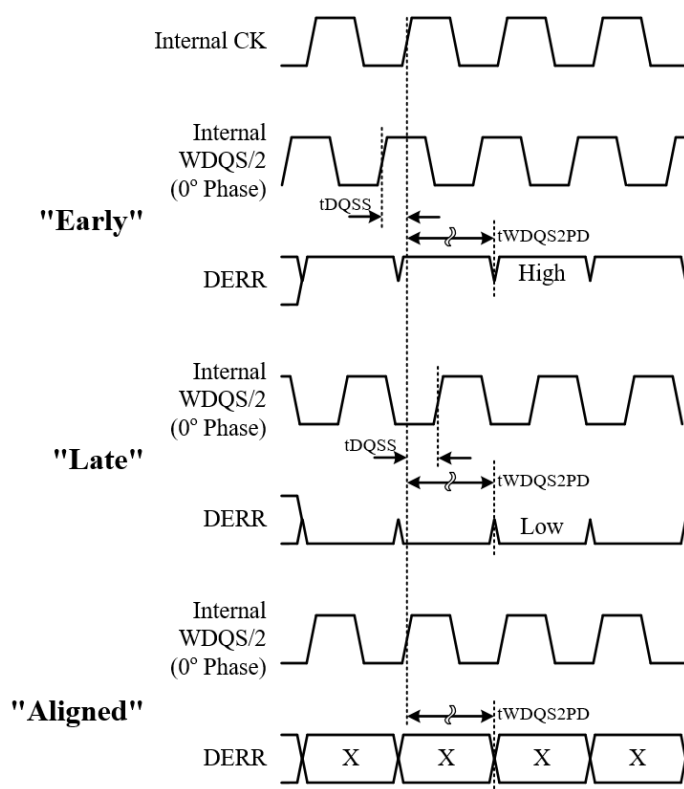


Figure 11 — DERR Signal Behavior in WDQS-to-CK Alignment Training

6.2 HBM3 Data Bus Inversion (DBIac)

6.2.1 Data Bus Inversion (DBIac)

HBM3 DRAMs supports a byte granular Data Bus Inversion (DBIac). The corresponding DBI signal is a DDR I/O and driven or sampled along with the DQs for read and write operations.

The word DBI refers to the internal state of the device unless explicitly noted as DBI signal. The DBIac function can be enabled or disabled independently for writes per MR0 OP1 (WDBI) and for reads per MR0 OP0 (RDBI).

The DBI input is a Don't care and the DBI input receivers are disabled when WDBI is disabled. The DBI output buffers are turned off when RDBI is disabled.

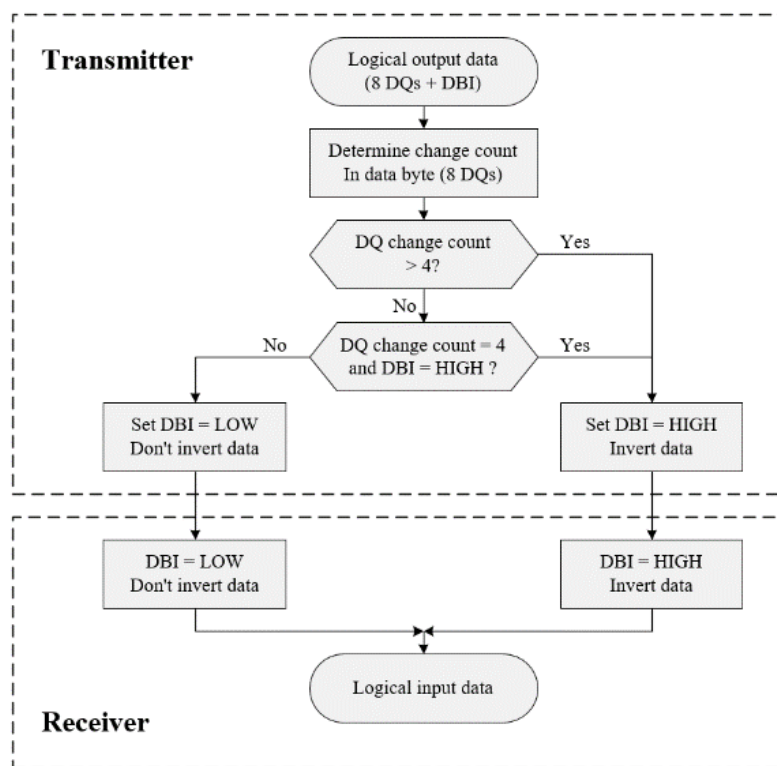


Figure 12 — DBIac Algorithm

Write operation: the HBM3 DRAM inverts write data received on the DQ inputs in case DBI is sampled HIGH, or leaves the write data non-inverted in case DBI is sampled LOW. Note that the ECC inputs are not affected by the DBIac function.

Read operation: the HBM3 DRAM counts the number of DQ signals that are transitioning from the previous state. Note that the ECC and SEV outputs are not affected by DBIac. See Internal DBIac States with Read for bus pre-conditioning. The HBM3 DRAM inverts read data and sets DBI HIGH when the number of transitioning data bits within a byte is greater than 4, or when the number of transitioning data bits within a byte equals 4 and DBI was HIGH; otherwise the HBM3 DRAM does not invert the read data and sets DBI LOW.

6.2.1 Data Bus Inversion (DBIac) (cont'd)

Table 29 — DBI(ac) Truth Table

DQ Charge Count	Previous DBI State	New DBI State	New DQ State
0 to 3	X	LOW	Not inverted
4	LOW		
	HIGH	HIGH	Inverted
5 to 8	X		

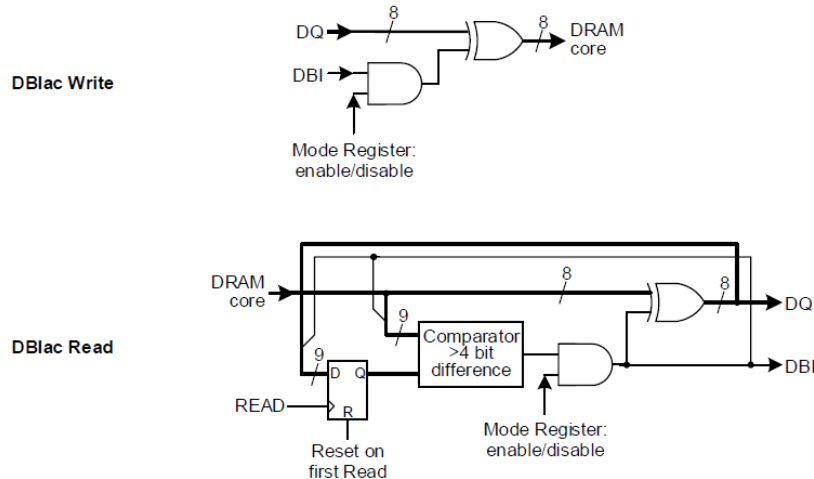


Figure 13 — Example DBIac Logic for Write and Read

6.2.1.1 Internal DBIac State with Read

The HBM3 DRAM resets the internal DBIac state to LOW whenever any of the following events occur:

- RESET_n signal de-assertion;
- a MODE REGISTER SET (MRS) command is received;
- a write-to-read bus turnaround;
- Self Refresh exit

For all other events or commands, the internal DBIac state is not reset to LOW and the HBM3 DRAM will use its previous state for DBIac calculation.

First Read Command:

When a first READ command is registered after a DBI reset, the HBM3 DRAM preconditions the bus to LOW prior to read data regardless whether RDBI is enabled or disabled in the mode register, as shown in Figure 14 in case of a write-to-read bus turnaround. The internal state D7 corresponding to the last UI of the read burst is internally stored as a seed value for a subsequent read burst.

The DPAR signal is not included in the DBI calculation and not preconditioned to LOW; its initial state is undefined (LOW or HIGH).

6.2.1.1 Internal DBIac State with Read (cont'd)

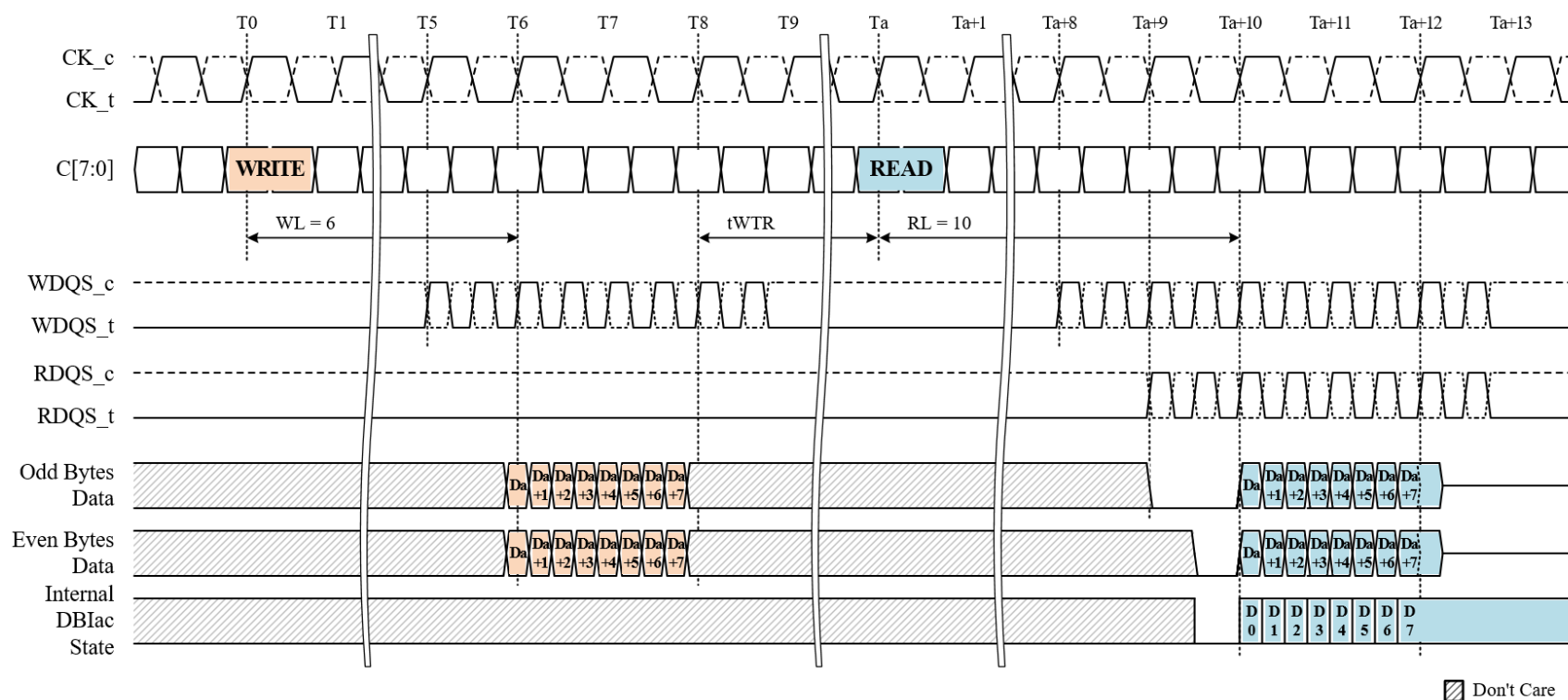


Figure 14 — Internal DBIac State Reset for Write to Read

6.2.1.2 Internal DBIac State with Consecutive Read Commands (Seamless and non-seamless)

Once the Read burst is complete, the HBM3 DRAM tri-states all DQ, DBI and ECC output drivers. However, the HBM3 DRAM internally stores the last data-out of the DQ, DBI, ECC and SEV outputs to pre-condition the bus prior to a subsequent read; it also uses the last data-out of the DQ and DBI outputs for DBIac calculation for any subsequent read operation barring a condition to DBI reset. For non-gapless read operations, the HBM3 DRAM pre-conditions all data outputs to the last data-out of the previous burst nominally two WDQS cycles (odd bytes) and one WDQS cycle (even bytes) prior to the first valid data bit as shown in Figure 15.

6.2.1.2 Internal DBIac State with Consecutive Read Commands (Seamless and non-seamless) (cont'd)

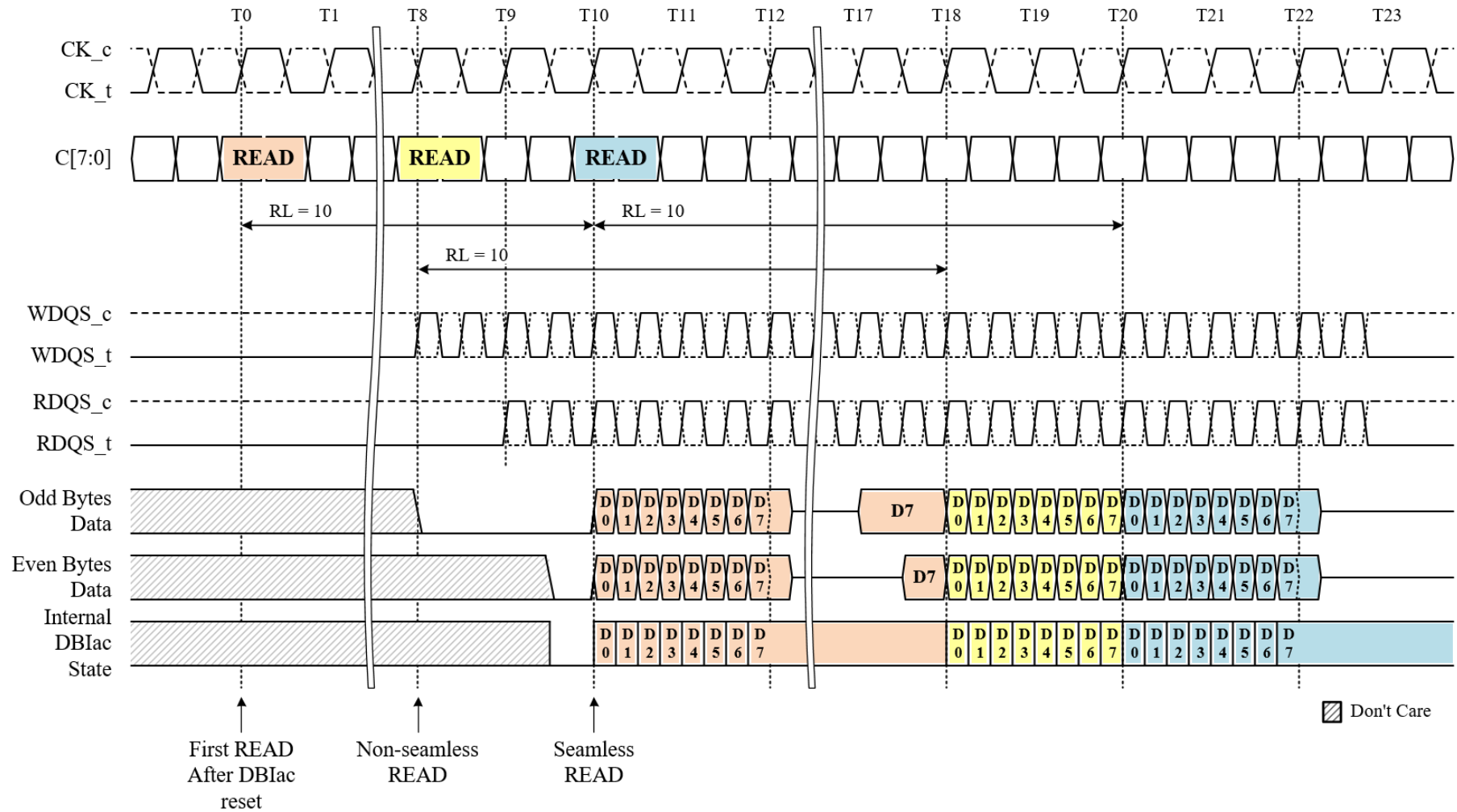


Figure 15 — Bus Preconditioning and DBI States for Read

6.3 Commands

The HBM3 DRAM features DDR commands entered on both rising and falling CK clock edges. Row Activate commands require one-and-a-half-cycle and other row commands require only a half-cycle except for PDE and SRE with one cycle. Column commands require only one cycle.

The command interface includes a reserved DDR input signal ARFU which is omitted from subsequent truth tables but required to be driven to a valid signal level along with the other AWORD inputs.

6.3.1 Command Truth Tables

Table 30 — Row Commands Truth Table

Command ⁴	Symbol	Clock Cycle	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	Notes
Row No Operation	RNOP	R or F	H	H	H	H	V	V	V	V	V	V	1, 2, 3
Activate	ACT	R	L	H	H	PC	SID0 / V	SID1 / V	BA0	BA1	BA2	BA3	1, 2, 3, 5, 6
		F	H	H	RA8	RA9	RA10	RA11	RA12	RA13 / V	RA14 / V	V	
		R	H	H	RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	
Precharge	PREpb	R or F	H	L	L	PC	SID0 / V	SID1 / V	BA0	BA1	BA2	BA3	1, 2, 3, 5, 6
Precharge All	PREab	R or F	H	L	H	PC	V	V	V	V	V	V	1, 2, 3, 5
Per-Bank Refresh	REFpb	R	L	L	L	PC	SID0 / V	SID1 / V	BA0	BA1	BA2	BA3	1, 2, 3, 5, 6
All-Bank Refresh	REFab	R	H	H	L	PC	V	V	V	V	L	V	1, 2, 3, 5
Per-Bank Refresh Management	RFMpb	R	L	L	H	PC	SID0 / V	SID1 / V	BA0	BA1	BA2	BA3	1, 2, 3, 5, 6, 7
All-Bank Refresh Management	RFMab	R	H	H	L	PC	V	V	V	V	H	V	1, 2, 3, 5, 7
Power-Down Entry	PDE	R	L	H	L	H	V	V	V	V	V	V	1, 2, 3
		F	L	H	L	H	V	V	V	V	V	V	
Self Refresh Entry	SRE	R	L	H	L	L	V	V	V	V	V	V	1, 2, 3
		F	L	H	L	L	V	V	V	V	V	V	
Power-Down and Self Refresh Exit	PDX/ SRX	R	H	H	H	H	V	V	V	V	V	V	1, 2, 8

NOTE 1 BA = Bank Address; RA = Row Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; V = Valid Signal (either H or L, but not floating);

NOTE 2 R[9:0] must be driven to a valid signal level even if a stack ID address (SID) or row address (RA) is not defined for a specific density. APAR must be driven to a valid signal level even if CA parity is disabled in MR0 OP6.

NOTE 3 Parity is evaluated on all pins if CA parity is enabled in MR0 OP6.

NOTE 4 All other command encodings not shown in the table are reserved for future use.

NOTE 5 PC = 0 selects pseudo channel 0 (PC0), and PC = 1 selects pseudo channel 1 (PC1). The pseudo channel not selected by PC performs a RNOP.

NOTE 6 The SID bits act as bank address bits in conjunction with ACT, PREpb, REFpb and RFMpb commands, and related timing diagrams shall be interpreted accordingly. All other row commands do not use SID. Refer to the channel addressing table for HBM3 configurations using SID.

NOTE 7 An HBM3 DRAM not requiring refresh management (RFM) will execute an RNOP command instead of RFMab or RFMpb.

NOTE 8 No Parity checking at Power-Down Exit or Self Refresh Exit command. The HBM3 device requires RNOP and CNOP commands on Row and Column bus respectively with valid parity if CA parity is enabled during the power-down exit period (t_{XP}) and self refresh exit period (t_{XS}).

NOTE 9 ACT is a 1.5 cycle command and another command is not allowed during ACT command.

6.3.1 Command Truth Tables (cont'd)

Table 31 — Column Commands Truth Table

Command ⁴	Symbol	Clock Cycle	C0	C1	C2	C3	C4	C5	C6	C7	Notes
Column No Operation	CNOP	R	H	H	H	V	V	V	V	V	1, 2, 3
		F	V	V	V	V	V	V	V	V	
Read	RD	R	H	L	H	L	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6, 7
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Read w/ AP	RDA	R	H	L	H	H	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6, 7
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Write	WR	R	H	L	L	L	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Write w/ AP	WRA	R	H	L	L	H	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Mode Register Set	MRS	R	L	L	L	MA4	OP5	OP6	OP7	MA0	1, 3, 8, 9
		F	MA1	MA2	MA3	OP0	OP1	OP2	OP3	OP4	

NOTE 1 BA = Bank Address; CA = Column Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; MA = Mode Register Address; V = Valid Signal (either H or L, but not floating).

NOTE 2 C[7:0] must be driven to a valid signal level even if a stack ID address (SID) is not defined for a specific density, or if parity is disabled in the mode register. APAR must be driven to a valid signal level even if CA parity is disabled in MR0 OP6. C[7:0] are Don't Care when the device is in power-down or self refresh.

NOTE 3 Parity is evaluated on all pins if CA parity is enabled in MR0 OP6.

NOTE 4 All other command encodings not shown in the table are reserved for future use.

NOTE 5 PC = 0 selects pseudo channel 0 (PC0), and PC = 1 selects pseudo channel 1 (PC1). The pseudo channel not selected by PC performs a CNOP.

NOTE 6 The SID bits act as bank address bits in conjunction with READ and WRITE commands, and related timing diagrams shall be interpreted accordingly. All other column commands do not use SID. Refer to the channel addressing table for HBM3 configurations using SID.

NOTE 7 HBM3 configurations using the SID specify a timing parameter t_{CCDR} for consecutive READs to different SID. Vendor datasheets should be consulted for details.

NOTE 8 All mode registers are write-only by default using the MRS command.

NOTE 9 Refer to the HBM3 Mode Register Overview table for MA4 of MRS.