

JEDEC STANDARD

Procedure for Wafer-Level DC Characterization of Bias Temperature Instabilities

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PROCEDURE FOR WAFER-LEVEL DC CHARACTERIZATION OF BIAS TEMPERATURE INSTABILITIES

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Foreword

This test procedure was drafted and approved by JEDEC JC-14.2 Wafer-Level Reliability Committee consisting of recognized bias-temperature instability industry experts from foundries and fabless member companies.

The objective of this Bias Temperature Instability (BTI) stress/test procedure is to provide a minimum recommendation for a simple and consistent comparison of End of Life (EOL) mean threshold voltage (V_T) shift due to BTI aging at agreed worst dc use conditions. Both PTBI and NBTI are addressed in this characterization procedure and can be easily implemented to allow comparison of BTI on different mature CMOS processes. Bias-temperature instabilities are investigated in a capacitor-like configuration with the MOSFET gate biased ($|V_{GS}| > 0$) at high temperature while other contacts are grounded (no channel conduction) ($V_{DS} = 0$). Typically physical BTI damage results in the degradation of the voltage threshold (V_T), as well as changes in the channel mobility and transconductance. As a consequence of the degradation of device parameters the circuit may fail to fully meet functional requirements.

The procedure enables only:

- Comparison of stable and manufacturable CMOS processes and technologies in which the process variation is low and the yield is mature.
- Estimate BTI aging of large area MOSFET transistor with a channel width, W_{des} ($W_{des} \geq W_{min}$ – see Annex B) and length L_{des} .
- Estimate of linear mean V_T shift as a measure of device flatband shift dependence on BTI aging. Annex A. provides recommendations to estimate other device parameters associated to BTI induced mobility and transconductance degradation.

BTI qualification and accept-reject criteria are not given in this document. Historical discrepancies resulting from inconsistent observation, metrology capabilities and quantification of BTI damage on the same CMOS process and technology are addressed by using this procedure as benchmark for BTI comparison.

The stress/test BTI dc characterization methodology can be used within the limits of this procedure as a benchmark to monitor BTI damage as related to flatband V_T shift. Future revisions this proposed methodology will be introduced as more experimental findings become available.

PROCEDURE FOR WAFER-LEVEL DC CHARACTERIZATION OF BIAS TEMPERATURE INSTABILITIES

(From JEDEC Board Ballot JCB-15-22, formulated under the cognizance of the JC-14.2 Subcommittee on Wafer-Level Reliability.)

1 Scope

The scope of this document is to provide a minimum common protocol for foundries and fabless customers to compare the dc BTI induced mean V_T shift at an agreed End of Life (EOL) of a MOSFET transistor with a channel width, W_{des} ($W_{\text{des}} \geq W_{\text{min}}$ – See Annex B) and length L_{des} of a manufacturable CMOS process and technology. The BTI comparison is proposed at an assumed worst dc use conditions (V_{DDmax} , T_{Jmax}). The procedure applies to both Negative ($V_{\text{GS}} < 0$) (NBTI) and Positive ($V_{\text{GS}} > 0$) (PBTI) BTI conditions for both pMOSFET and nMOSFET transistors.

The proposed procedure consists of two parts:

1) BTI stress/test characterization methodology

A two-step stress/test waveform with V_{GS} and V_{DS} switching between a capacitor-like BTI stress with no channel conduction ($V_{\text{GS}} = V_{\text{GSstr}}$, $V_{\text{DS}} = V_{\text{DSstr}} = 0$) and a single drain current, I_{D} , measurement in linear mode ($V_{\text{GS}} = V_{\text{GSst}}$, $V_{\text{DS}} = V_{\text{DSst}} < V_{\text{DSat}}$). The V_{GSst} is chosen to estimate the constant current V_T ($V_{\text{T(ci)}}$) in the linear region of the weakly inverted region of the device I/V characteristics to mainly monitor the associated flatband voltage shift (charge accumulation in the gate dielectric stack). Measurement is accomplished with a selected measuring delay ($1 \mu\text{s} \leq \Delta \leq 2 \text{ ms}$) from stress to test bias conditions. The procedure to determine Δ is given in paragraph 6. As a reference, a procedure to determine I_{D} shifts in linear or saturation mode and $V_{\text{T(ci)}}$ shift in saturation mode during dc BTI stressing is given in Annex A.

2) DC EOL V_T shift estimation at worst V_{DDnom}/T dc use conditions.

Estimation of dc V_T shift at a given EOL is performed once a phenomenological BTI model is derived that is representative of the dc BTI sensitivity of the CMOS processes and/or technologies under evaluation. Section 7, describes this procedure and Annex C suggests a possible $V_{\text{GSstr}}/T_{\text{str}}$ design of experiments to estimate the DC BTI model parameters.

2 Normative references

- ASTM F616-86, *Standard Method for Measuring MOSFET Drain Leakage Current*.
 ASTM F617-86, *Standard Method for Measuring MOSFET Linear Threshold Voltage*.
 ASTM F1096-87, *Standard Method for Measuring MOSFET Saturated Threshold Voltage*.
 JEP001, *Foundry Process Qualification Guidelines (Wafer Fabrication Manufacturing Sites)*.
 JEP122, *Failure Mechanisms and Models for Semiconductor Devices*.
 JESD60, *A Procedure for Measuring P-Channel MOSFET Hot-Carrier Induced Degradation Under DC Stress*.
 JESD77, *Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices*.
 JESD90, *A Procedure for Measuring P-Channel MOSFET Negative Bias Temperature Instabilities*.
 JESD91, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms*.

3 Terms and definitions

For the purposes of this standard, the terms and definitions given apply.

alternating current, ac: The voltage bias applied at alternating current bias conditions.

bias temperature instability, BTI: A temperature-activated intrinsic wear out mechanism in MOSFETs operating with the channel in inversion or accumulation.

NOTE 1 ($|V_{GS}| > 0$) with no channel conduction ($V_{DS} = 0$).

NOTE 2 Wearout results in an increase in the $|V_{TO}|$ with consequential decrease in drain current and possibly transconductance. BTI aging with $V_{GS} < 0$ is called NBTI (Negative BTI), while with $V_{GS} > 0$ it is called PBTI (Positive BTI).

BTI power law time exponent, n: The BTI aging exponent that describes a typical power law dependence on stress time.

channel length, L_{des} : The MOSFET channel length by design.

channel width, W_{des} : The design channel width.

cumulative stress time, t_{str} : The cumulative stress time.

current threshold voltage, constant $V_{T(c)}$: The threshold voltage at a constant current.

direct current, dc: A constant voltage bias condition. (No alternating component.)

drain current, I_D : The direct current into the drain terminal.

drain supply voltage, dc, V_{DD} : The drain supply voltage.

drain-to-source voltage, V_{DSlin} : The drain-to-source voltage in the linear region of the IV curve ($V_{DS} \ll V_{DSat}$).

drain-to-source voltage, V_{DSsat} : Drain-to-source voltage in the saturation region of the IV curve ($V_{DS} \geq V_{DSat}$).

gate current dc, I_G : The direct current into the gate terminal.

gate-source voltage, dc, V_{GS} : The dc voltage between the gate and source terminals.

linear drain current, I_{Dlin} : The linear drain current measured when the transistor is biased in the linear region.

maximum drain supply voltage, V_{DDmax} : The maximum rated supply voltage of the technology.

measurement delay, Δ : The measurement delay determined from the minimum equipment timestamp to reach a stable I_D measurement during testing.

3 Terms and definitions (cont'd)

metal-oxide-semiconductor field-effect transistor, MOSFET: An insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material and the gate is metal or another highly conductive material. (Ref. IEC 747-8.)

NOTE See JESD77 for MOSFET terms.

MOSFET gate oxide thickness, T_{ox} : The oxide thickness parameter used for inline monitoring ($T_{ox,gl}$, T_{inv} etc.).

n-channel field-effect transistor, nFET: A field-effect transistor that has an n-type conduction channel. (Ref. IEC 747-8.)

nominal drain supply voltage, dc, V_{DDnom} : The nominal drain supply voltage, dc.

p-channel field-effect transistor, pFET: A field-effect transistor that has a p-type conduction channel. (Ref. IEC 747-8.)

saturation drain current, I_{Dsat} : The drain current when the transistor is biased in the saturation region.

stress gate-source voltage dc, V_{GSstr} : The V_{GS} at stress conditions.

stress mode: The bias condition at which a MOSFET device is stressed.

stress temperature, T_{str} : The chamber ambient temperature at which the DUT is stressed during BTI stress.

NOTE When only one temperature experiment is run, the stress temperature should be the maximum allowed during circuit operation.

test gate-source voltage dc, V_{GSst} : The V_{GS} at test conditions.

test mode: The bias condition at which a MOSFET device parameter is monitored during test.

test temperature, T_{tst} : The chamber ambient temperature at which the DUT is tested during the test of the device which is typically $T_{tst}=T_{str}$ during the BTI stress.

test time, t_{tst} : The cumulative test time that includes stress delay time ($t_{str} + \Delta$).

NOTE Δ is the stress delay time defined later in the definition list.

threshold voltage, linear, V_{Tlin} : The threshold voltage tested in linear mode.

threshold voltage, linear, V_{Tsat} : The threshold voltage measured in saturation mode.

threshold voltage, V_T : The threshold voltage is the gate voltage at which an inversion layer forms at the interface between the insulating layer (gate dielectric) and the substrate (body) of a MOSFET transistor.

well current dc, I_W : The direct current into the well contact.

NOTE If the well is an n-well then $I_{Wn}=I_W$, if a p-well then $I_{Wp}=I_W$.

well to source voltage, stress, V_{WSstr} : The V_{ws} at stress conditions.

well to source voltage, V_{ws} : The well to-source voltage.

4 Technical requirements

4.1 Constant current threshold Voltage – $V_{T(ci)}$ determination

For a MOSFET at a given V_{DS} and V_{WS} bias condition, the constant current threshold voltage ($V_{T(ci)}$) is defined as the V_{GS} applied to the device to result in a given I_D value (I_{VT}) at test such that $V_{T(ci)} \equiv V_{GS}$ at I_{VT} . A typical selected value for I_{VT} is; $I_{VT} = I_{D0} \times (W_{des}/L_{des})$ with I_{D0} being the drain current per square of channel corresponding to a constant inversion charge density. Typically an I_{D0} of between 50-300 nA is selected corresponding to a V_T measured in the weakly inverted region of the device.

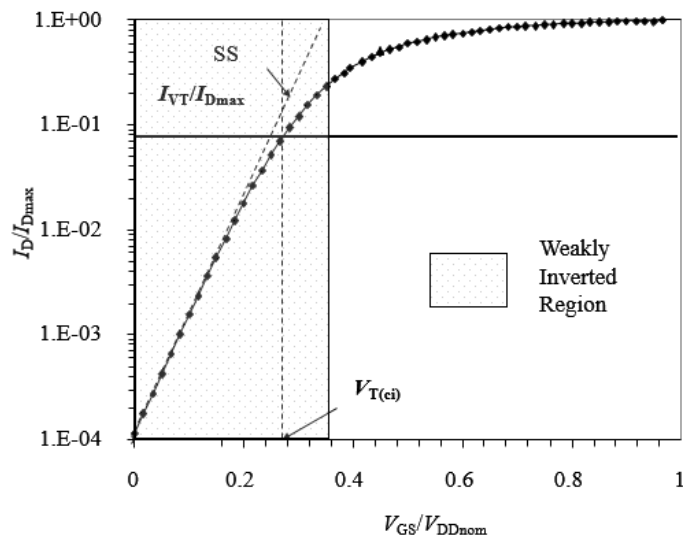


Figure 1 — Normalized I_D/I_{Dmax} (linear-log scale) as function of V_{GS}/V_{DDnom} in the linear region ($V_{DS} < V_{DSsat}$). $I_{VT} = I_{D0} \times (W_{des}/L_{des})$ is selected such that $V_{T(ci)}$ is a V_{GS} value in the weakly inverted region of the I - V characteristic curve

By the definition of I_{VT} , the linear $V_{T(ci)}$ shift relates to the V_{GS} associated with the same amount of inversion charge density during the BTI stress. As such, it is directly related to the induced voltage flat band shift and mainly dependent on the V_{GSstr} during BTI aging in a capacitor-like ($V_{DSstr} = 0$) stress configuration.

The $V_{T(ci)}$ extraction methodology is described in Figure 2 where, in this case, $V_{T(ci)}$ is obtained in the following steps:

- 1) Measure the I - V curve with a given V_{GS} step at the applied V_{DS} and V_{WS} bias conditions.
- 2) For the $V_{GS(i)}$ and $V_{GS(i-1)}$ values corresponding to $I_D(i-1)$ and $I_D(i)$ (absolute values) such that $I_D(i-1) < I_{VT} < I_D(i)$ is used to estimate $V_{T(ci)}$ by the linear interpolation:

$$V_{T(ci)} = V_{GS(i)} - [V_{GS(i)} - V_{GS(i-1)}] \times \left[\frac{\log I_D(i)/I_{VT}}{\log I_D(i)/I_{D(i-1)}} \right] \quad (1)$$