

JEDEC STANDARD

GRAPHICS DOUBLE DATA RATE (GDDR6) SGRAM STANDARD

JESD250C

(Revision of JESD250B, November 2018)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Contents

1 SCOPE	1
2 GDDR6 SGRAM STANDARD OVERVIEW	2
2.1 FEATURES	2
2.2 FUNCTIONAL DESCRIPTION	3
2.3 DEFINITION OF SIGNAL STATE TERMINOLOGY	4
2.4 DEFINITION OF CLOCKING TERMINOLOGY	4
2.5 CLOCKING	5
2.6 STATE DIAGRAM	8
3 INITIALIZATION	10
3.1 POWER-UP SEQUENCE	10
3.2 INITIALIZATION WITH STABLE POWER	13
3.3 VENDOR ID	14
4 ADDRESS	18
4.1 COMMAND and ADDRESSING	18
4.2 COMMAND ADDRESS BUS INVERSION (CABI)	19
4.3 BANK GROUPS	20
5 TRAINING	22
5.1 INTERFACE TRAINING SEQUENCE	22
5.2 COMMAND ADDRESS TRAINING	23
5.3 WCK2CK TRAINING	28
5.4 READ TRAINING	35
5.5 WRITE TRAINING	40
6 MODE REGISTERS	43
6.1 MODE REGISTER 0 (MR0)	45
6.2 MODE REGISTER 1 (MR1)	47
6.3 MODE REGISTER 2 (MR2)	49
6.4 MODE REGISTER 3 (MR3)	52
6.5 MODE REGISTER 4 (MR4)	54
6.6 MODE REGISTER 5 (MR5)	56
6.7 MODE REGISTER 6 (MR6) & MODE REGISTER 9 (MR9)	58
6.8 MODE REGISTER 7 (MR7)	63
6.9 MODE REGISTER 8 (MR8)	65
6.11 MODE REGISTER 11 (MR11)	69
6.12 MODE REGISTER 12 (MR12)	71
6.14 MODE REGISTER 14 (MR14)	73
6.15 MODE REGISTER 15 (MR15)	74
7 OPERATION	76
7.1 COMMANDS	76
7.2 COMMAND, ADDRESS and WRITE DATA INPUT TIMINGS	78
7.3 NO OPERATION (NOP)	78
7.4 MODE REGISTER SET	79
7.5 ROW ACTIVATION	80
7.6 BANK RESTRICTIONS	81
7.7 WRITE (WOM)	82
7.8 WRITE DATA MASK (DM)	89
7.9 MASKED WRITE DATA TIMING CONSTRAINTS	97
7.10 READ	98
7.11 DQ PREAMBLE	105
7.12 RDQS MODE	107
7.13 READ and WRITE DATA BUS INVERSION (DBI)	108
7.14 ERROR DETECTION CODE (EDC)	110
7.15 PRECHARGE	115
7.16 AUTO PRECHARGE	115
7.17 REFRESH and PER-BANK / PER-2-BANK REFRESH	116
7.18 REFRESH MANAGEMENT	124
7.19 SELF REFRESH	125
7.20 HIBERNATE SELF REFRESH	128
7.21 HIBERNATE SELF REFRESH WITH VDDQ OFF	129
7.22 POWER-DOWN	130

7.23 COMMAND TRUTH TABLES	132
7.24 CLOCK FREQUENCY CHANGE SEQUENCE	136
7.25 DYNAMIC VOLTAGE SWITCHING (DVS)	137
7.26 TEMPERATURE SENSOR	139
7.27 DUTY CYCLE CORRECTOR (DCC)	140
8 OPERATING CONDITIONS.....	141
8.1 ABSOLUTE MAXIMUM RATINGS.....	141
8.2 PAD CAPACITANCES	141
8.3 PACKAGE ELECTRICAL SPECIFICATION	142
8.4 PACKAGE THERMAL CHARACTERISTICS	143
8.5 ELECTROSTATIC DISCHARGE SENSITIVITY CHARACTERISTICS	143
8.6 AC & DC OPERATING CONDITIONS	144
8.7 POD I/O SYSTEM	149
8.8 IDD and IPP PARAMETERS and TEST CONDITIONS	153
8.9 AC TIMINGS	160
8.10 CLOCK-TO-DATA TIMING SENSITIVITY	167
8.11 1.35V I/O DRIVER MODELS	168
8.12 1.25V I/O DRIVER MODELS	171
9 PACKAGE SPECIFICATION	174
9.1 BALL-OUT	174
9.2 SIGNALS	175
9.3 ON DIE TERMINATION (ODT)	176
9.4 PACKAGE OUTLINE	177
9.5 x8 MODE ENABLE	178
9.6 PSEUDO-CHANNEL (PC) MODE	182
10 IEEE.1149.1 BOUNDARY SCAN	185
10.1 TEST PINS	185
10.2 TAP CONTROLLER	186
10.3 TAP REGISTERS	187
10.4 TAP INSTRUCTION SET	190
10.5 BOUNDARY SCAN OPERATION	192
10.6 INTERACTIONS BETWEEN BOUNDARY SCAN AND NORMAL DEVICE OPERATION	193
11 Annex A (informative) Differences between JESD250C and JESD250B	194

GRAPHICS DOUBLE DATA RATE 6 (GDDR6) SGRAM

(From JEDEC Board Ballot JCB-20-59, formulated under the cognizance of the JC-42.3 Subcommittee on Dynamic RAMs (DDRx.)

1 SCOPE

This document defines the Graphics Double Data Rate 6 (GDDR6) Synchronous Graphics Random Access Memory (SGRAM) specification, including features, functionality, package, and pin assignments.

The purpose of this Standard is to define the minimum set of requirements for 8 Gb through 16 Gb x16 dual channel GDDR6 SGRAM devices. System designs based on the required aspects of this standard will be supported by all GDDR6 SGRAM vendors providing compatible devices. Some aspects of the GDDR6 standard such as AC timings and capacitance values were not standardized. Some features are optional and therefore may vary among vendors. In all cases, vendor data sheets should be consulted for specifics. This document was created based on some aspects of the GDDR5 Standard (JESD212).

2 GDDR6 SGRAM STANDARD OVERVIEW

8 Gb	=	2 Channels 256Mb x 16	2 x (16Mb x 16 x 16 banks)	/	2 Channels 512Mb x 8	2 x (32Mb x 8 x 16 banks)
12 Gb	=	2 Channels 384Mb x 16	2 x (24Mb x 16 x 16 banks)	/	2 Channels 768Mb x 8	2 x (48Mb x 8 x 16 banks)
16 Gb	=	2 Channels 512Mb x 16	2 x (32Mb x 16 x 16 banks)	/	2 Channels 1Gb x 8	2 x (64Mb x 8 x 16 banks)
24 Gb	=	2 Channels 768Mb x 16	2 x (48Mb x 16 x 16 banks)	/	2 Channels 1.5Gb x 8	2 x (96Mb x 8 x 16 banks)
32 Gb	=	2 Channels 1Gb x 16	2 x (64Mb x 16 x 16 banks)	/	2 Channels 2Gb x 8	2 x (128Mb x 8 x 16 banks)

2.1. FEATURES

- 2 separate independent channels with point-to-point interface for data, address and command
- Half CA data rate differential clock inputs CK_t/CK_c for CMD/ADD (CA) per 2 channels
- Four half data rate or quarter data rate differential clock inputs WCK_t/WCK_c, each associated with a data byte (DQ, DBI_n, EDC) or Two quarter data rate or half data rate differential clock input WCK_t/WCK_c, each associated with the two bytes in the channel (Vendor specific)
- Double Data Rate (DDR) or Quad Data Rate (QDR) data (with regards to the WCK) (Vendor specific)
- Double Data Rate (DDR) Command Address (with regards to the CK)
- 16 internal banks
- 4 bank groups for t_{CCDL} = 3 t_{CK} and 4 t_{CK}
- 16n prefetch architecture: 256 bit per array read or write access per channel
- Burst length: 16 only
- Programmable READ latency: 9 to 36 t_{CK}
- Programmable WRITE latency: 5 to 8 t_{CK}
- WRITE Data mask function via CA bus (single/double byte mask)
- Data bus inversion (DBI) & Command Address bus inversion (CABI)
- Input/output PLL/DLL on/off mode
- Command Address training: command address input monitoring by DQ/DBI_n/EDC signals
- WCK2CK clock training with phase information by EDC signals
- Data read and write training via READ FIFO (depth 6)
- READ FIFO pattern preload by LDFF command
- Direct write data load to READ FIFO by WRTR command
- Consecutive read of READ FIFO by RDTR command
- Read/Write data transmission integrity secured by cyclic redundancy check using either a half or full data rate CRC
- READ/WRITE EDC on/off mode
- Programmable EDC hold pattern for CDR
- Programmable CRC READ latency = 1 to 4 t_{CK} and CRC WRITE latency = 10 to 16 t_{CK}
- Low Power modes
- On-chip temperature sensor with read-out
- Auto precharge option for each burst access
- Auto refresh & self refresh modes
- 32ms, auto refresh (16k cycles)
- Temperature sensor controlled self refresh rate and Partial Array Self Refresh
- Per-Bank / Per-2-Bank Refresh
- Optional digital t_{RAS} lockout
- On-die termination (ODT)
- ODT and output driver strength auto-calibration with external resistor ZQ
- Programmable termination and driver strength offsets (40 ohm to 60ohm)
- Internal V_{REF} for data inputs and CA inputs with programmable levels
- Separate internal V_{REF} for CA (Command / Address) inputs
- Vendor ID1 and ID2 for identification
- x16/x8 mode configuration set at power-up with EDC
- Pseudo-channel mode (PC mode) configuration set at power up with CA6
- 1.35V +/- 0.0405V supply for device operation (V_{DD})
- 1.35V +/- 0.0405V supply for I/O interface (V_{DDQ})
- 1.8 + 0.108V / - 0.054V supply for V_{PP}
- 180 ball BGA package with 0.75mm pitch

2.2 FUNCTIONAL DESCRIPTION

The GDDR6 SGRAM is a high-speed dynamic random-access memory designed for applications requiring high bandwidth. GDDR6 devices contain the following number of bits:

8 Gb has 8,589,934,592 bits
12 Gb has 12,884,901,888 bits
16 Gb has 17,179,869,184 bits
24 Gb has 25,769,803,776 bits
32 Gb has 34,359,738,368 bits

The GDDR6 SGRAM's high-speed interface is optimized for point-to-point connections to a host controller. On-die termination (ODT) is provided for all high-speed interface signals to eliminate the need for termination resistors in the system.

GDDR6 uses a 16n prefetch architecture and a DDR or QDR interface to achieve high-speed operation. The device's architecture consists of two 16 bit wide fully independent channels.

GDDR6 operates from a differential clock CK_t and CK_c. CK is common to both channels. Command and Address (CA) are registered at every rising edge of CK and every falling edge of CK. There are both single cycle and multi cycle commands. See command truth table for details.

GDDR6 uses a free running differential forwarded clock (WCK_t/WCK_c) with both input and output data registered and driven respectively at both edges of the forwarded WCK. See Clocking section for details.

Read and write accesses to GDDR6 are burst oriented; accesses start at a selected location and consists of a total of sixteen data words. Accesses begin with the registration of an Activate command, which is then followed by a Read, Write (WOM) or masked Write (WDM, WSM) command.

The row and bank address to be accessed is registered coincident with the Activate command. The address bits registered coincident with the Read, Write or masked Write command are used to select the bank and the starting column location for the burst access.

This specification includes all features and functionality required for GDDR6 SGRAM devices. In many cases the GDDR6 specification describes the behavior of a single channel.

2.3 DEFINITION OF SIGNAL STATE TERMINOLOGY

GDDR6 SGRAM will be operated in both ODT Enable (terminated) and ODT Disable (unterminated) modes. For highest data rates it is recommended to operate in the ODT Enable mode. ODT Disable mode is designed to reduce power and may operate at reduced data rates. There exist situations where ODT Enable mode can not be guaranteed for a short period of time, i.e., during power up.

Following are four terminologies defined for the state of a device (GDDR6 SGRAM or controller) signal during operation. The state of the bus will be determined by the combination of the device signal connected to the bus in the system. For example, in GDDR6 it is possible for the SGRAM pin to be tristated while the controller signal is HIGH or ODT. In both cases the bus would be HIGH if the ODT is enabled. For details on the device's signals and their function see Sections 9.1 and 9.2.

Device pin signal level:

- HIGH: A device signal is driving the Logic "1" state.
- LOW: A device signal is driving the Logic "0" state.
- Hi-Z: A device signal is tristate.
- ODT: A device signal terminates with ODT setting, which could be terminating or tristate depending on Mode Register setting.

Bus signal level:

- HIGH: One device on bus is HIGH and all other devices on bus are either ODT or Hi-Z. The voltage level on the bus would be nominally V_{DDQ} .
- LOW: One device on bus is Low and all other devices on bus are either ODT or Hi-Z. The voltage level on the bus would be nominally $V_{OL(DC)}$ if ODT was enabled, or V_{SS} if Hi-Z.
- Hi-Z: All devices on bus are Hi-Z. The voltage level on bus is undefined as the bus is floating.
- ODT: At least one device on bus is ODT and all others are Hi-Z. The voltage level on the bus would be nominally V_{DDQ} .

2.4 DEFINITION OF CLOCKING TERMINOLOGY

- Data refers to the signal being clocked (e.g. DQ by WCK and CA by CK)
- Half rate: clock is running at half of the data rate (e.g. WCK 4GHz and DQ at 8Gbps, or CK 1GHz and CA at 2Gbps)
- Quarter rate: clock is running at a quarter of the data rate (e.g. WCK 2GHz and DQ at 8Gbps)
- Eighth rate: clock is running at one eighth of the data rate (e.g. WCK internal 1GHz and DQ at 8Gbps)
- DDR (Double Data Rate): complement to half rate, referring to data relative to clock
- QDR (Quad Data Rate): complement to quarter rate, referring to data relative to clock
- ODR (Octa Data Rate): complement to eighth rate, referring to data relative to clock

2.5 CLOCKING

The GDDR6 SGRAM supports two operating modes for WCK frequency which differ in the DQ/DBI_n pin to WCK clock frequency ratio. The GDDR6 SGRAM supports DDR and QDR operating modes for WCK frequency which differ in the DQ/DBI_n to WCK clock frequency ratio.

Figure 1 illustrates the difference between a DDR WCK and a QDR WCK. Figure 61 illustrates a WRITE command with a DDR WCK clock while Figure 62 illustrates a WRITE command with a QDR WCK clock. Figure 76 illustrates a READ command with DDR WCK clocking and Figure 77 illustrates a READ command with QDR WCK clocking. Other figures in the specification are shown only with the DDR WCK for simplicity unless otherwise noted.

GDDR6 SGRAM also supports 2 granularities for the WCK data clock in the device. GDDR6 SGRAM devices can be designed with either a WCK/byte or a WCK/word. The ball-out has provisions for a WCK/byte but also supports WCK/word with the unused WCK balls as NC; the host must turn the unused WCK off.

The DRAM info bits for WCK Granularity, WCK Frequency and Internal WCK can be read by the host during the initialization process to determine the WCK architecture for the device and for devices that support multiple frequencies, MR10 OP9 allows for the mode to be set. For the frequencies for each mode see Table 73.

In both WCK QDR and DDR modes the GDDR6 device operates from a differential clock CK_t and CK_c. Command and Address (CA) are registered at every rising and falling CK edge. For both WCK DDR and QDR ratio the GDDR6 device can support either a full data rate EDC or a half data rate EDC. See EDC section for more details.

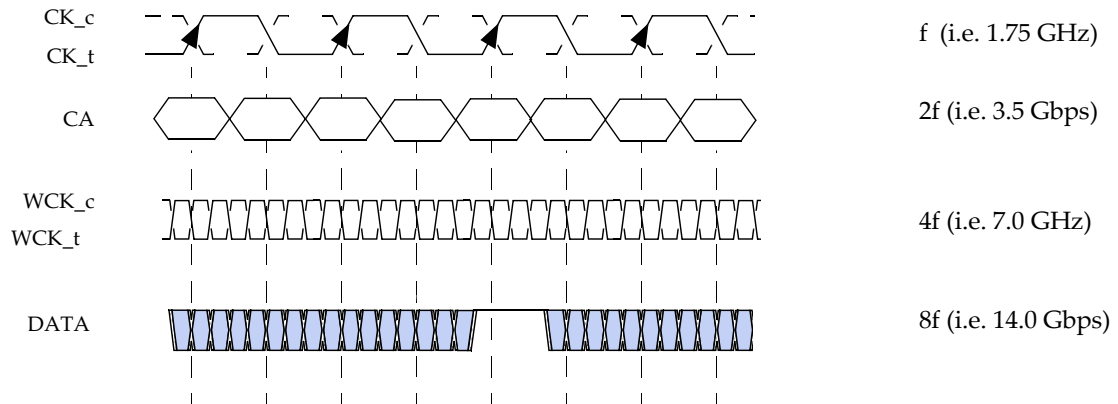
A rising CK (or WCK) edge is defined as the crossing of the positive edge of CK_t (or WCK_t) and the negative edge of CK_c (or WCK_c). A falling CK (or WCK) edge is defined as the crossing of the negative edge of CK_t (or WCK_t) and the positive edge of CK_c (or WCK_c).

Table 1 — Example Clock and Interface Signal Frequency Relationship

PIN	DDR WCK		QDR WCK		UNIT
CK_t, CK_c	1.5		1.5		GHz
CA	3.0		3.0		Gbps/pin
WCK_t, WCK_c	6.0		3.0		GHz
DQ, DBI_n	12.0		12.0		Gbps/pin
EDC	6.0	12.0	6.0	12.0	Gbps/pin

2.5 CLOCKING (cont'd)

DDR WCK



QDR WCK

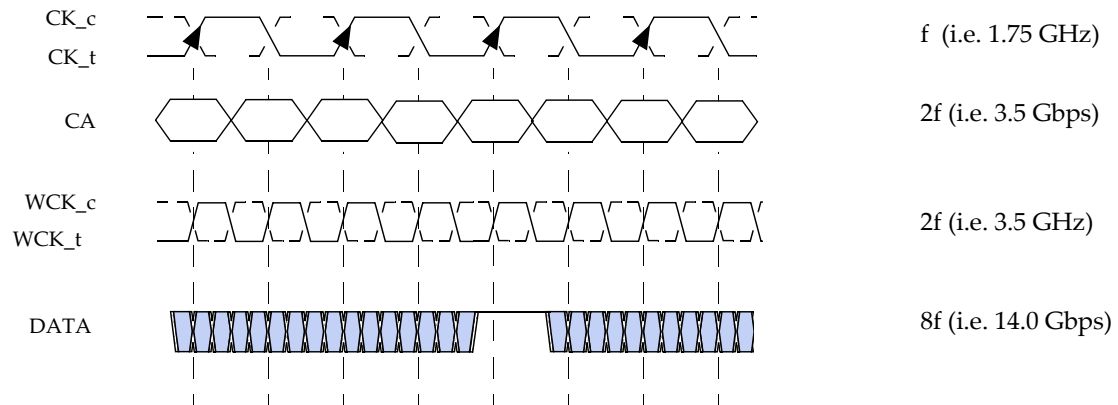


Figure 1 — GDDR6 Clocking and Interface Relationship

2.5 CLOCKING (cont'd)

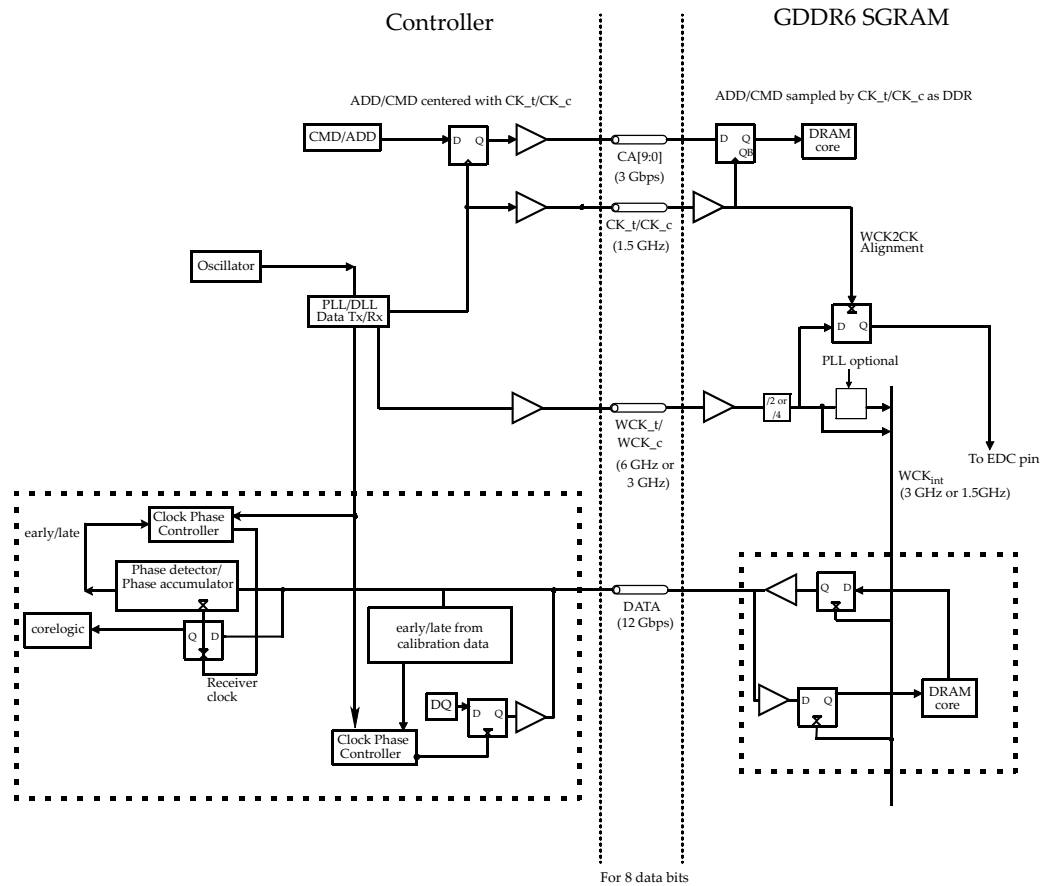


Figure 2 — Block Diagram of an example clock system

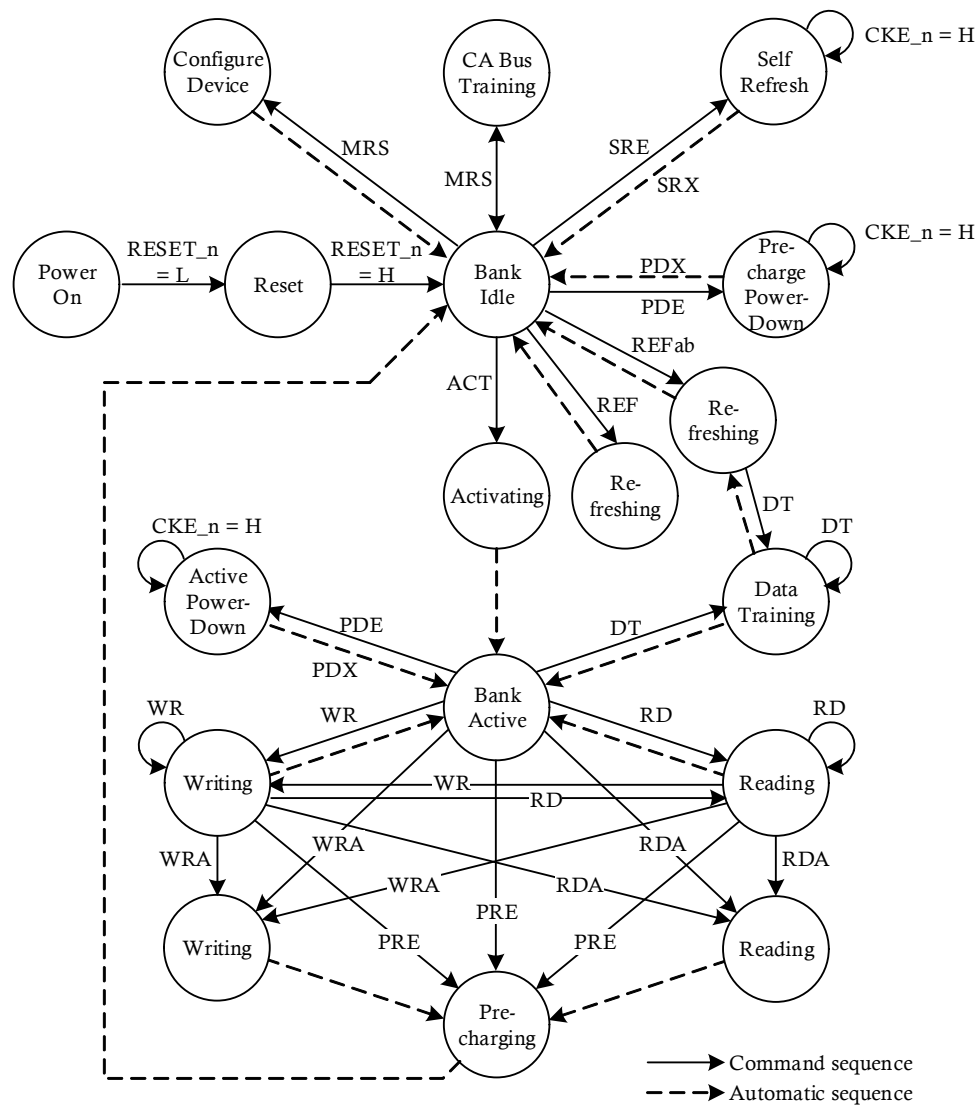
2.6 STATE DIAGRAM

The state diagram provides a simplified illustration of the allowed state transitions and the related commands to control them. The following operations are not or not completely shown in the diagram:

- state transitions involving more than one bank;
- device configurations set at the exit from reset state, including x16/x8 mode and 2 channel mode vs. PC mode;
- enabling or disabling of on-die termination;
- reading the Vendor ID or temperature sensor via the DQ bus;
- the procedures for WCK2CK training, clock frequency change and dynamic voltage switching (DVS);
- the suppression of a read or write data transfer by the use of the CE bit as part of READ (RD, RDTR) and WRITE (WOM, WDM, WSM, WRTR) commands, intended to be used with PC mode;
- variations of self refresh mode like hibernate self refresh and hibernate self refresh with VDDQ Off;
- the immediate transition from any state to reset state by asserting RESET_n LOW or by loading one of the boundary scan instructions EXTEST, CLAMP or HIGH-Z.

For a complete description of the device behavior, use the information provided in the state diagram along with the command truth tables and AC timing specifications.

2.6 STATE DIAGRAM (cont'd)



Code	Command	Code	Command
ACT	ACTIVATE	REF	REFpb or REFp2b; RFMab, RFMpb or RFMp2b
PRE	PREab or PREpb	REFab	REFab
RD	READ	MRS	MODE REGISTER SET
RDA	READ w/ AP	PDE	POWER-DOWN ENTRY
WR	WOM, WDM or WSM	PDX	POWER-DOWN EXIT
WRA	WOM, WDM or WSM w/ AP	SRE	SELF REFRESH ENTRY
DT	LDFF, WRTR or RDTR	SRX	SELF REFRESH EXIT

Figure 3 — Simplified State Diagram

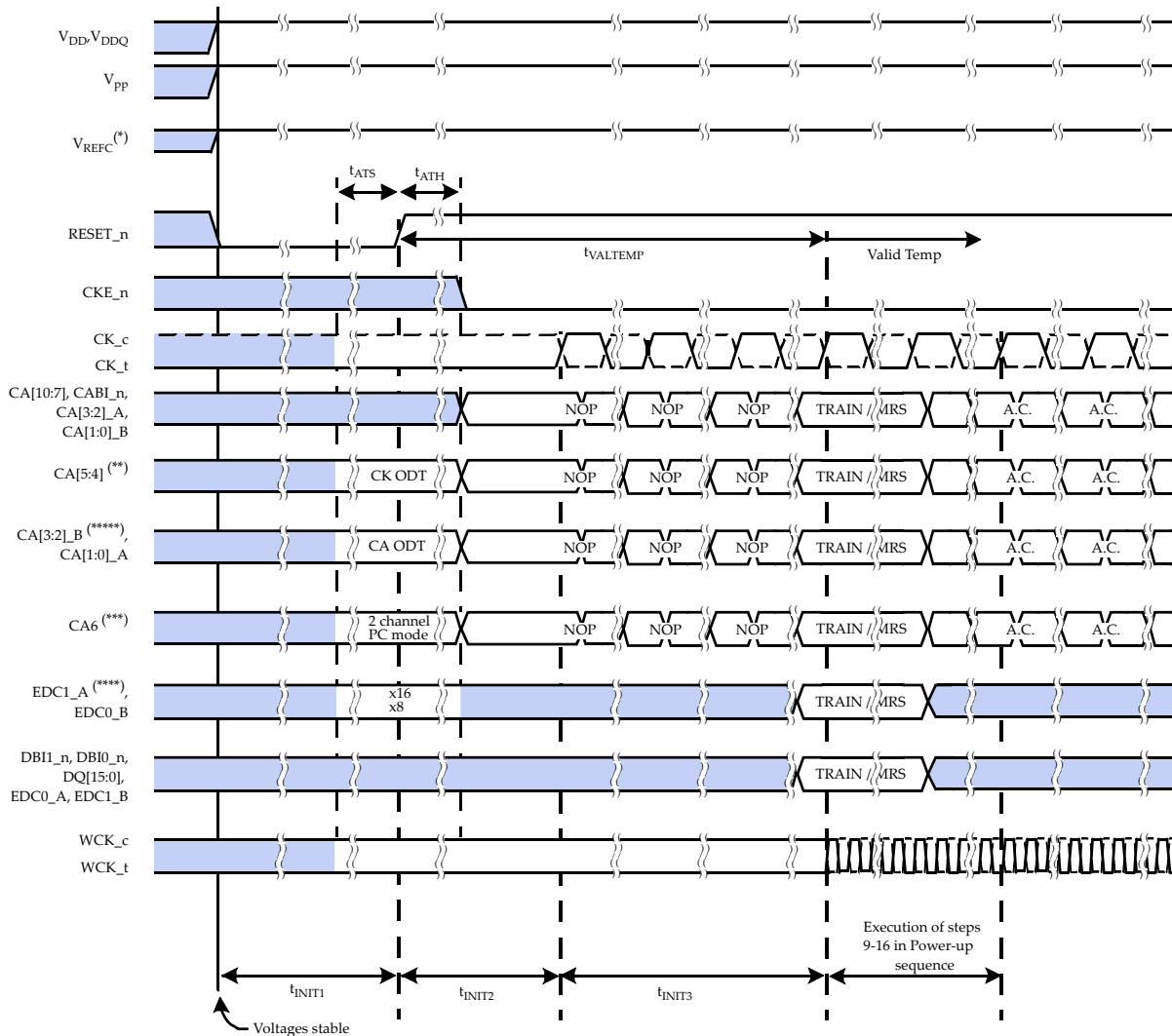
3 INITIALIZATION

3.1 POWER-UP SEQUENCE

GDDR6 SGRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The Mode Registers do not have RESET default values, except for CABI, CA termination, and the EDC hold pattern. If the mode registers are not set during the initialization sequence, it may lead to unspecified operation.

- 1) Apply power to V_{PP} . Apply power to V_{DD} at the same time or after power is applied to V_{PP} . Apply power to V_{DDQ} at the same time or after power is applied to V_{DD} . V_{PP} must be equal to or higher than V_{DD} at all times the device is powered up except during power-off sequence.
- 2) Apply V_{REFC} at same time or after power is applied to V_{DDQ} , or pull V_{REFC} LOW to select internal V_{REFC} .
- 3) The voltage levels on all signal balls must be less than or equal to V_{DD} and V_{DDQ} on one side and must be larger than or equal to V_{SS} on the other side.
- 4) Assert RESET_n LOW to ensure all drivers are in Hi-Z and all ODT are off. Maintain RESET_n LOW for a minimum time of t_{INIT1} .
- 5) Set system configuration info at least a time t_{ATS} before RESET_n is driven HIGH:
 - a. Drive CA[5:4]_A and CA[5:4]_B both LOW or HIGH for the desired CK ODT
 - b. Drive EDC1_A and EDC0_B both HIGH for x16 mode or LOW for x8 mode
 - c. Drive CA6_A and CA6_B both HIGH for 2 channel mode or LOW for PC mode
 - d. Drive CA1_A and CA0_A per Table 3 to select CA bus termination strength for Channel A.
 - e. Drive CA3_B and CA2_B per Table 3 to select CA bus termination strength for Channel B
 - d. Drive CK_t, WCK_t to static LOW level, and CK_c, WCK_c to static HIGH level.After meeting t_{ATS} requirement, drive RESET_n HIGH
- 6) After RESET_n is pulled HIGH, maintain CA[6:0] and EDC signals stable for a minimum time of t_{ATH} .
- 7) Pull CKE_n LOW after t_{ATH} is satisfied. Assert and hold NOP command. The device performs the initial impedance calibration during this time; this will be done without external clocks. Latest after t_{INIT2} the device enables the CK and CA ODT as determined in steps 5 and 6.
- 8) Provide a stable CK clock for a minimum of t_{INIT3} cycles. Maintain a stable CK clock indefinitely. The CK clock may only be stopped when the device is put into self refresh (see Self Refresh for timing requirements on stopping and enabling the CK clock). The device state will be undefined when the CK clock is stopped outside of self refresh, and a chip reset as outlined in the Initialization with Stable Power section would be required before the GDDR6 SGRAM can return to normal operation.
- 9) Issue MRS command to MR15 to set the device into CA training mode (optional).
- 10) Complete CA training (optional).
- 11) Issue MRS command to read the Vendor ID (optional).
- 12) Issue MRS command to set WCK termination values.
- 13) Provide stable WCK clocks.
- 14) Issue MRS commands to the mode registers in any order. Issue MRS commands to use PLL or not, to select the position of a WCK2CK alignment point and WCK ratio, and to set WLMrs, RLMrs, CRCWL, and CRCRL to appropriate values. All these features must be programmed before WCK2CK training, and t_{MOD} must be met during this procedure.
- 15) Issue two REFab commands followed by NOP until t_{RFCab} is satisfied.
- 16) After any necessary training sequences such as WCK2CK training, READ training (LDFF, RDTR) and WRITE training (WRTR, RDTR), the device is ready for normal operation.

3.1 POWER-UP SEQUENCE (cont'd)



- Notes:
- CA10 is only present in 24 Gb and 32 Gb densities
 - A.C. = Any Command
 - (*) Pull VREFC ball to VSS to select internal VREFC
 - (**) Drive CA[5:4] HIGH or LOW to select default CK ODT
 - (***) Drive CA6 HIGH or LOW to select either 2 channel or PC mode
 - (****) Drive EDC HIGH or LOW to select x8 or x16 mode
 - (*****) Drive CA[3:2]_B and CA[1:0]_A HIGH or LOW to select default CA ODT

Don't Care

Figure 4 — Power-up Initialization

3.1 POWER-UP SEQUENCE (cont'd)

Table 2 — Device Initialization Timings

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
RESET_n initial LOW time after power-up	t_{INIT1}	200	–	μ s	
Time after RESET_n de-assertion before starting the CK clock	t_{INIT2}	1	–	ms	
Stable CK clock cycles before issuing valid commands	t_{INIT3}	100	–	t_{CK}	
CA[6:0] and EDC setup time before RESET_n de-assertion	t_{ATS}	10	–	ns	
CA[6:0] and EDC hold time after RESET_n de-assertion	t_{ATH}	10	–	ns	
RESET_n LOW time with stable power	t_{RES}	100	–	ns	
Temperature sensing time after RESET_n deassertion	$t_{VALTEMP}$	1.5		ms	

Table 3 — CA Termination

CA[3:2]_B or CA[1:0]_A at RESET_n high transition	Termination for CA[3:0]	Termination with CA6 LOW for CA[10:4], CABI_n & CKE_n	Termination with CA6 HIGH for CA[10:4], CABI_n & CKE_n
LOW, LOW	Disabled	Disabled	Disabled
LOW, HIGH	60 Ohms	120 Ohms	60 Ohms
HIGH, LOW	120 Ohms	240 Ohms	120 Ohms
HIGH, HIGH	Reserved	Reserved	Reserved

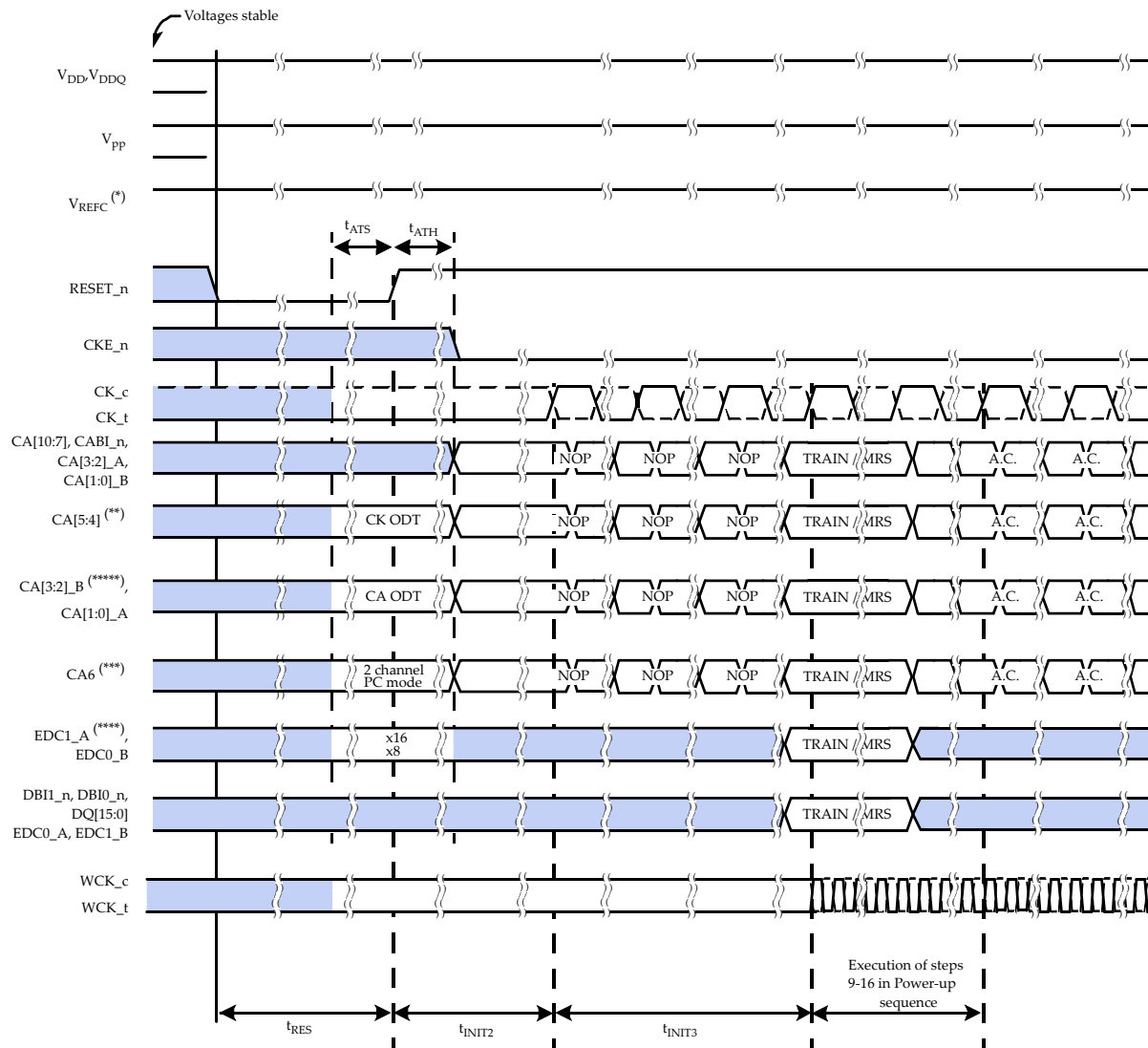
Table 4 — CK Termination

CA5_A CA5_B	CA4_A CA4_B	Default CK Termination Value
LOW	X	Disabled
HIGH	LOW	60 Ohm
HIGH	HIGH	120 Ohm

3.2 INITIALIZATION WITH STABLE POWER

The following sequence is required for reset subsequent to power-up initialization. This requires that the power has been stable within the specified V_{DD} , V_{DDQ} and V_{PP} ranges since power-up initialization (see Figure 5):

- 1) Assert RESET_n LOW anytime when reset is needed.
- 2) Hold RESET_n LOW for minimum t_{RES} . Assert and hold NOP command.
- 3) Continue with step 5 of the power-up initialization sequence.



- Notes:
- CA10 is only present in 24 Gb and 32 Gb densities
 - A.C. = Any Command
 - (*) Pull V_{REFC} ball to V_{SS} to select internal V_{REFC}
 - (**) Drive CA[5:4] HIGH or LOW to select default CK ODT
 - (***) Drive CA6 HIGH or LOW to select either 2 channel or PC mode
 - (****) Drive EDC HIGH or LOW to select x8 or x16 mode
 - (*****) Drive CA[3:2]_B and CA[1:0]_A HIGH or LOW to select default CA ODT

Don't Care

Figure 5 — Initialization with Stable Power

3.3 VENDOR ID

GDDR6 SGRAMs include a Vendor ID feature that allows the controller to receive information from the device to differentiate between different vendors and different devices using a software algorithm.

Vendor ID is part of the INFO field of Mode Register 3 (MR3) and is selected by issuing a MODE REGISTER SET command with MR3 OP[7:6] = 01 for ID1 and MR3 OP[7:6] = 11 for ID2. MR3 OP[11:8] and OP[5:0] are set to the desired values.

When the Vendor ID function is enabled the device information will be transmitted on the DQ bus as shown in Figure 6. The device will provide the Vendor ID as shown in Table 5 or Table 6 depending on whether ID1 or ID2 is selected. For x8 mode the 16 bits of Vendor ID information comes from 2 devices as only 1 data byte per channel per device is enabled.

Additional information can optionally be provided by the vendor using a vendor specific setting in the Reserved for Vendor Specific Features MR and will follow the same protocol as vendor ID unless explicitly stated in the vendor data sheet.

The Vendor ID will be driven onto the DQ bus after the MRS command that sets bits OP6 to 1 and OP7 to 0 for ID1 or to 1 for ID2. The DQ bus will be continuously driven until an MRS command sets MR3 OP6 and OP7 back to 0. The DQ bus will be in ODT state after $t_{WRIDOFF}(max)$. The code can be sampled by the controller after waiting $t_{WRIDON}(max)$ and before $t_{WRIDOFF}(min)$. DBI is not enabled or ignored during all Vendor ID operations.

The EDC hold pattern is continuously driven on the EDC signals provided a stable WCK clock is applied.

Table 5 — Vendor ID to DQ Mapping - ID1 (MR3 OP[7:6] = 01)

DQ15_A DQ15_B	DQ[14:13]_A DQ[14:13]_B	DQ12_A DQ12_B	DQ11_A DQ11_B	DQ[10:8]_A DQ[10:8]_B	DQ[7:4]_A DQ[7:4]_B	DQ[3:0]_A DQ[3:0]_B
VDDQ OFF See Table 12	WCK Frequency see Table 11	WCK Granularity see Table 10	Internal WCK see Table 8	Density see Table 9	Revision ID	Manufacturers Vendor Code see Table 7

The Manufacturers Vendor Code, Revision ID and Density allow the host to differentiate which vendor's device, the revision of the device and the density used in the system. Internal WCK tells the host whether to use an invert or quad shift when programming MR10 OP[7:4]. WCK Granularity and WCK Frequency are used by the host to determine if the device in the has WCK/byte or WCK/word to allow the device to be properly trained and configured.

Table 6 — Vendor ID to DQ Mapping - ID2 (MR3 OP[7:6] = 11)

DQ15_A DQ15_B	DQ[14:13]_A DQ[14:13]_B	DQ[12:10]_A DQ[12:10]_B	DQ[9:3]_A DQ[9:3]_B	DQ2_A DQ2_B	DQ1_A DQ1_B	DQ0_A DQ0_B
RAA Counter Decrement per REF See Table 18	RAAMMT Value See Table 17	RAAIMT Value See Table 16	RFU ("1")	RFM See Table 15	PRBS See Table 14	Programmable P2BR See Table 13

Programmable P2BR allows the host to determine if the device has a register to select between MSB and LSB Don't Care when using REFp2b commands or the device has just LSB do not care when using REFp2b commands.

PRBS allows the host to determine if the optional PRBS feature in MR12 is supported by the device.

3.3 VENDOR ID (cont'd)

Table 7 — Manufacturers Vendor Code

DQ3_A DQ3_B	DQ2_A DQ2_B	DQ1_A DQ1_B	DQ0_A DQ0_B	Manufacturer's Name
0	0	0	1	Samsung
0	1	1	0	SK hynix
1	1	1	1	Micron
all others				Reserved

Table 8 — Internal WCK

DQ11_A DQ11_B	Internal WCK
0	Internal Quarter data rate WCK
1	Internal Eighth data rate WCK

Table 9 — Channel Density

DQ10_A DQ10_B	DQ9_A DQ9_B	DQ8_A DQ8_B	Channel (Device) Density
0	0	0	RFU
0	0	1	4 Gb (8 Gb)
0	1	0	6 Gb (12 Gb)
0	1	1	8 Gb (16 Gb)
1	0	0	12 Gb (24 Gb)
1	0	1	16 Gb (32 Gb)
all others			Reserved

Table 10 — WCK Granularity

DQ12_A DQ12_B	WCK Granularity
0	WCK/byte
1	WCK/word

Table 11 — WCK Frequency

DQ14_A DQ14_B	DQ13_A DQ13_B	WCK Frequency
0	0	Reserved
0	1	Half data rate WCK
1	0	Quarter data rate WCK
1	1	Both

Note: The vendor datasheet shall be consulted for the supported frequency ranges of QDR and DDR WCK in case a device supports both options.

3.3 VENDOR ID (cont'd)

Table 12 — VDDQ Off

DQ15_A DQ15_B	VDDQ off
0	Hibernate Self Refresh with VDDQ off not supported
1	Hibernate Self Refresh with VDDQ off supported

Table 13 — Programmable P2BR

DQ0_A DQ0_B	Programmable P2BR
0	Both LSB (BA0) and MSB (BA3) Don't Care for REFp2b supported
1	LSB (BA0) Don't Care only for REFp2b

Table 14 — PRBS

DQ1_A DQ1_B	PRBS
0	Optional PRBS is supported
1	Optional PRBS is not supported

Table 15 — RFM

DQ2_A DQ2_B	Refresh Management (RFM)
0	Refresh Management required
1	Refresh Management not required

Table 16 — RAA Initial Management Threshold (RAAIMT)

DQ[12:10]_A DQ[12:10]_B	RAAIMT Value
000	32
001	40
010	48
011	56
100	64
101	72
110	80
111	Reserved

3.3 VENDOR ID (cont'd)

Table 17 — RAA Maximum Management Threshold (RAAMMT)

DQ[14:13]_A DQ[14:13]_B	RAAMMT Value
00	3 * RAAIMT
01	4 * RAAIMT
10	5 * RAAIMT
11	6 * RAAIMT

Table 18 — RAA Counter Decrement per REF Command

DQ[15]_A DQ[15]_B	RAA Counter Decrement per REF Command
0	RAAIMT
1	0.5 * RAAIMT

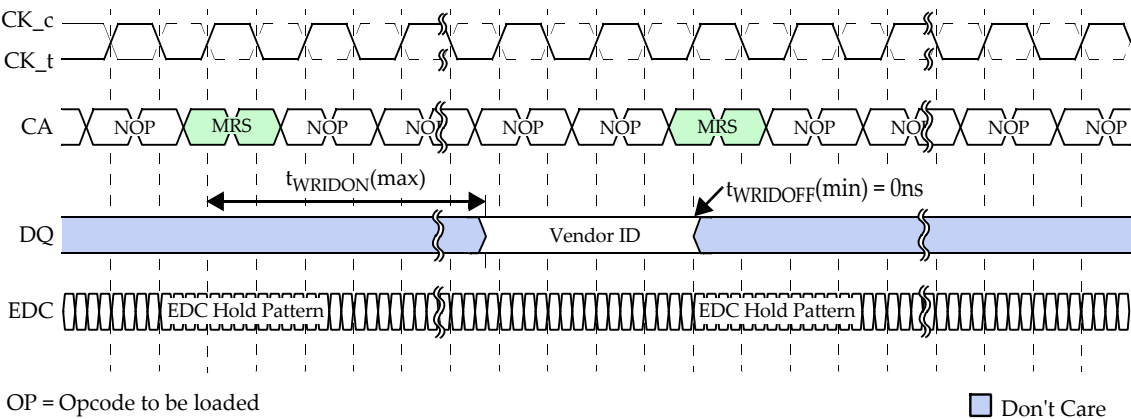


Figure 6 — Vendor ID Timing Diagram

4 ADDRESS

4.1 COMMAND and ADDRESSING

GDDR6 SGRAMs use a double data rate command address scheme to reduce balls required on the device. The command and address is packetized on the 10 CA signals (CA[9:0]) over either single cycle or multi cycles depending on the command (see Command Truth Table). For single cycle commands the command and address data is provided to the device in two parts; the first half is latched on the rising edge of CK; the second half is latched on the falling edge of CK. An 11th CA signal (CA10) is for 24 Gb and 32 Gb densities.

GDDR6 addressing is defined for a single channel with devices having 2 channels/device.

Table 19 — Addressing Scheme

Memory Density	8 Gb		12 Gb		16 Gb		24 Gb		32 Gb	
	8,589,934,592		12,884,901,888		17,179,869,184		25,769,803,776		34,359,738,368	
Device Organization	x16 mode	x8 mode	x16 mode	x8 mode	x16 mode	x8 mode	x16 mode	x8 mode	x16 mode	x8 mode
Number channels	2		2		2		2		2	
Channel Memory Density	4 Gb		6 Gb		8Gb		12Gb		16Gb	
Channel Density	4,294,967,296		6,442,450,944		8,589,934,592		12,884,901,888		17,179,869,184	
Array Pre-Fetch (bits, per channel)	256	128	256	128	256	128	256	128	256	128
Bank address (per channel)	BA[3:0]		BA[3:0]		BA[3:0]		BA[3:0]		BA[3:0]	
Number Banks (per channel)	16		16		16		16		16	
Row address (per channel)	R[13:0]	R[13:0]	R[13:0]	R[14:0]	R[13:0]	R[14:0]	R[14:0]	R[15:0]	R[14:0]	R[15:0]
Number of Rows (per channel)	16,384	16,384	12,288	24,576	16,384	32,768	24,576	49,152	32,768	65,536
Column address (per channel)	C[5:0]	C[6:0]	C[6:0]	C[6:0]	C[6:0]	C[6:0]	C[6:0]	C[6:0]	C[6:0]	C[6:0]
Page Size (per channel)	2K	2K	4K	2K	4K	2K	4K	2K	4K	2K
Refresh	16K/32ms		16K/32ms		16K/32ms		16K/32ms		16K/32ms	
Refresh period	1.9us		1.9us		1.9us		1.9us		1.9us	

NOTE

1. The column address notation for GDDR6 does not include the lower four address bits as the burst order is always fixed for READ and WRITE commands.
2. Row and column address values on the CA bus that are not used for a particular density must be at valid logic levels.
3. Page Size = $2^{\text{COLBITS}} * (\text{Prefetch_Size}/8)$ where COLBITS is the number of column address bits.
4. Row address range with R[14:13] = 11 for x8 and R[13:12] = 11 for x16 is not present for 12 Gb density
5. Row address range with R[15:14] = 11 for x8 and R[14:13] = 11 for x16 is not present for 24 Gb density

4.2 COMMAND ADDRESS BUS INVERSION (CABI)

Command Address Bus Inversion (CABI) reduces the power requirements on Command Address (CA) bus, as the number of CA lines driving a LOW level can be limited to 5 in 2 channel mode or 7 in PC mode for 8 Gb, 12 Gb and 16 Gb densities and limited to 6 in 2 channel mode or 8 in PC mode for 24 Gb and 32 Gb densities.

The Command Address Bus Inversion function is associated with the electrical signalling on the CA lines between a controller and the device, regardless of whether the information conveyed on the CA lines is a row or column address, a command, a mode register op-code, a data mask, or any other pattern.

The CABI_n input is an active LOW double data rate (DDR) signal and sampled by the device at the rising edge of CK and the falling edge of CK along with the CA inputs.

Once enabled by the corresponding CABI Mode Register bit, the GDDR6 SGRAM will invert the pattern received on the CA inputs in case CABI_n was sampled LOW, or leave the pattern non-inverted in case CABI_n was sampled HIGH, as shown in Figure 7.

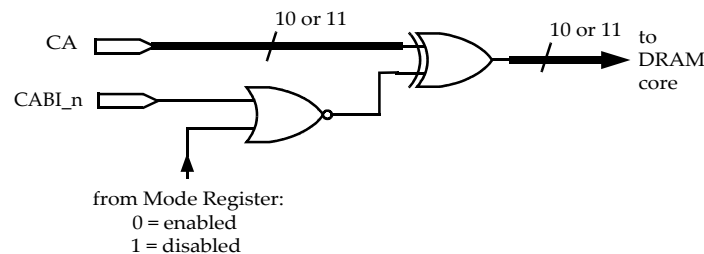
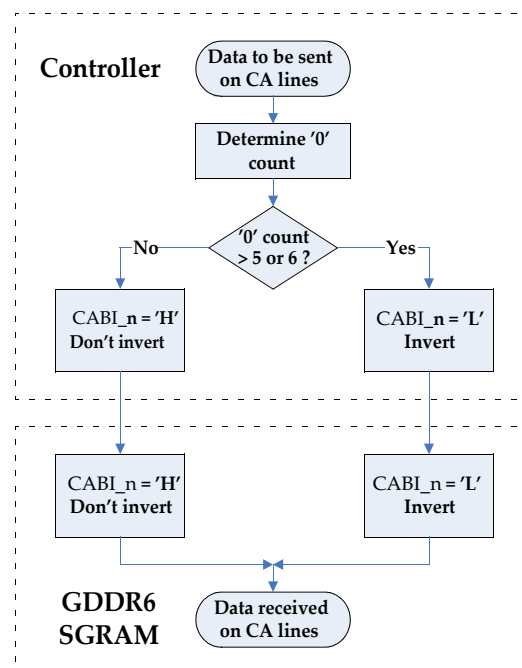


Figure 7 — Example of Command Address Bus Inversion Logic

The flow diagram in Figure 8 illustrates the CABI operation. The controller decides whether to invert or not invert the data conveyed on the CA lines. The GDDR6 SGRAM has to perform the reverse operation based on the level of CABI_n. CA input timing parameters are only valid with CABI being enabled and a maximum of 5, 6, 7 or 8 CA inputs driven LOW depending on the channel configuration.



Note: Figure shown for 2 channel configuration. In PC mode check for '0' count > 7 or 8

Figure 8 — Command Address Bus Inversion (CABI) Flow Diagram

4.3 BANK GROUPS

For devices operating at frequencies above a certain threshold (f_{CKBG}), the activity within a bank group must be restricted to ensure proper operation of the device. The 16 banks are divided into four bank groups. The bank groups feature is controlled by OP[11:10] in Mode Register 3 (MR3). The assignment of the banks to the bank groups is shown in Table 20.

Table 20 — Bank Groups

Bank	Addressing				16 banks
	BA3	BA2	BA1	BA0	
0	0	0	0	0	Group A
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	Group B
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	Group C
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	Group D
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

These bank groups allow the specification of different command delay parameters depending on whether back-to-back accesses are to banks within one bank group or across bank groups as shown in Table 21.

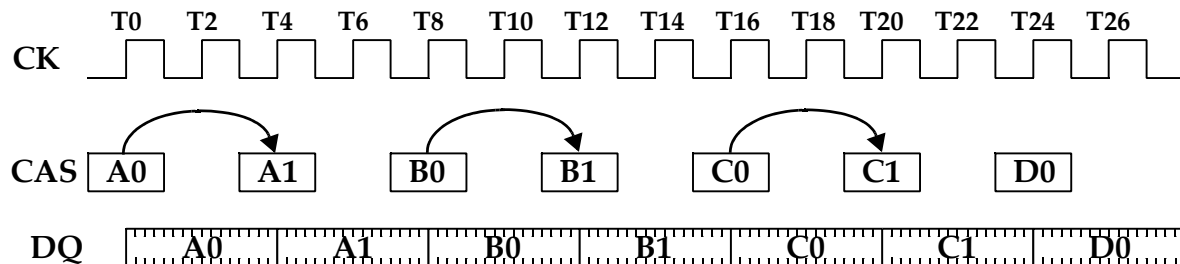
Table 21 — Command Sequences Affected by Bank Groups

Command Sequence	Corresponding AC Timing Parameter			Notes
	Bank Groups Disabled	Bank Groups Enabled		
		Accesses to a different bank group	Accesses within the same bank group	
ACTIVATE to ACTIVATE	t _{RRDS}	t _{RRDS}	t _{RRDL}	
WRITE to WRITE	t _{CCDS}	t _{CCDS}	t _{CCDL}	
READ to READ	t _{CCDS}	t _{CCDS}	t _{CCDL}	
Internal WRITE to READ	t _{WTRS}	t _{WTRS}	t _{WTRL}	
READ to PRECHARGE	t _{RTPS}	--	t _{RTPL}	1
NOTE 1: Parameters t _{RTPS} and t _{RTPL} apply only when READ and PRECHARGE go to the same bank; use t _{RTPS} when BG are disabled, and t _{RTPL} when BG are enabled.				

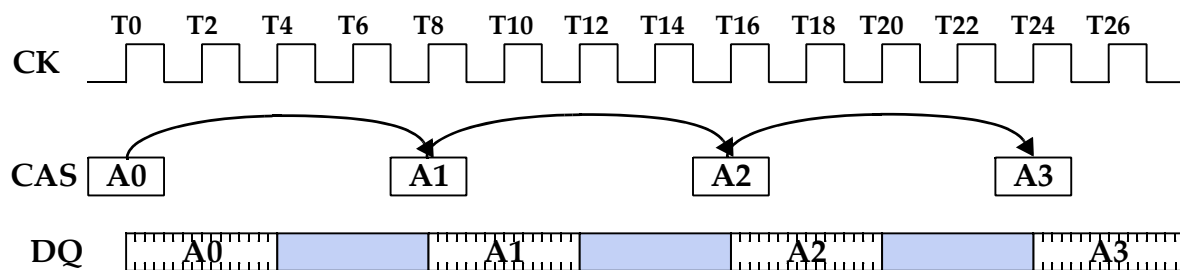
4.3 BANK GROUPS (cont'd)

Figure 9 shows back-to-back column accesses based on t_{CCDL} and t_{CCDS} parameters.

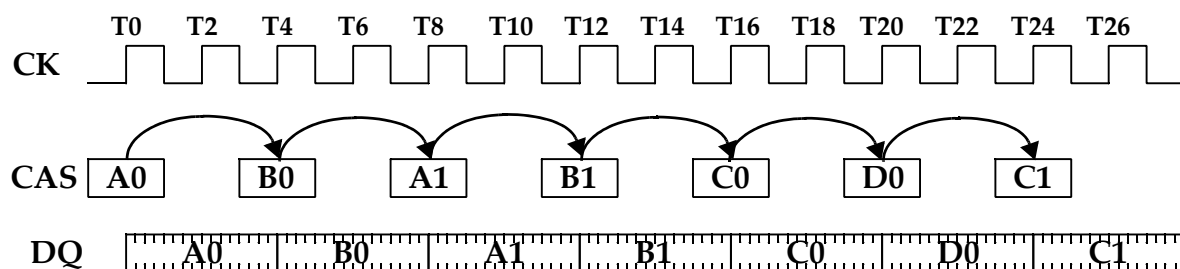
Example 1 (Bank Groups disabled): $t_{CCDS} = 2 * t_{CK}$



Example 2: (Bank Groups enabled): $t_{CCDL} = 4 * t_{CK}$



Example 3: (Bank Groups enabled): $t_{CCDS} = 2 * t_{CK}$



NOTE 1 Column accesses (CAS commands) are to open banks, and t_{RCD} has been met.

NOTE 2 $RL = 0$ assumed for illustration purposes

NOTE 3 Ax, Bx, Cx, Dx: accesses to bank groups A, B, C or D, respectively

NOTE 4 With bank groups enabled, t_{CCDL} is $3 t_{CK}$ or $4 t_{CK}$, as programmed in MR3.

Figure 9 — t_{CCDS} and t_{CCDL}

5 TRAINING

5.1 INTERFACE TRAINING SEQUENCE

Due to the high data rates of GDDR6, it is recommended that the interfaces be trained to operate with the optimal timings. GDDR6 SGRAM has features defined which allow for complete and efficient training of the I/O interface without the use of the device's memory array. The interface trainings are required for normal DRAM functionality unless deemed optional by the DRAM vendor or unless running in lower frequency modes as described in the low frequency section. Interface timings will only be guaranteed after all required trainings have been executed.

A recommended order of training sequences has been chosen based on the following criteria:

The Command Address (CA) training must be done first to allow full access to the Mode Registers. (MR15 for CA training is a special single data rate mode register guaranteed to work without training). CA input timing shall function without training as long as $t_{AS/H}$ are met.

WCK2CK training should be done before read training because a shift in WCK relative to CK will cause a shift in all READ timings relative to CK.

READ training should be done before WRITE training because optimal WRITE training depends on correct READ data. As part of WRITE training, the host not only has the ability to find the data-eye optimal position in the horizontal direction but also the ability to adjust VREFD levels using the mode registers to find the data-eye optimal position in the vertical direction.

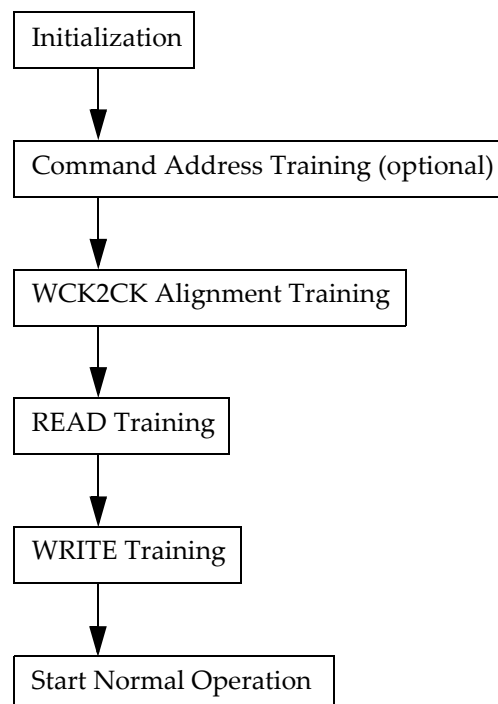


Figure 10 — Interface Training Sequence

5.2 COMMAND ADDRESS TRAINING

GDDR6 SGRAMs provide a means for Command Address (CA) bus interface training. The controller may use the CA training mode to improve the timing margins on the CA bus.

CA training mode is entered via the CADT bits in Mode Register 15 (MR15). Even though CA9 and CA8 are sampled on both rising and falling edge of CK, the command encoding allows relaxed timing to guarantee the setup and hold times can be met even though the CA bus timing has not yet been trained. When issuing an MRS command the increase in the CA8 timing around the rising edge of clock will lead to one of three different NOP encodings depending on the value on CA8 during the falling edges on either side of the clock rising edge. All NOPs are treated equally.

CA training mode uses an internal bridge between the device's CA inputs and DQ/DBI_n/EDC outputs. It also uses a special COMMAND ADDRESS TRAINING CAPTURE (CAT) command that is encoded using the SDR pin CKE_n. Once the device is placed into CA training mode, the only commands that can be interpreted use CKE_n = HIGH and are the CAT command, a CA training mapping change or CA training exit. When CKE_n = LOW, the CA inputs are do not care, no command is decoded and thus will be treated as a NOP. Once the CA training mode has been entered and t_{MOD} has been met, the CA values registered coincident with the CAT command will be transmitted to the controller on DQ/DBI_n/EDC. The controller is then expected to compare the CA pattern received to the expected value and to adjust the CA transmit timing accordingly. The procedure may be repeated using different CA patterns and interface timings. No WCK clock is required for this special CA training mode. The latched CA values are driven out asynchronously.

The CABI_n signal can be trained directly by using MR15 OP[3:2] = 11 or indirectly as part of a pass with MR15 OP[3:2] = 10 or 01 by enabling the CABI in MR1 OP10. When enabled by the CABI bit in Mode Register 1, command address bus inversion (CABI) is effective during CA training mode. It is suggested to train CABI_n's interface timing together with the other CA lines. CABI is enabled by default on power up or subsequent reset. If CABI is disabled, CABI_n (input) is ignored and CABI_n (output) is undefined during CA training.

CA training uses multiple passes to train all the CA signals for the rising and falling CK edge setup and hold times. Table 23 defines the correspondence between CA bits and DQ/DBI_n/EDC for all three passes.

When in CA training mode, two cycles of CKE_n = HIGH allows either the change of the mapping while in CA training mode or the exit of CA training mode. The first cycle of CKE_n = HIGH will be interpreted as a CAT command. In the case of a CA training exit, the first cycle of CKE_n = HIGH will be treated as a dummy CAT command as the CA training exit may disable the outputs before the pattern sent to the CA inputs is output on the data bus as t_{ADZ} may be shorter than t_{ADR} and should not be considered a valid training result. The second cycle will be interpreted as either an exit if MR15 OP[3:2] = 00 or a change to the mapping. While in CA training mode, t_{AS}/t_{AH} must be met for the second cycle of CKE_n = HIGH.

Devices configured to x8 mode reflect the CA on the one byte being enabled in that mode, specifically byte 0 in Channel A and byte 1 in Channel B. Devices configured to x16 mode reflect the CA on the same DQ as in x8 mode; in addition they are allowed but not required to reflect the CA on those bytes that are disabled in x8 mode, specifically byte 1 in Channel A and byte 0 in Channel B, thus reflecting each CA twice.

The timing diagram in Figure 11 illustrates the typical command sequence in CA training mode. The DQ/DBI_n/EDC output drivers are enabled as long as the CADT bits are set to either 01, 10 or 11. The minimum spacing between consecutive CAT commands is $2 t_{CK}$. The minimum spacing between consecutive CA training passes is t_{MOD} as shown in Figure 11. t_{MOD} is also to be met before the next valid command after the CA training exit.

5.2 COMMAND ADDRESS TRAINING (cont'd)

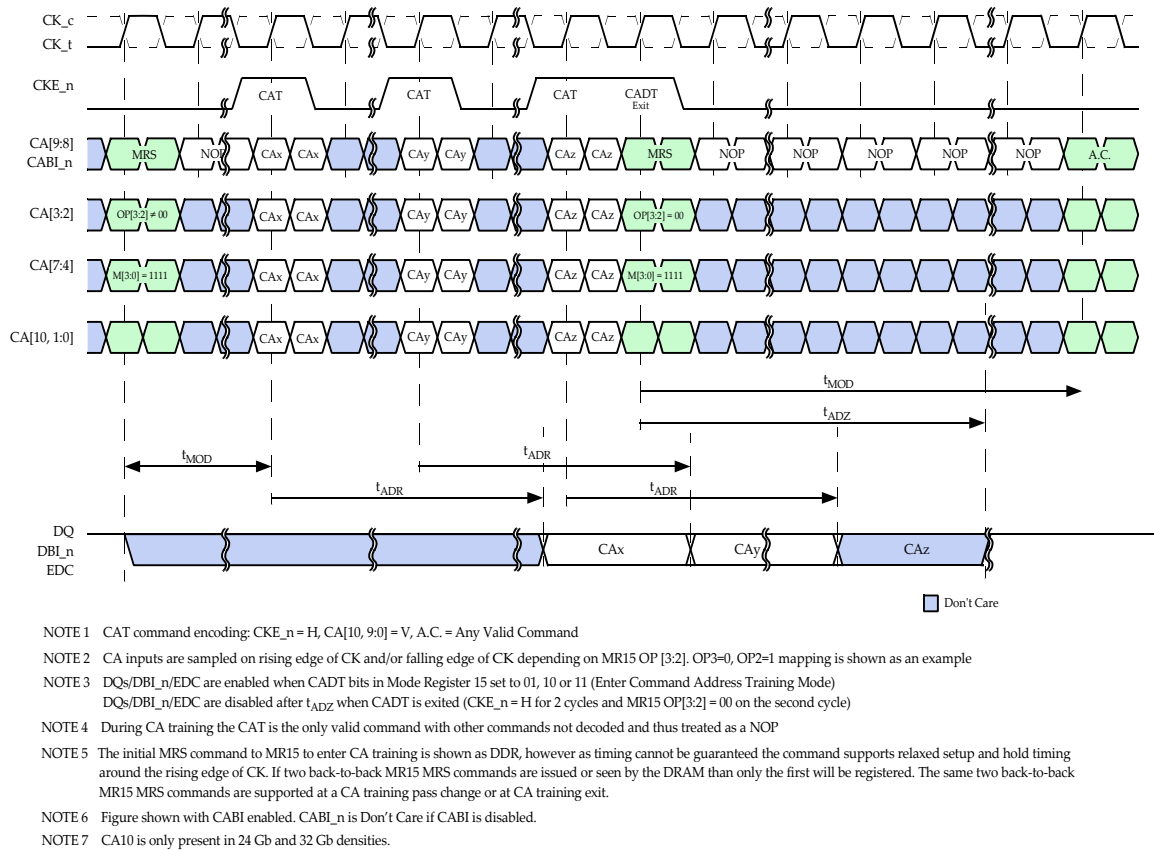


Figure 11 — Command Address Training Timing - Single Pass

Table 22 — AC timings in Command Address Training Mode

Parameter	Symbol	Min	Max	Unit
CAT command to data out delay	t _{ADR}	0	vendor specific	ns
CADD off to DQ/DBI_n in ODT state delay	t _{ADZ}	--	vendor specific	ns

Command Address Training with Self Refresh (CADD Self Refresh)

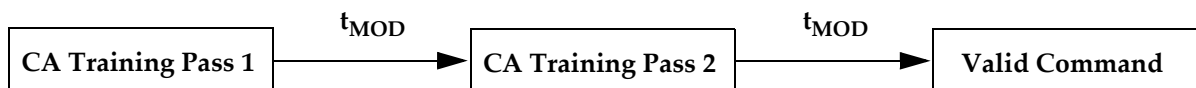
GDDR6 DRAMs support the ability to enable an active Self Refresh mode, here in after CADD Self Refresh mode, to maintain the DRAM contents and enable the required receivers and transmitter that are normally powered down in Self Refresh mode to allow the CA bus to be trained. To enable CADD Self Refresh mode, the CADD SRF register (MR2 OP10) should be set to 1 prior to entering CA training mode with MR15 OP[3:2]. By default CADD Self Refresh will not be enabled when CA training mode is entered. Once the CADD SRF register is set to 1 when MR15 OP[3:2] is set to something other than 00 to enter CA training mode, the DRAM will also enter CADD Self Refresh mode. CA training with Self Refresh does not support Hibernate nor VDDQ off modes and therefore those two Mode Registers are ignored when entering CADD Self Refresh mode.

5.2 COMMAND ADDRESS TRAINING (cont'd)

CA Training in Self Refresh works exactly the same as in normal CA training with the exception of exit from CA Training. When CA training mode is exited with two cycles of $\text{CKE}_n = \text{HIGH}$ and $\text{MR15 OP}[3:2] = 00$ then the device will also exit CADT Self Refresh. After the device has exited CA training with Self Refresh, t_{XS} is required to be met before another valid command as shown in Figure 12.

If multi pass training is planned, the two cycles of $\text{CKE}_n = \text{HIGH}$ and $\text{MR15 OP}[3:2] = 01, 10$ or 11 will leave the DRAM in the CADT Self Refresh state and change the mapping allowing an additional pass after t_{MOD} is met. The current consumption in CADT Self Refresh mode will be higher than in actual Self Refresh mode because the CK clock, CA and data interface is kept in an active state during CA training.

CA Training without Self Refresh (CADT Mode)



CA Training with Self Refresh (CADT Self Refresh Mode)

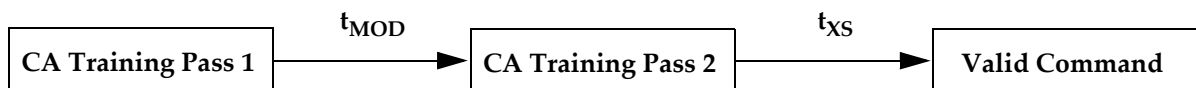
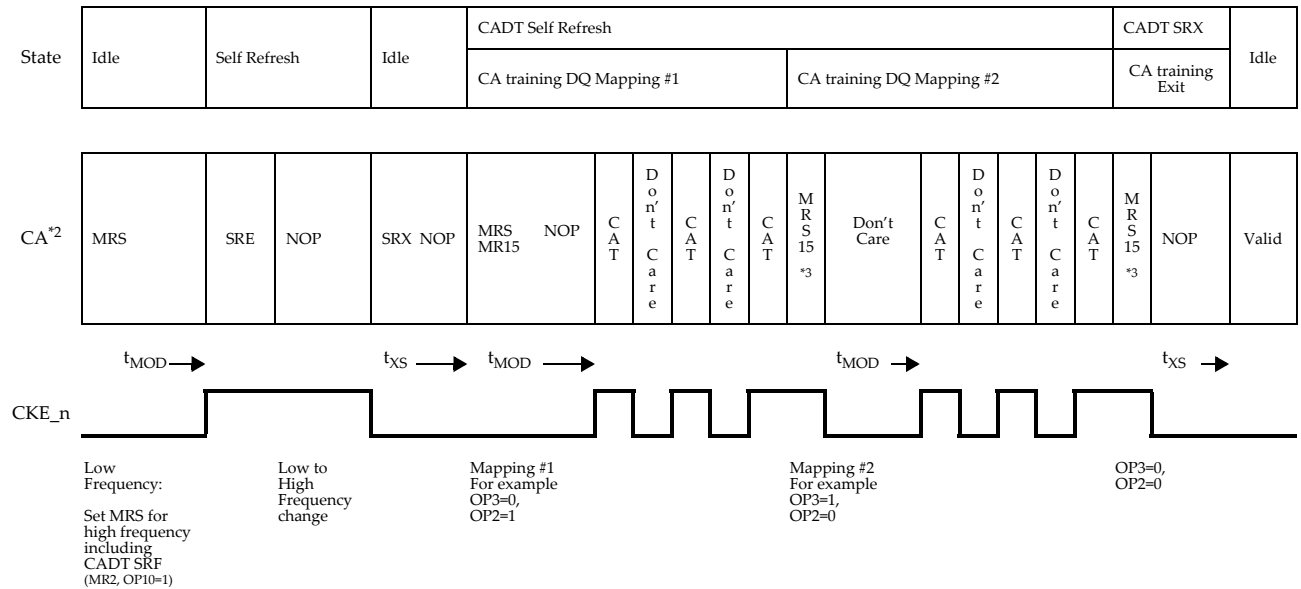


Figure 12 — Multi pass CA Training Timings

An example of one use of CA Training is shown in Figure 13 and Figure 14. The first figure shows an example that sets the CADT SRF register bit in low frequency where CA bus timing is assumed to be met without prior training. The frequency is changed to a higher frequency using Self Refresh and then at the higher frequency two passes of CA training before the exit of CA Training and CADT Self Refresh. The second figure shows the same example CADT sequence without CADT Self Refresh.

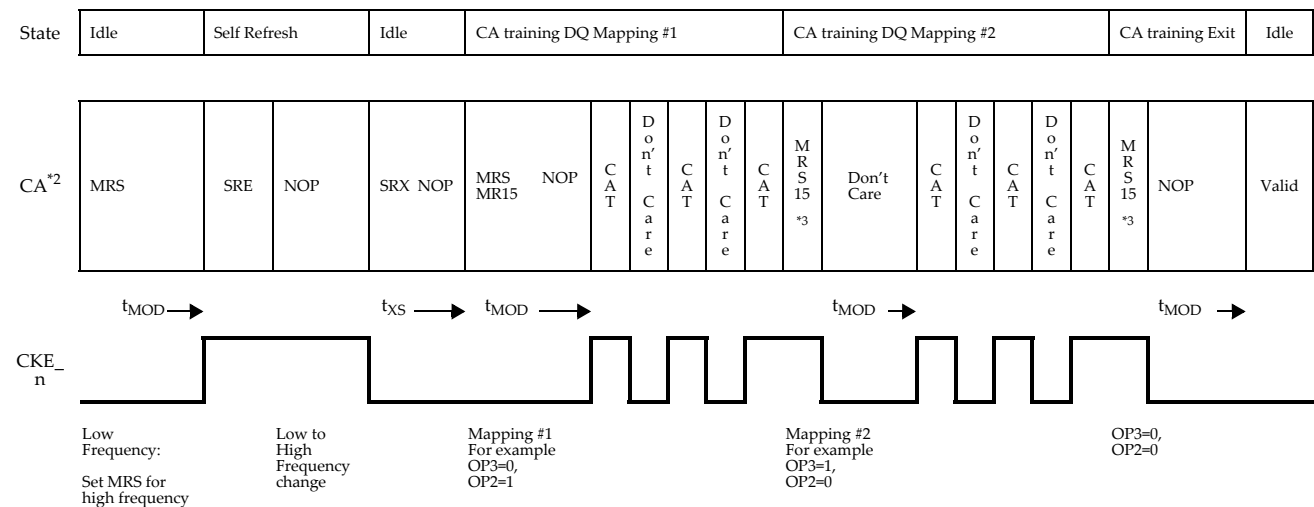
5.2 COMMAND ADDRESS TRAINING (cont'd)



Notes:

- 1) CA training using 2 passes while in Self Refresh is shown as an example.
- 2) See command truth table for detailed encoding of the Commands shown on the CA bus
- 3) The second cycle of CKE_n = H signals the DRAM of a mapping change or CA training exit depending on the value of MR15 OP[3:2]. Two back-to-back MR15 MRS commands are supported at CA training entry, pass change or exit as timing cannot be guaranteed.

Figure 13 — Example of CADT Self Refresh - Multi pass



Notes:

- 1) CA training using 2 passes with a frequency change is shown as an example.
- 2) See command truth table for detailed encoding of the Commands shown on the CA bus
- 3) The second cycle of CKE_n = H signals the DRAM of a mapping change or CA training exit depending on the value of MR15 OP[3:2]. Two back-to-back MR15 MRS commands are supported at CA training entry, pass change or exit as timing cannot be guaranteed.

Figure 14 — Example of CA Training - Multi pass

5.2 COMMAND ADDRESS TRAINING (cont'd)

Table 23 — CA to Data Mapping in CA Training Mode

MR15 OP3 = 0 OP2 = 1										
Output	CA inputs registered at rising edge of CK									
	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
CH A	EDC0	DBI0_n	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
CH B	EDC1	DBI1_n	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8

MR15 OP3 = 1 OP2 = 0										
Output	CA inputs registered at falling edge of CK									
	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
CH A	EDC0	DBI0_n	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
CH B	EDC1	DBI1_n	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8

MR15 OP3 = 1 OP2 = 1			
Output	CA inputs registered at rising edge of CK		
	CABI_n	CA10	
CH A	DQ7	DQ6	
CH B	DQ15	DQ14	
Output	CA inputs registered at falling edge of CK		
	CABI_n	CA10	
CH A	DQ5	DQ4	
CH B	DQ13	DQ12	

5.3 WCK2CK TRAINING

The purpose of WCK2CK training is to align the DATA WCK clock with the COMMAND and ADDRESS (CA) CK clock to aid in the device's internal data synchronization between the logic clocked by CK and WCK. This will help to define both READ and WRITE latencies between the GDDR6 SGRAM and memory controller. WCK2CK training mode is controlled via MRS. The host can read the Vendor ID for info on the WCK characteristics such as WCK Granularity, WCK Frequency and the Internal WCK architecture to ensure the DRAM is configured properly.

Before starting WCK2CK training, the following conditions must be met:

- CK clock is stable and toggling
- The timing of all CA signals must be guaranteed
- PLL on/off (MR1 OP7) and PLL delay compensation enable (MR7 OP2) are set to desired mode
- The desired WCK2CK alignment point (MR7, OP0) and WCK Ratio (MR10 OP9) are selected.
- 2 Mode Register bits for internal WCK Inversion / Quad Shift (MR10, bits OP[7:4]) must be set to a known state
- All banks are idle and no other command execution is in progress

WCK2CK training must be done after any of the following:

- Device initialization
- Any RLmrs (MR0 OP[6:3], MR8 OP8 or MR12 OP3), WLmrs (MR0 OP[2:0]), CRCRL (MR4 OP[8:7]) or CRCWL (MR4 OP[6:4] or MR12 OP4) latency change
- CK and WCK frequency changes
- PLL on/off (MR1 OP7) and PLL delay compensation mode (MR7 OP2) changes
- Change of the WCK2CK alignment point (MR7 OP0) or WCK Ratio (MR10 OP9)
- Self Refresh exit or exit from Power-Down when LP2 (OP1 in MR5) is set

Figure 15 and Figure 16 show example WCK2CK training sequences. WCK2CK training is entered via MRS by setting OP8 in MR10. This will initiate the WCK divider circuits associated with WCK0 and WCK1 clocks in the case of WCK/byte or WCK0 in the case of WCK/word. In case the divider circuits on each byte of the channel are not in phase, which is indicated by opposite or multiple U.I. Offset "early/late" phases on the EDC signals, they may be put into phase by using the WCK INV/Quad shift MR bits to either invert the internal WCK (2UI shift if using internal quarter-rate WCK, 4UI shift if using internal eighth-rate WCK) or Quad shift the internal WCK (2UI shift if using internal eighth-rate WCK, not valid with internal quarter-rate WCK). Alternatively, the WCK clocks may be put into a stable inactive state for this initialization event to aid in resetting all dividers to the same output phase as shown in Figure 16. The host is required to restart the WCK clocks in a way that all clock edges meet the WCK clock input specification. Otherwise, the WCK divider circuits for both WCK0 (and WCK1 if WCK/byte) might again have opposite alignment (Internal Quarter data rate) or out of phase alignment (internal eighth data rate). The use of this WCK2CK training method is restricted to operating frequencies up to $f_{WCKSTOP}$. Figure 18 illustrates the difference between a device that uses an internal quarter data rate and a device that uses a internal eighth data rate for the internal WCK divider circuit.

Figure 17 illustrate how the WCK phase information is derived. The phase detectors (PD) sample the internally divided WCK clocks. Only one sample point is shown in the figure for clarity. In reality, when WCK2CK training mode is enabled, a sample will occur every t_{CK} and will be translated to the EDC signals accordingly. If the divided WCK clock arrives early, then the EDC pin outputs a HIGH during the time interval specified in Figure 17. If the divided WCK clock arrives late, then the EDC pin outputs a LOW during the time interval specified in Figure 17. This is shown in Table 24. Finally, if the divided WCK and CK clocks are perfectly aligned at the PD, the EDC signals are indeterminate. For a GDDR6 device with WCK / word the phase information is returned on both EDC0 and EDC1 in x16 mode and on the enabled byte in x8 mode.

5.3 WCK2CK TRAINING (cont'd)

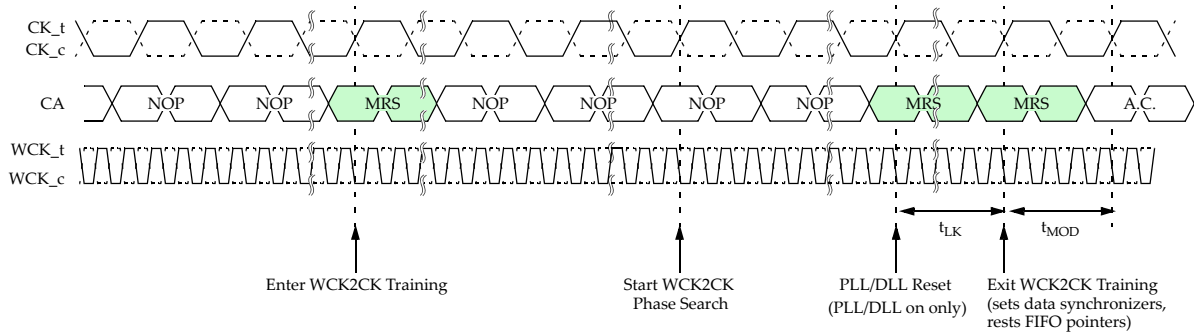


Figure 15 — Example WCK2CK Training Sequence

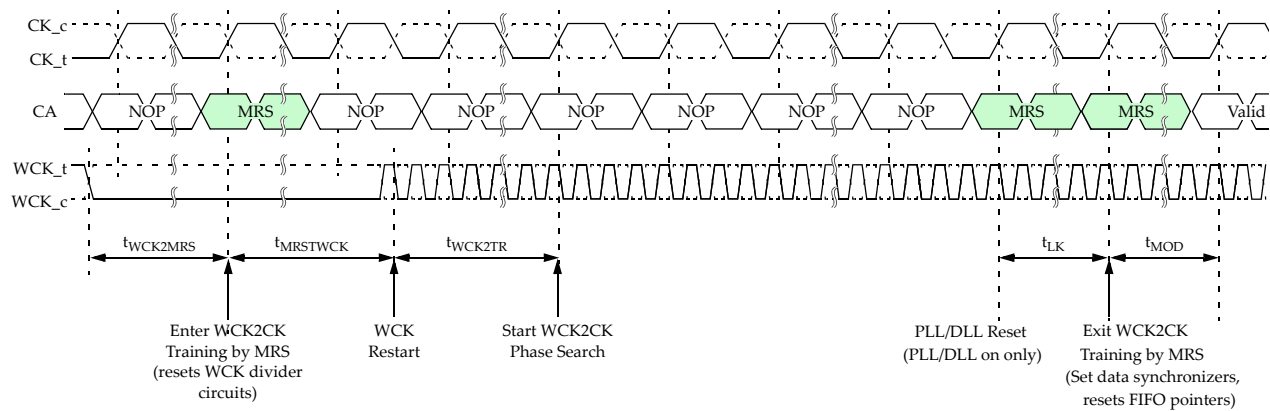
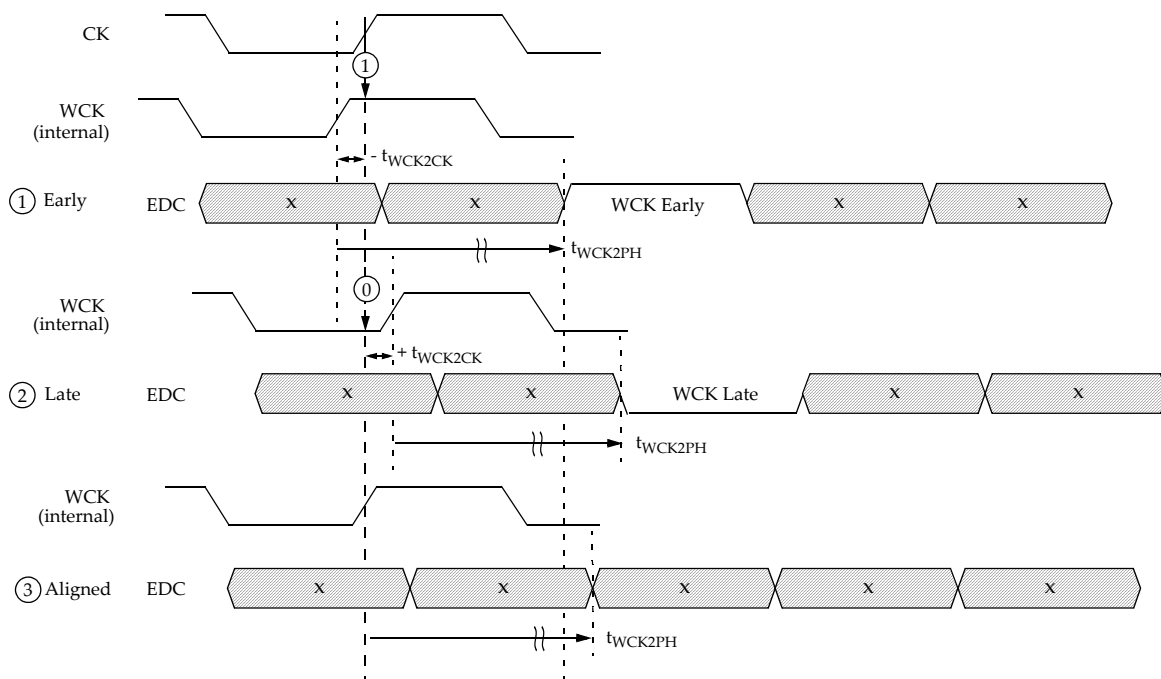


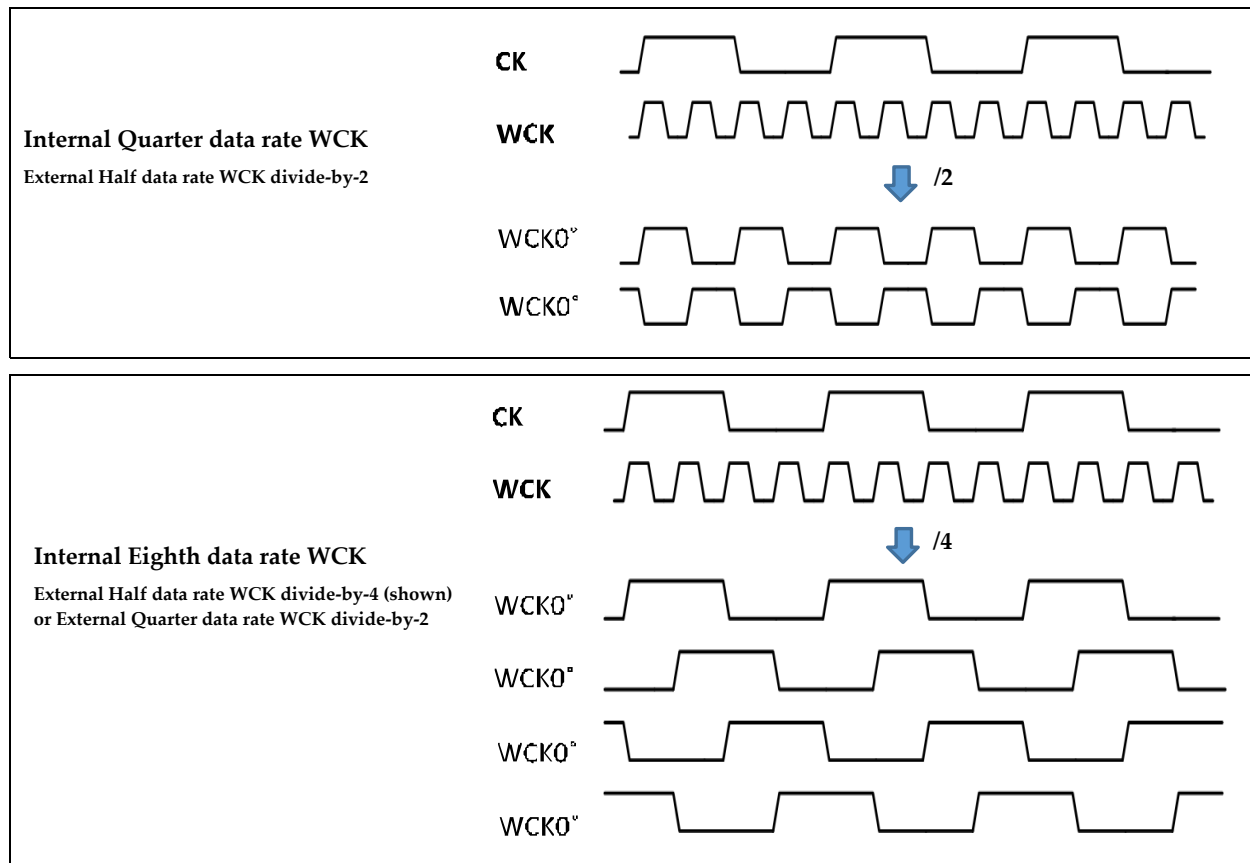
Figure 16 — Example WCK2CK Training Sequence with WCK Stopping



Note Example shows an internal eighth data rate WCK.

Figure 17 — EDC pin Behavior for WCK2CK Training with Internal WCK

5.3 WCK2CK TRAINING (cont'd)



Note 1 External Quarter data rate WCK divide-by-4 is not a valid architecture for a WCK Divider.
Note 2 WCK0° represents the possible positions of the internal divided WCK clock.

Figure 18 — Internal WCK Divider Circuit

Table 24 — Phase Detector and EDC behavior

Internal Quarter data rate or Internal Eighth data rate value sampled by CK	WCK2CK Phase	Data on EDC	Action
'HIGH'	'Early'	HIGH	Increase Delay on WCK
'LOW'	'Late'	LOW	Decrease Delay on WCK

The ideal alignment is indicated by the phase detector output transitioning from “early” to “late” when the delay of the WCK phase is continuously increased. The WCK phase range for ideal alignment is specified by the parameter $t_{WCK2CKPIN}$ in the vendor’s datasheet; the value(s) vary with the PLL/DLL mode (on or off) and the selected alignment point.

If enabled, the PLL/DLL shall not interfere in the behavior of the WCK2CK training. Significantly moving the phase and/or stopping the WCK during training may disturb the PLL/DLL. It is required to perform a PLL/DLL reset after the WCK2CK training has determined and selected the proper alignment between WCK and CK clocks. The PLL/DLL lock time t_{LK} must be met before exiting WCK2CK training to guarantee that the PLL/DLL is in lock such that the data synchronizers are set upon WCK2CK training exit.

5.3 WCK2CK TRAINING (cont'd)

WCK2CK training is exited via MRS by resetting OP8 in MR10. If the WCK Inversion / Quad Shift bits in MR10 OP[7:4] have been programmed during WCK2CK training, this MRS command to exit WCK2CK training must be a subsequent and additional MRS command, and the WCK Inversion / Quad Shift bits must be kept the same as programmed before with the MRS command.

For proper reset of the data synchronizers it is required that the WCK and CK clocks are aligned within $t_{WCK2CKSYNC}$ at the time of the WCK2CK training exit.

After exiting WCK2CK training mode, the WCK phase is allowed to further drift from the ideal alignment point by a maximum of t_{WCK2CK} (e.g., due to voltage and temperature variation). Once this WCK phase drift exceeds $t_{WCK2CK(min)}$ or $t_{WCK2CK(max)}$, it is required to repeat the WCK2CK training and realign the clocks. The values of t_{WCK2CK} and $t_{WCK2CKSYNC}$ may vary with the WCK ratio as defined in the AC timing table.

WCK2CK alignment at PIN Mode (optional)

The WCK and CK phase alignment point can be changed via MRS by setting OP0 in MR7. In normal mode, when MR7 OP0 is set to '0', the phases of CK and WCK are aligned at the phase detector. On the other hand, when MR7 OP0 is set to '1', the phases of CK and WCK are aligned at the balls as shown in Figure 20. PIN mode is supported up to the max CK clock frequency of f_{CKPIN} , and is an option to reduce the time of WCK2CK training at low frequency.

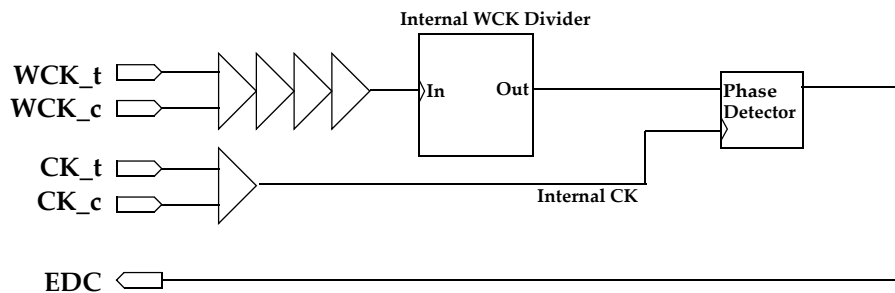


Figure 19 – Normal Mode

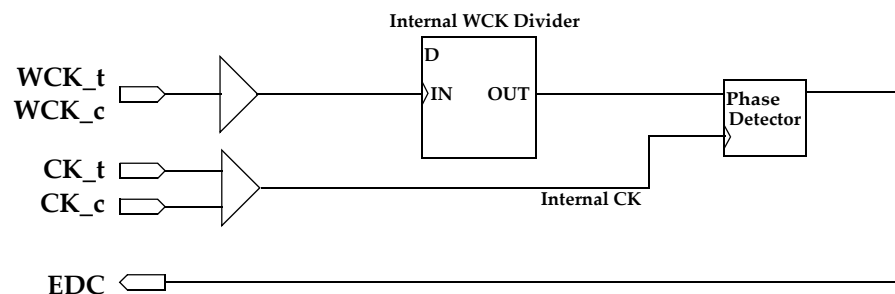


Figure 20 – Pin Mode (optional)

5.3 WCK2CK TRAINING (cont'd)

WCK2CK Auto Synchronization

When WCK2CK automatic synchronization mode is enabled using MR7 OP4, WCK2CK training can be limited to meeting the $t_{WCK2CKSYNC}$ specification and issuing two WCK2CK MRS for WCK 2CK training entry and exit. The PLL/DLL sequence is not affected by this mode. The use of WCK2CK automatic synchronization mode is restricted to operating frequencies up to $f_{CKAUTOSYNC}$ as described in vendor's datasheets and works for both normal and PIN mode.

Table 25 describes WCK2CK training methods for different frequency ranges. Each Frequency range is vendor specific. Normal and PIN mode of WCK2CK training are described in Table 25. Each frequency range is DRAM vendor specific. Divider initialization can be done by training with WCK2CK inversion, WCK2CK stopping, or WCK2CK auto-sync. If the user wants to use WCK2CK stop for divider initialization instead of WCK2CK auto-sync, the user must not set the WCK2CK auto-sync. Below middle frequency, the combined use of PIN and WCK2CK auto-sync modes can minimize WCK2CK training time.

Table 25 — An example of WCK2CK training simplified for Normal mode and PIN mode

	High Frequency (i.e., 12 Gbps)		Middle Frequency (i.e., 4 Gbps)		Low Frequency (i.e., 800 Mbps)	
Frequency (Vendor Specific)						
WCK2CK alignment mode	Normal	PIN	Normal	PIN	Normal	PIN
Phase Search	Required	Required	Required	No*	No*	No*

* NOTE The divided WCK_t/WCK_c should be aligned CK_t/CK_c by WCK2CK Auto Synchronization or WCK stop mode

The following examples describe the WCK2CK training in more detail.

Example 1: outline of a basic WCK2CK training sequence without WCK clock stop:

- 1) Enable training mode via MRS and wait t_{MOD}
- 2) Sweep and observe the phase independently for WCK0 on EDC0 and WCK1 on EDC1; in case the internal divider circuits are at opposite phase use either the WCK inversion / quad shift bits to flip/ shift one of the WCK divider circuits
- 3) Adjust the WCK phase independently for WCK0 and WCK1 or WCK0 for WCK/word to the optimal point ("ideal alignment")
- 4) Issue a PLL/DLL reset and wait for t_{LK} (PLL/DLL on mode only)
- 5) While all WCK and CK are aligned, exit WCK2CK training mode via MRS
- 6) Wait t_{MOD} for the reset of data synchronizers

Example 2: outline of a basic WCK2CK training sequence with WCK clock stop:

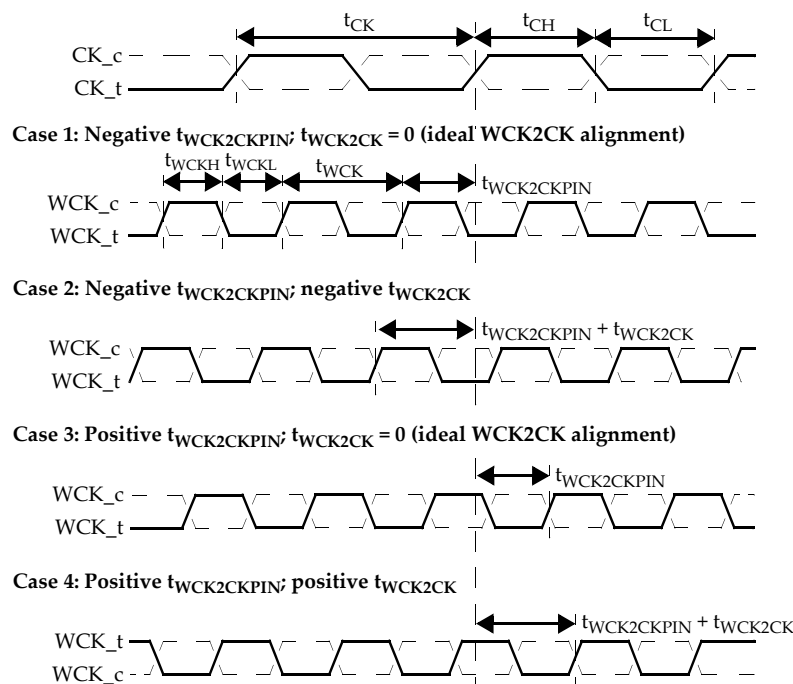
- 1) Stop WCK clocks with WCK0_t/WCK1_t LOW and WCK0_c/WCK1_c HIGH
- 2) Wait $t_{WCK2MRS}$ for internal WCK clocks to settle
- 3) Enable training mode via MRS and wait $t_{MRSTWCK}$ for divider circuits to reset
- 4) Start WCK clocks without glitches (divider circuits remain in sync)
- 5) Wait t_{WCK2TR} for internal WCK clocks to stabilize
- 6) Sweep and observe the phase independently for WCK0 on EDC0 and WCK1 on EDC1 or WCK0 for WCK/word; adjust the WCK phase to the optimal point ("ideal alignment")
- 7) Issue a PLL/DLL reset and wait t_{LK} (PLL/DLL on mode only)
- 8) While all WCK and CK are aligned, exit WCK2CK training mode via MRS
- 9) Wait t_{MOD} for the reset of data synchronizers

5.3 WCK2CK TRAINING (cont'd)

Example 3: WCK2CK training sequence for configurations with 2 devices sharing their WCK clocks:

- 1) Enable training mode for both DRAMs via MRS and wait t_{MOD}
- 2) For both DRAMs sweep and observe the phase independently for WCK0 on EDC0 and WCK1 on EDC1; in case the internal divider circuits are at opposite phases use either the WCK inversion / quad shift bits to flip/shift one of the WCK divider circuits; use MREA and MREB bits in MR15 (soft chip select) to explicitly direct the MRS command for this operation to one of the two devices.
- 3) Sweep and observe the phase on the first device; store the setting for the optimal WCK phase.
- 4) Sweep and observe the phase on the second device; store the setting for the optimal WCK phase.
- 5) Sweep WCK phase to the midpoint of both device's optimal settings
- 6) Issue a PLL/DLL reset and wait for t_{LK} (PLL/DLL on mode only)
- 7) While all WCK and CK are aligned, exit WCK2CK training mode via MRS
- 8) Wait t_{MOD} for the reset of data synchronizers

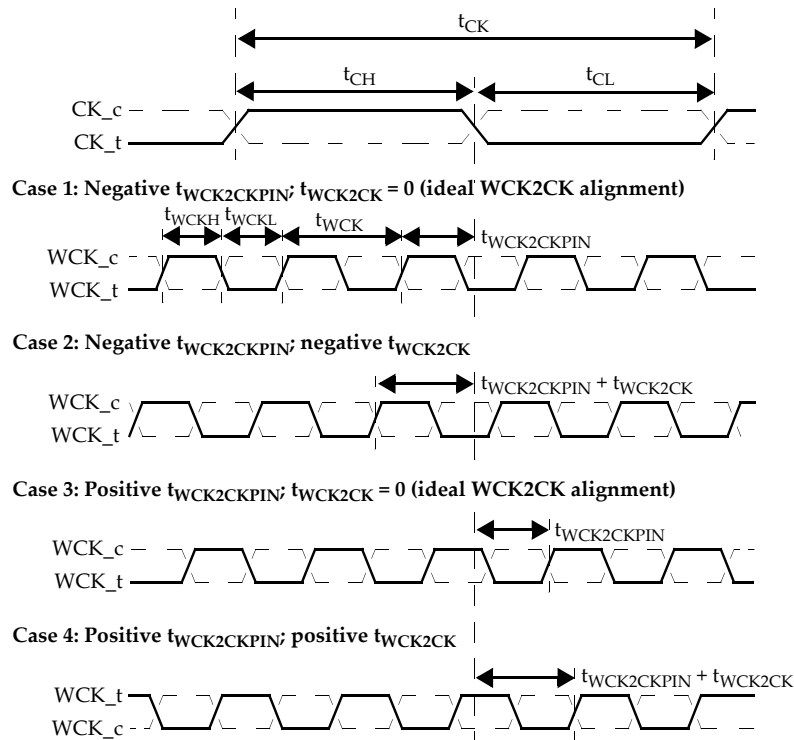
READ and WRITE latency timings are defined relative to CK. Any offset in WCK and CK at the balls and/or the phase detector will be reflected in the latency timings. The parameters used to define the relationship between WCK and CK are shown in Figure 21. For more details on the impact on READ and WRITE timings see the OPERATIONS section.



Note: $t_{WCK2CKPIN}$ and t_{WCK2CK} parameter values could be negative or positive numbers, depending on the selected WCK2CK alignment point, PLL-on-or PLL-off mode operation and design implementation. They also vary across PVT. WCK2CK training is required to determine the correct WCK-to-CK phase for stable device operation.

Figure 21 — WCK2CK Timings for WCK QDR Ratio

5.3 WCK2CK TRAINING (cont'd)



Note: $t_{WCK2CKPIN}$ and t_{WCK2CK} parameter values could be negative or positive numbers, depending on the selected WCK2CK alignment point, PLL-on-or PLL-off mode operation and design implementation. They also vary across PVT. WCK2CK training is required to determine the correct WCK-to-CK phase for stable device operation.

Figure 22 — WCK2CK Timings for WCK DDR Ratio

5.4 READ TRAINING

Read training allows the memory controller to find the data-eye optimal position (symbol training) and burst frame location (frame training) for each high-speed output of the device. Each pin (DQ[15:0], DBI[1:0]_n, EDC[1:0]) can be individually trained during this sequence.

For Read Training the following conditions must be true:

- at least one bank is active, or a REFab must be in progress and OP2 in Mode Register 5 (MR5) is set to 0 to allow training during a REFab (to disable this special refresh enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- WCK2CK training must be complete
- the PLL/DLL must be locked, if enabled
- RDBI and WDBI must be enabled prior to and during Read Training if the training shall include DBI_n. RDCRC and WRCRC must be enabled prior to and during Read Training if the training shall include the EDC signals.

The following commands are associated with Read Training:

- LDFF to preload the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither LDFF nor RDTR access the memory core. No MRS is required to enter Read Training.

Figure 23 shows an example of the internal data paths used with LDFF and RDTR. Table 26 lists AC timing parameters associated with Read Training.

Table 26 — LDFF and RDTR TIMINGS

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
ACTIVATE to LDFF command delay	t_{RCDLTR}		–	ns	
ACTIVATE to RDTR command delay	t_{RCDRTR}		–	ns	
REFab to RDTR or WRTR command delay	t_{REFTR}		–	ns	
RDTR to RDTR command delay	t_{CCDS}		–	t_{CK}	1
LDFF to LDFF command cycle time	t_{LTLTR}	4	–	t_{CK}	
LDFF15 to RDTR command delay	t_{LTRTR}		–	t_{CK}	
READ or RDTR to LDFF command delay	t_{RDILT}		–	t_{CK}	
Note 1: Use t_{CCDS} for gapless consecutive RDTR commands regardless whether Bank Groups is enabled or not.					

5.4 READ TRAINING (cont'd)

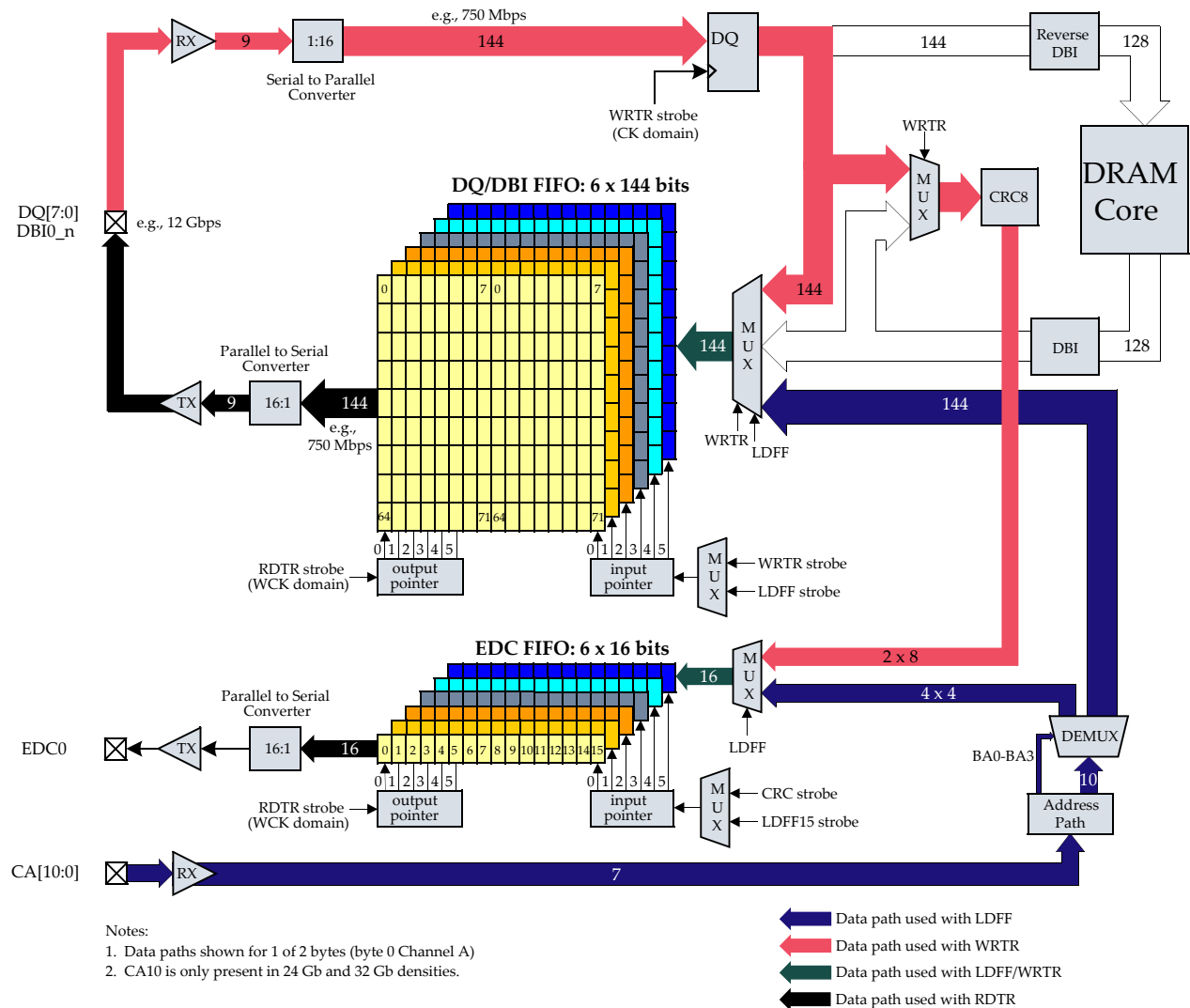


Figure 23 — Data Paths used for Read and Write Training

LDF Command

The LDF command (Figure 24) is used to securely load data to the device's Read FIFOs via the CA bus. The READ FIFO has a fixed depth of 6 bursts and thus can store a $6 \times 16 = 96$ U.I. long bit pattern uniquely to every DQ, DBI_n and EDC pin within a byte.

Sixteen LDF commands are required to fill one FIFO stage; each LDF command loads one burst position, and B[3:0] conveyed on CA[7:4] select the burst position from 0 to 15.

The data pattern D[9:0] for DQ[7:0], DBI0_n, and EDC0 is conveyed on CA[5:0]; the data are internally replicated to both bytes in a channel, as shown in Figure 25.

LDF loads the DBI FIFO when WDBI and RDBI are enabled in the Mode Register. It also loads the EDC FIFO regardless of the WRCRC and RDCRC Mode Register bits, and no CRC is calculated; however, RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command.

If the EDC Mode is set to Half data rate in MR2 OP8, the pattern for the EDC pin provided with the LDF command must be the same for the even and next odd burst position (e.g. burst positions 0-1, 2-3, ... , 14-15). If retrieved from the EDC FIFO using the RDTR command, such a pattern will appear as a half data rate.

5.4 READ TRAINING (cont'd)

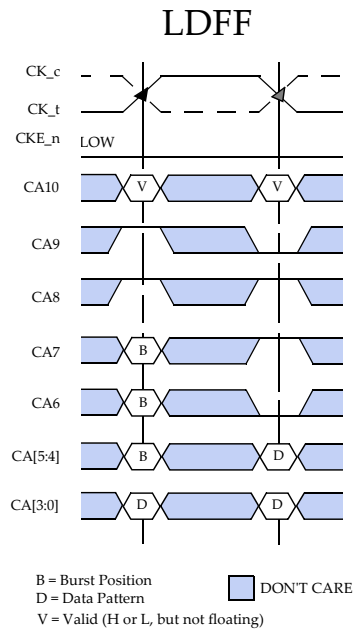


Figure 24 – LDFF Command

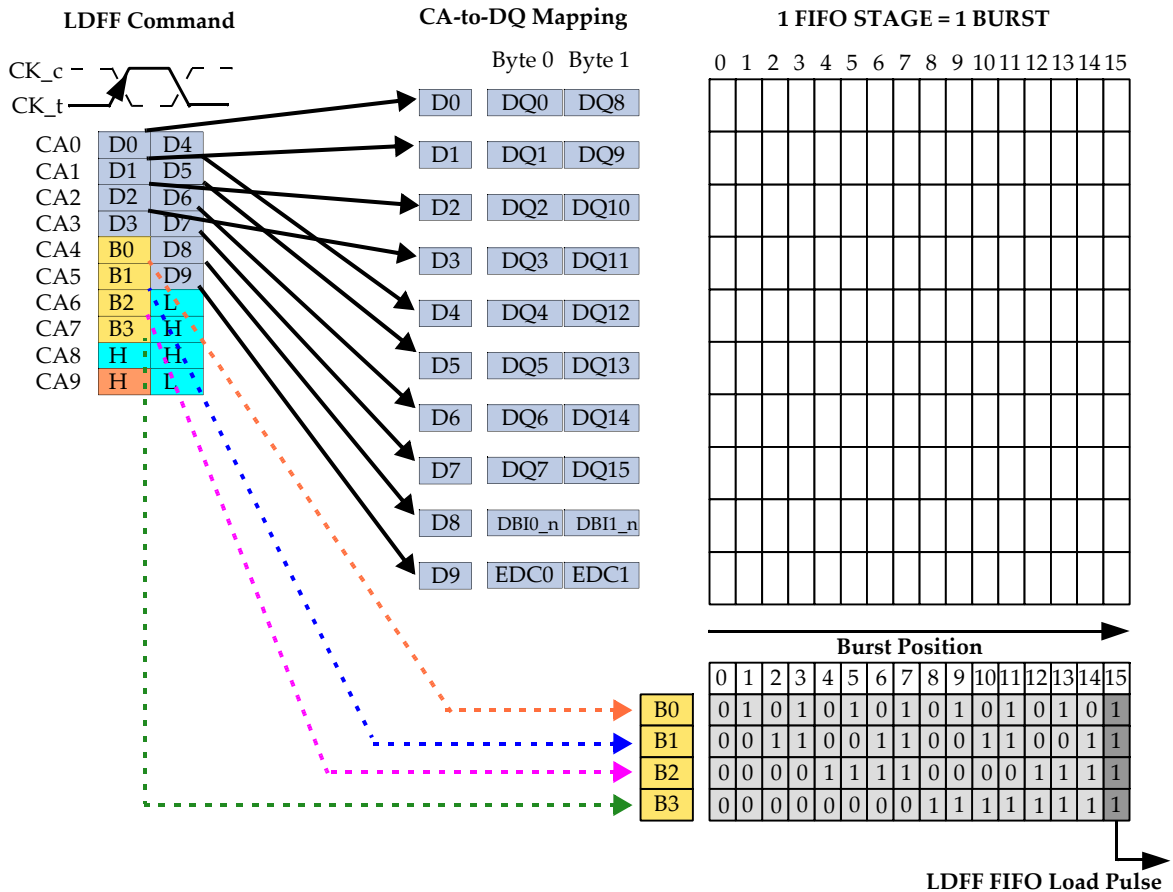


Figure 25 – LDFF Command Address to DQ/DBI_n/EDC Mapping

5.4 READ TRAINING (cont'd)

All bursts (0 to 15) must be loaded; LDFF commands to burst 0 to 14 may be issued in random order; the LDFF command to burst 15 (LDFF15) must be the last of 16 consecutive LDFF commands, as it effectively loads the data into the FIFO and results in a FIFO pointer increment. Consecutive LDFF commands have to be spaced by at least t_{LTLTR} .

LDFP pattern may efficiently be replicated to the next FIFO stages by issuing consecutive LDFP commands to burst 15 (with identical data pattern). The data pattern in the scratch memory for LDFP will be available until the first RDTR command.

The DQ/DBI_n output buffers remain in ODT state during LDFF.

An amount of LDFF commands to burst 15 greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data input.

The total number of LDFF commands to burst 15 modulo FIFO depth must equal the total number of RDTR commands modulo FIFO depth when used in conjunction with RDTR. No READ or WRITE commands are allowed between LDFF and RDTR.

The EDC hold pattern is driven on the EDC signals during LDFF.

RDTR Command

A RDTR burst is initiated with a RDTR command as shown in Figure 26. No bank or column addresses are used as the data is read from the internal READ FIFO, not the array. The length of the burst initiated with a RDTR command is sixteen. There is no interruption nor truncation of RDTR bursts. The FIFO access is suppressed when CE bit is LOW, and the DQ, DBI and EDC will behave as if no RDTR is occurring. In two channel mode CE shall be driven HIGH.

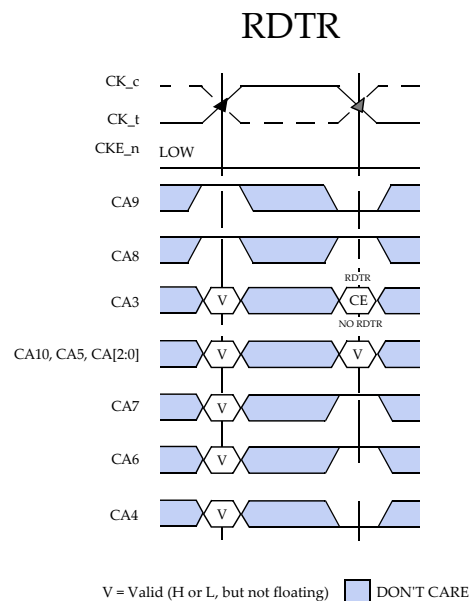


Figure 26 — RDTR Command

5.4 READ TRAINING (cont'd)

A RDTR command may only be issued when a bank is open or a refresh is in progress and bit OP2 in MR5 is set to 0 to allow training during REFab.

RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command. If not set, DBI_n will remain in ODT state, and the EDC signals will drive the EDC hold pattern.

An amount of RDTR commands greater than the FIFO depth (= 6) is allowed and shall result in a looping of the FIFO's data output.

During RDTR bursts, the first valid data-out element will be available after the Read latency (RL). The latency is the same as for READ. The data on the EDC signals comes with additional CRC latency (t_{CRCRD}) after the RL.

Upon completion of a burst, assuming no other RDTR command has been initiated, all DQs and DBI_n will drive a value of '1' and the ODT will be enabled at a maximum of 1 t_{CK} later. The drive value and termination value may be different due to separately defined calibration offsets. If the ODT is disabled, the signals will drive Hi-Z.

Data from any RDTR burst may be concatenated with data from a subsequent RDTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new RDTR command should be issued after the first RDTR command according to the t_{CCDS} timing.

A WRTR can be issued any time after a RDTR command as long as the bus turn around time t_{RTW} is met.

The total number of RDTR commands modulo FIFO depth must be equal to total number of WRTR commands modulo FIFO depth when used in conjunction with WRTR. No READ or WRITE commands are allowed between WRTR and RDTR.

The total number of RDTR commands modulo FIFO depth must be equal to the total number of LDFF commands to burst position 15 modulo FIFO depth when used in conjunction with LDFF. No READ or WRITE commands are allowed between LDFF and RDTR.

5.5 WRITE TRAINING

Write training allows the memory controller to find the data-eye optimal position (symbol training) and burst frame location (frame training) for each high-speed input of the device. Each signal pin (DQ[15:0] and DBI[1:0]_n) can be individually trained during this sequence.

For Write Training the following conditions must be true:

- at least one bank is active, or a REFab must be in progress and bit OP2 in Mode Register 5 (MR5) is set to 0 to allow training during a REFab (to disable this special REF enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- the PLL/DLL must be locked, if enabled.
- WCK2CK training should be complete
- Read training should be complete
- RDBI and WDBI must be enabled prior to and during Write Training if the training shall include DBI_n. RDCRC and WRCRC must be enabled prior to and during Write Training if the training shall include the EDC signals.

The following commands are associated with Write Training:

- WRTR to write a burst of data directly into the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither WRTR nor RDTR access the memory core. No MRS is required to enter Write Training.

Figure 23 shows an example of the internal data paths used with WRTR and RDTR. Figure 28 shows a typical Write training command sequence using WRTR and RDTR. Table 27 lists AC timing parameters associated with WRITE Training.

Table 27 — WRTR and RDTR Timings

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
ACTIVATE to WRTR command delay	t_{RCDWTR}		–	ns	
ACTIVATE to RDTR command delay	t_{RCDRTR}		–	ns	
REFab to RDTR or WRTR command delay	t_{REFTR}		–	ns	
RD/WR bank A to RD/WR bank B command delay different bank groups	t_{CCDS}		–	t_{CK}	1
WRTR to RDTR command delay	t_{WTRTR}		–	t_{CK}	
WRITE to WRTR command delay	t_{WRWTR}		–	t_{CK}	
READ or RDTR to WRITE or WRTR command delay	t_{RTW}		–	ns	2
Note 1: Use t_{CCDS} for gapless consecutive WRTR and RDTR commands regardless whether Bank Groups is enabled or not. Note 2: t_{RTW} is not a device limit but determined by the system bus turnaround time. The difference between t_{WCK2DQO} and t_{WCK2DQI} shall be considered in the calculation of the bus turnaround time.					

5.5 WRITE TRAINING (cont'd)

WRTR Command

A WRTR burst is initiated with a WRTR command as shown in Figure 27. No bank or column addresses are used as the data is written to the internal READ FIFO, not the array. The length of the burst initiated with a WRTR command is sixteen. There is no interruption nor truncation of WRTR bursts. The FIFO access is suppressed when CE bit is LOW, and the DQ, DBI and EDC will behave as if no WRTR is occurring. In two channel mode CE shall be driven HIGH.

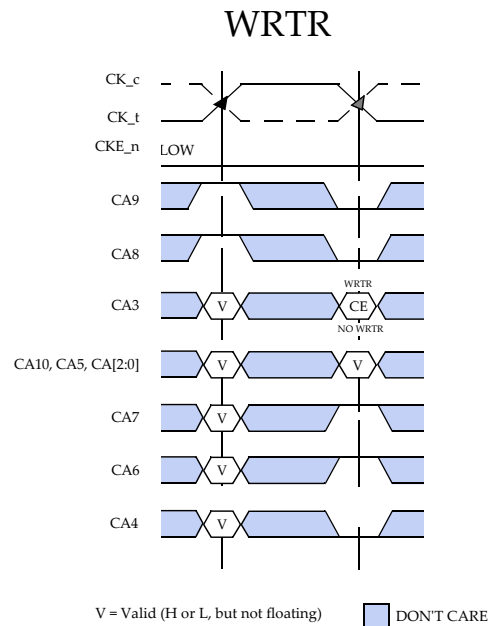


Figure 27 — WRTR Command

A WRTR command may only be issued when a bank is open or a refresh is in progress and OP2 in MR5 is set to 0 to allow training during REFab.

WDBI and WRCRC must be enabled to write the DBI and EDC bits, respectively, with the WRTR command. If WDBI is not set, a '1' will be written to the DBI FIFO, and a '1' will be assumed for the DBI_n input in the CRC calculation. In contrast to a normal WRITE, no CRC is returned by the WRTR command and the EDC signals will drive the EDC hold pattern.

Please note that RDCRC must be enabled to read the calculated CRC data with the RDTR command.

An amount of WRTR commands equal to the FIFO depth (= six) is required to fully load the FIFO; any number of WRTR commands greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data input.

During WRTR bursts, the first valid data-in element must be available at the input latch after the Write Latency (WL). The Write Latency is the same as for WRITE.

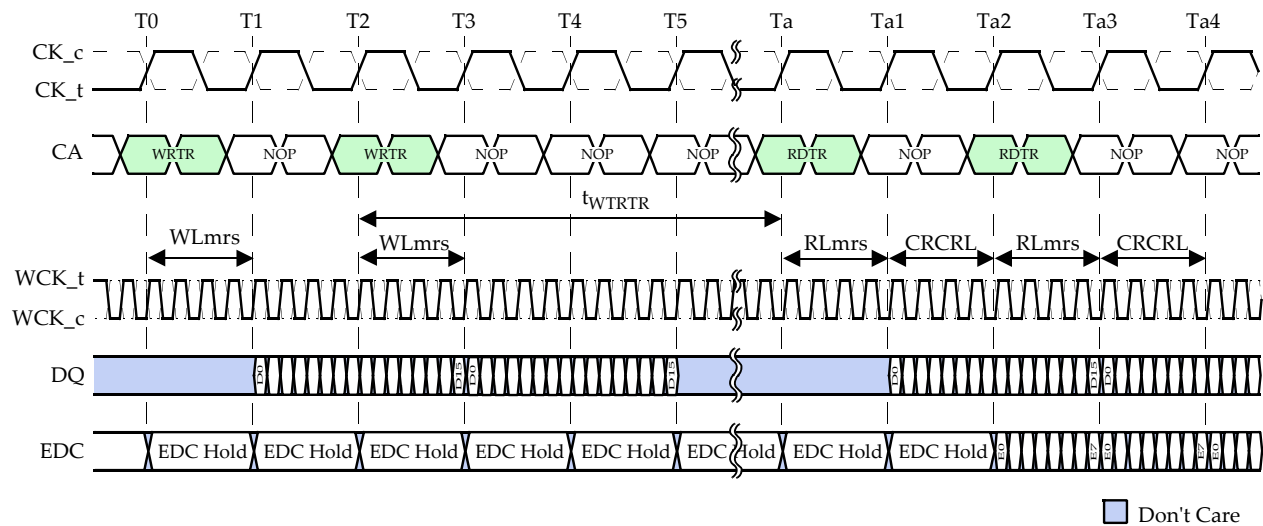
Upon completion of a burst, assuming no other WRTR data is expected on the bus the DQs and DBI_n will be driven according to the ODT state. Any additional input data will be ignored.

5.5 WRITE TRAINING (cont'd)

Data from any WRTR burst may be concatenated with data from a subsequent WRTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new WRTR command should be issued after the previous WRTR command according to the t_{CCDS} timing.

A RDTR can be issued any time after a WRTR command as long as the internal bus turn around time t_{WRTR} is met.

The total number of WRTR commands modulo FIFO depth must equal the total number of RDTR commands modulo FIFO depth when used in conjunction with RDTR. No READ or WRITE commands are allowed between WRTR and RDTR.



1. WLmrs, RLmrs and CRCRL = 1 for ease of illustration; check Mode Register definition for supported settings
2. WCK and CK are shown aligned ($t_{WCK2CKPIN}=0$, $t_{WCK2CK}=0$) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

Figure 28 — Write Training using WRTR and RDTR Commands

6 MODE REGISTERS

GDDR6 specifies 14 Mode Registers to define the specific mode of operation. MR0 to MR12 and MR15 are defined as shown in the overview in Figure 29. MR13 and MR14 are not defined and reserved for vendor specific features. Reprogramming the Mode Registers will not alter the contents of the memory array.

All Mode Registers are programmed via the MODE REGISTER SET (MRS) command and will retain the stored information until they are reprogrammed, chip reset, or the device loses power. Mode Registers must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MOD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

No default states are defined for Mode Registers except when otherwise noted. Users therefore must fully initialize all Mode Registers to the desired values upon power-up or after a subsequent chip reset.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0.

If the user activates bits in an optional field, either the optional field is activated (if option is implemented in the device) or no action is taken by the device (if option is not implemented).

6 MODE REGISTERS (cont'd)

	M3	M2	M1	M0	OP11	OP10	OP9	OP8	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	0	0	0	0	Write Recovery (WR)				TM	Read Latency (RLmrs)				Write Latency (WLmrs)		
MR1	0	0	0	1	PLL Reset	CABI	WDBI	RDBI	PLL DLL	Cal Upd	PLL/DLL Range	Data Termination		Driver Strength		
MR2	0	0	1	0	EDC HR	CADT SRF	RDQS	EDC mode	Self Refresh		OCD Pullup Driver Offset		OCD Pulldown Driver Offset			
MR3	0	0	1	1	Bank Groups		WR Scaling		Info		CA Termination Offset		DQ and WCK Termination Offset			
MR4	0	1	0	0	EDC Inv	WR CRC	RD CRC	CRC Read Latency (CRCRL)		CRC Write Latency (CRCWL)		EDC Hold Pattern				
MR5	0	1	0	1	RAS						PLL/DLL Bandwidth (PLLBW)		LP3	LP2	LP1	
MR6	0	1	1	0	Pin Sub-Address					VREFD Level						
MR7	0	1	1	1	DCC		VDD Range		Half VREFD	HALF VREFC	DQ PreA	Auto Sync	LF Mode	PLL DelC	Hiber-nate	WCK AP
MR8	1	0	0	0	CK Termination		WR EHF	RL EHF	REFpb	CK AC	EDC Hi-Z	CA TO	CAH Termination		CAL Termination	
MR9	1	0	0	1	Pin Sub-Address					RFU			Decision Feedback Equalization (DFE)			
MR10	1	0	1	0	WCK Termination		WCK Ratio	WCK2 CK	WCK Inv / QS Byte 1		WCK Inv / QS Byte 0		VREFC Offsets			
MR11	1	0	1	1	PASR Row Segment Mask					PASR 2-Bank Mask						
MR12	1	1	0	0	RFU						WR EHF2	CRCWL EHF	RL EHF2	PRBS	P2BR Addr	VDDQ OFF
MR13	1	1	0	1	Reserved for Vendor Specific Features											
MR14	1	1	1	0	Reserved for Vendor Specific Features											
MR15	1	1	1	1									CADT		MRE	

Figure 29 — Mode Registers Overview

6.1 MODE REGISTER 0 (MR0)

Mode Register 0 controls operating modes such as Write Latency, Read Latency, Write Recovery and Test Mode as shown in Figure 30. The register is programmed via the MODE REGISTER SET (MRS) command with M[3:0] = 0000.

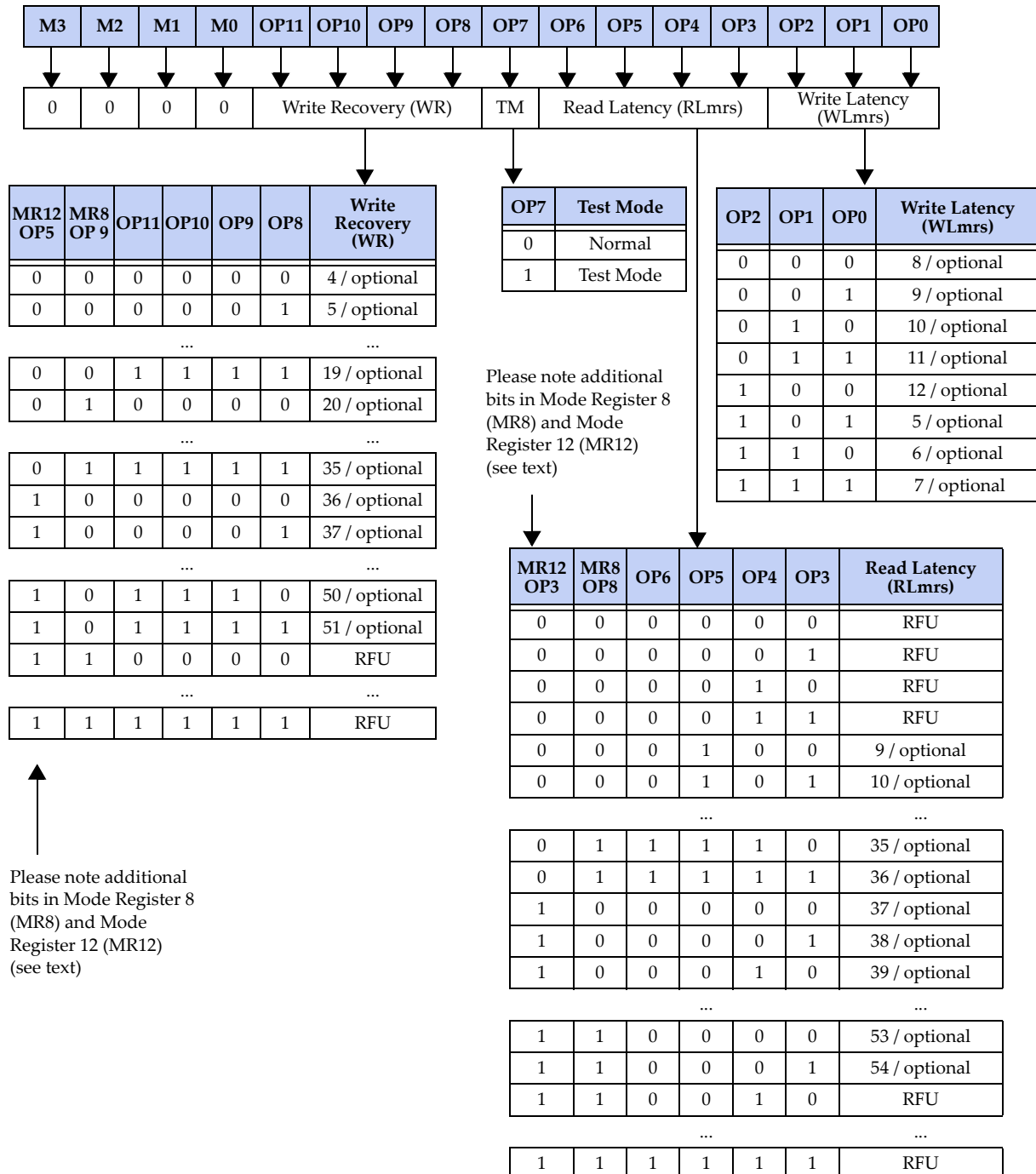


Figure 30 — Mode Register 0 (MR0) Definition