

JEDEC STANDARD

Addendum No. 1 to JESD251, Optional x4 Quad I/O With Data Strobe

JESD251-1.01

(Minor editorial revision to JESD251-1, October 2018)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Foreword

This document was prepared by the JC42.4_3 Serial Flash task group authorized by the JC-42.4 Non-Volatile Memory subcommittee.

This standard is intended for use by SoC, ASIC, ASSP, and FPGA developers or vendors interested in incorporating an initiator (sometimes called ‘controller’) interface having a low signal count and high data transfer bandwidth with access to multiple sources of target devices compliant with the interface. It is also, intended for use by peripheral developers or vendors interested in providing target devices compliant with the standard, including non-volatile memories, volatile memories, graphics peripherals, networking peripherals, FPGAs, sensors, etc.

Introduction

This purpose of the addendum is to add an optional 4-bit bus width (x4) to JESD251, xSPI standard. The xSPI interface currently supports a x1 interface that acts as a bridge to legacy SPI functionality as well as the x8 interface intended to achieve dramatically higher bus performance than legacy SPI memory implementations.

Legacy x4 SPI devices are currently available that support DDR operation at 100MHz which achieves a 100MB/s bus throughput. This 100MB/s data rate is about as high as the legacy quad SPI interface can achieve without adopting additional infrastructure.

The xSPI standard describes two infrastructure mechanisms that are intended to achieve higher bus throughput. First, the bus width is increased from four to eight bits. Second, a data strobe has been added to assist in host data capture. The expansion to eight bits and the addition of a data strobe doubles the bus throughput and allows the xSPI interface to achieve a 400MB/s data rate.

The gap between the legacy 100MB/s throughput and the new xSPI throughput of 400MB/s is substantial. The addendum adds a single data strobe pin to double the throughput (200MB/s).

The addendum is intended to fit within the scope of the JEDEC JESD251, xSPI standard as an optional feature. The standard specifies x1, x4 and x8 behavior. Bus width options offered by manufacturers would include: **x1/x8 (JEDEC xSPI)**, **x1/x4/x8** or **x1/x4**. Pinout of the x4 device is identical to the existing xSPI standard with the exception that the upper four bits of the I/O bus are unpopulated or unused. Besides having four fewer I/O pins, there are two other important differences between the existing x8 option and the x4 option:

1. The x4 option uses a single 8-bit byte for the Command whereas the x8 option requires two 8-bit bytes (Word) for the Command.
2. The x4 option uses a slightly different command protocol: The x8 option uses DDR mode for Commands, Address, and Data while the x4 option uses SDR mode for Commands and DDR mode for Address and Data.