

JEDEC STANDARD

SPD5118 Hub and Serial Presence Detect Device Standard

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SPD5118 HUB and SERIAL PRESENCE DETECT DEVICE STANDARD

From JEDEC Board Ballot JCB-21-42, formulated under the cognizance of JC-42.4, Non-Volatile Memory Devices, item 1852.07H.

1 Scope

This standard defines the specifications of interface parameters, signaling protocols, and features for DDR5 Serial Presence Detect EEPROM with Hub function (SPD5 Hub) and integrated Temperature Sensor (TS) as used for memory module applications. The Hub feature allows isolation of a local bus from a Controller host bus. The designation SPD5118 or generic term SPD5 Hub refers to the devices specified by this standard.

The purpose is to provide a standard for the SPD5 Hub devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

Unless otherwise noted in the document, any illegal operation is not allowed and device operations is not guaranteed.

The designation SPD5118 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Definition of SPD5 5118 Hub Device for Memory Module Applications

2.1 Device Standard

2.1.1 Description

The SPD5 Hub device family contains 1024 bytes of non-volatile memory arranged as 16 blocks of 64 bytes per block. Each block may optionally be write protected via software command. Write protection for each block may be overridden in an offline programmer environment while overrides are prevented in normal use. The SPD5 Hub device operate from 1.8 V nominal power supply input. The SPD5 Hub device is intended to operate up to 12.5 MHz on a 1.0V I²C Basic bus or up to 1 MHz on a 1.0 V to 3.3 V I²C bus. The SPD5 Hub devices are intended to interface to I²C/I³C Basic buses which have multiple devices on a shared bus, and must be uniquely addressed with fixed addressing on the same bus.

All SPD5 Hub devices respond to specific pre-defined I²C/I³C Basic device select codes on a host interface bus. The SPD5118 devices also incorporate a second local I²C/I³C Basic bus and pass through of commands from the host bus onto the local bus for addressing of I²C/I³C Basic devices on the local bus (Hub function).

The SPD5118 device incorporates thermal sensing capability which is controlled and read over I²C/I³C Basic bus.

2.1.2 Common Features Summary:

Table 1 — Device Part Numbers and Feature Summary

Part Number	Hub Function	Internal Thermal Sensor	Non Volatile Memory (Bytes)	Temperature Range
SPD5118	Yes	Yes	1024	-40 °C to +125 °C

- Two wire I²C or I3C Basic bus serial interface
- Single device load on the Host bus
- Up to 12.5 MHz transfer rate
- 1.8 V, 1.0 V power supply input
- 1.0 V Push Pull I/O levels
- 1.0 V, 1.1 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V Open Drain IO levels
- 1024 Bytes of non-volatile memory (16 blocks; 64 bytes per block)
- Hub Function
- Integrated Temperature Sensor
- Packet Error Check (PEC) Function
- Parity Error Check Function
- Bus Reset Function
- Up to 8 unique addressing
- In Band Interrupt (IBI)
- Write protection for each block of NVM
- 9-pin thermally enhanced DFN package

2.2 Device Power Up

The SPD5 Hub device has one VDDSPD supply input.

In order to prevent inadvertent operations during power up, a Power On Reset (POR) circuit is included. On cold power on, VDDSPD input supply must rise monotonically between VPON and VDDSPD_{min} and VDDIO input supply must rise monotonically to VDDIO_{min} without ringback to ensure proper startup.

The SPD5 Hub device uses VDDIO supply for its IO levels and it must reach VDDIO_{min} to ensure proper operation of I²C or I3C Basic bus interface.

Once the VDDSPD and VDDIO supply is valid and stable, the SPD5 Hub device shall:

1. Once VDDSPD supply is valid and stable, within $t_{\text{Sense_HSA}}$ time, sense its HSA pin to determine if SPD5 Hub device is in application environment or in an offline tester program mode. Depending on what it sense on HSA pin, the SPD5 Hub device configures its HID code automatically based on what it detects on HSA pin at power up.
2. Enable I²C interface within t_{INIT} time and be ready to receive the command from the host. The SPD5 Hub device is ready for operation after t_{INIT} time.

2.2 Device Power Up (cont'd)

The host interface HSDA and HSCL signal pins are pulled up to a pullup voltage through a pullup resistor on the platform or on the host controller. The pullup voltage can be available before or after VDDSPD or VDDIO is valid and stable. If HSDA and HSCL pullup voltage is available before VDDSPD or VDDIO is available, the HSDA and HSCL signal is high and remains high with no leakage path or damage to the SPD Hub device.

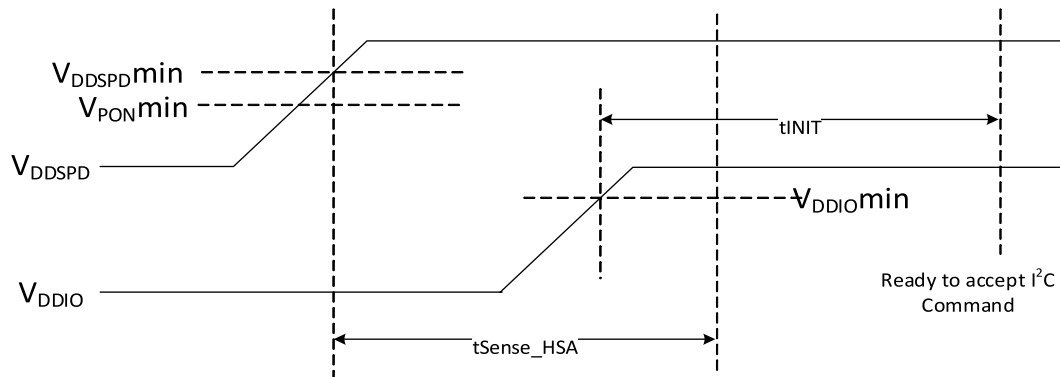


Figure 1 — Device Power Up Sequence

2.3 Device Reset and Initialization

At power down (phase during which VDDSPD input supply decreases continuously), as soon as VDDSPD input supply drops below the VDDSPD_{min}, the SPD5 Hub device does not guarantee the operation.

On warm power cycling, the VDDSPD and VDDIO input supply must remain below V_{POFF} for t_{POFF} and must meet cold power on reset timing when restoring the power.

2.4 I²C and I3C Basic Operation

At power on, by default, the SPD5 Hub device comes up in I²C mode of operation. Following applies in I²C mode:

1. The maximum operation speed is limited to 1 MHz.
2. In-band interrupts are not supported.
3. Bus reset is supported.
4. Parity check is not supported except for supported CCCs.
5. Packet Error check is not supported.

The SPD5 Hub device shall operate in the I²C mode until put into I3C Basic mode via command.

The host may put the SPD5 Hub device in I3C Basic mode by issuing SETAASA CCC.

Following applies in I3C mode.

1. The maximum operation speed is up to 12.5 MHz
2. In-band interrupts are supported
3. Bus reset is supported.
4. Parity check is always enabled by default.
5. Packet error check is supported and by default is disabled.

2.5 Device Interface - IO Voltage Configuration

The SPD5 Hub device supports configurable Open Drain and Push Pull IO levels to accommodate broad range of DDR5 platform.

2.5.1 Open Drain Interface with Internal On Die Pullup Resistor

Figure 2 shows the SPD5 Hub device configuration options for Open Drain interface for both Host side and local side of the device. In this configuration, the SPD5 Hub device supports Open Drain IO levels on both Host and Local side. However, the IO voltage levels on Host side and Local side are independent and can be different.

On Host side, the SPD5 device can support IO levels from 1.0 V to 3.3 V depending on the supply rail Host may have pulled up the resistor to. The host side pullup resistor can be on motherboard or on die inside the host logic device.

On local side, the SPD5 device can support IO levels from 1.0 V to 1.2 V and register Table 115, “MR14” [5] must be configured to ‘0’.

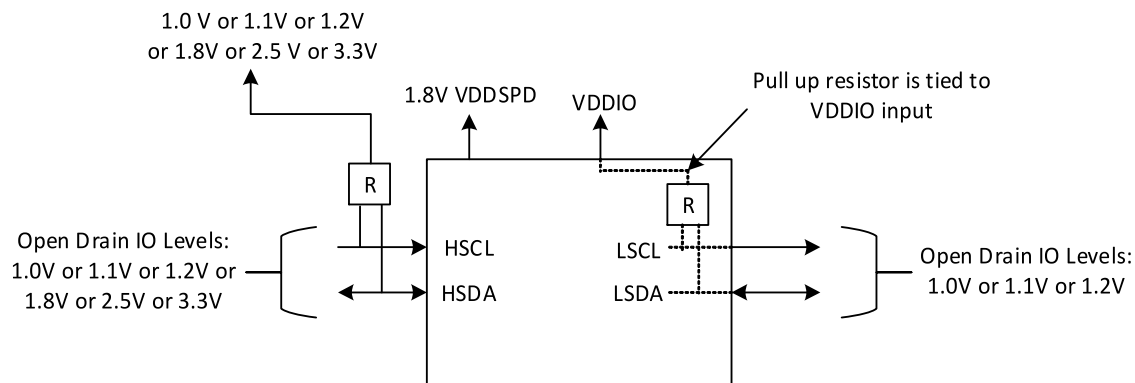


Figure 2 — Open Drain Interface; Internal Pullup Resistor

2.5.2 Open Drain Interface with External Pullup Resistor

Figure 3 shows the SPD5 Hub device configuration options for Open Drain interface for both Host side and local side of the device. In this configuration, the SPD5 device supports Open Drain IO levels on both Host and Local side. However, the IO voltage levels on Host side and Local side are independent and can be different.

On Host side, the SPD5 Hub device can support IO levels from 1.0 V to 3.3 V depending on the supply rail Host may have pulled up the resistor to. The host side pullup resistor can be on motherboard or on die inside the host logic device.

On local side, the SPD5 device can support IO levels from 1.0 V to 3.3 V and Table 115, “MR14” [5] must be configured to ‘1’.

2.5.2 Open Drain Interface with External Pullup Resistor (cont'd)

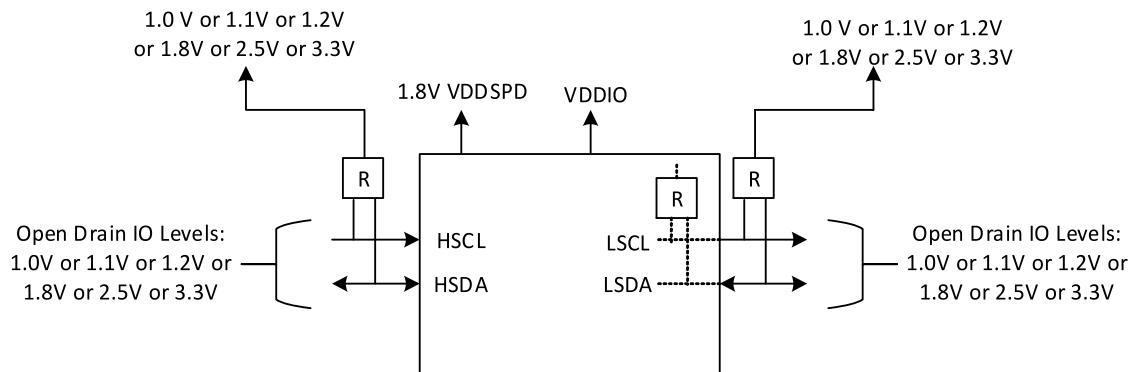


Figure 3 — Open Drain Interface; External On Board Pullup Resistor

2.5.3 Push Pull Interface with Internal On Die Pullup Resistor

The configuration option shown in Figure 4 is only supported when device is in I3C Basic mode.

Figure 4 shows the SPD5 Hub device configuration options for Push Pull interface for both Host side and local side of the device. In this configuration, the SPD5 Hub device supports Push Pull IO levels on both Host and Local side. However, the pullup IO voltage levels on Host side and Local side are independent and can be different.

On Host side, the SPD5 Hub device can support IO levels from 1.0 V to 1.2 V. The host side pullup resistor can be on motherboard or on die inside the host logic device.

On local side, the SPD5 Hub device can support IO levels from 1.0 V to 1.2V and Table 115, “MR14” [5] can be configured to ‘0’ or ‘1’.

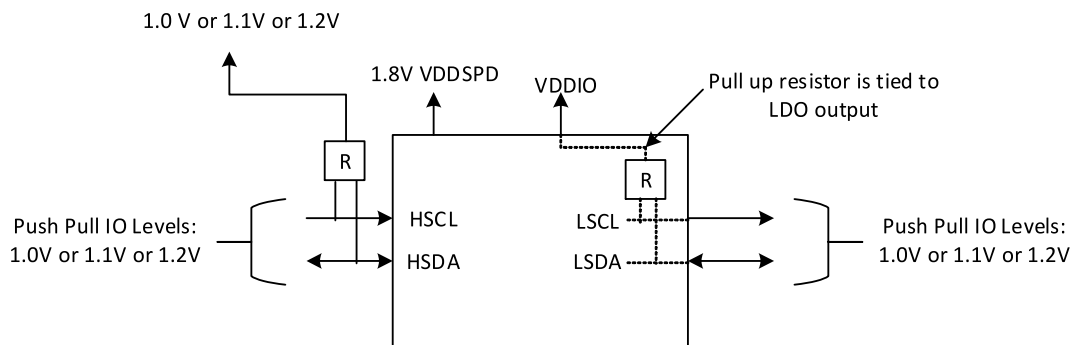


Figure 4 — Push Pull Interface; On Die Pullup

2.6 Device Interface - Protocol

The 7-bit serial address of the SPD5 Hub device and all local devices behind the SPD5 Hub applies to both I²C and I3C Basic mode of operation identically.

2.6.1 Serial Address of the SPD5 Hub Device

The SPD5 Hub device type ID is 4-bit binary value of 1010b.

The SPD5 Hub device samples the status of the HSA pin on power up. The sampled status of the HSA pin determine the unique host ID (HID) of the device. The host identifier value (HID) is merged with the SPD5 Hub device type 1010 xxxb to establish the 7-bit address (SPD5 Hub DevID[6:0]) for the device on the I²C or I3C Basic bus as shown in Table 2. For example, if the value sensed on HSA pin identifier is 2 (010 binary), then the unique 7-bit address for this device is 1010 010b.

Table 2 — 7-bit Address of SPD5 Hub Device

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	0	HID[2]	HID[1]	HID[0]	R/W
SPD5 Hub Device Type ID (LID)				Host ID (HID)			Read/Write

2.6.2 Serial Address of the Local Devices

Each local device behind the SPD5 Hub device has a unique 4 bit local device ID (LID) code. For example the PMIC local device type ID is 4-bit binary value of 1001b.

The 3 HID bits of the local device type has a default value of ‘111’ and is merged with its unique 4 bit local ID code to establish the 7-bit address (DevID[6:0]) for the local device on the I²C or I3C Basic bus as shown in Table 3. For example, the PMIC local device behind the SPD5 Hub has 7-bit address of 1001 111b.

Table 3 — 7-bit Address of the Local Devices (e.g., PMIC Device)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	1	1	1	1	R/W
Local Device Type ID (LID)				Host ID (HID)			Read/Write

2.6.3 Switch from I²C Mode to I3C Basic Mode

By default, when SPD5 Hub first powers on, it operates in I²C mode. The SPD5 Hub device shall operate in I²C mode until put into I3C Basic mode via command.

In I²C mode, the host is allowed to issued only 3 CCCs (DEVCTRL, SETHID, SETAASA). All other CCCs are not supported and the SPD5 Hub device may simply ignore it. The Host must issue DEVCTRL and SETHID CCC first (if required) followed by SETAASA CCC.

The Host puts the SPD5 Hub device in I3C Basic mode by issuing SETAASA CCC.

When SETAASA CCC is registered by the SPD5 Hub device, it updates the Table 117, “MR18” [5] to ‘1’.

When SETHID CCC is registered by the SPD5 Hub device, it stops the 3-bit HID translation for the local Target device as explained in clause 2.6.6.

2.6.4 Switch from I3C Basic Mode to I²C Mode

The Host can put the SPD5 Hub device back in I²C mode from I3C mode at any time by issuing RSTDAA CCC.

When RSTDAA CCC is registered by the SPD5 Hub device, it updates the Table 117, “MR18” [5] to ‘0’.

2.6.5 SPD5 Hub Device Selection

The host can access any SPD5 Hub device as shown in Table 4 in both I²C mode and I3C Basic mode. The last 3 bits represent the HID bits.

Table 4 — 7-bit Address of Each Hub Devices on I²C/I3C Bus

Host Access to:	7-bit Address
DIMM 0 SPD Hub	1010 000
DIMM 1 SPD Hub	1010 001
DIMM 2 SPD Hub	1010 010
DIMM 3 SPD Hub	1010 011
DIMM 4 SPD Hub	1010 100
DIMM 5 SPD Hub	1010 101
DIMM 6 SPD Hub	1010 110
DIMM 7 SPD Hub	1010 111

2.6.6 Local Device Selection Through the SPD5 Hub Device (Before SETHID CCC)

By default, the SPD5 Hub device and all local Target devices powers up in I²C mode of operation, Prior to Host issuing SETHID CCC, the host can access the any local device behind the SPD5 Hub device. To access the local device, the host sends 7-bit address that is made up of 4 bits of local device code (LID) followed by the 3 bits of HID code. The LID code represents which local device host is intended to target. The HID code represents which DIMM the local device resides on. Table 5 shows an example of four different local device address codes behind SPD5 Hub on each DIMM.

Table 5 — 7-bit Address of Local Devices on I²C/I3C Bus

Host Access to:	7-bit Address LID = 1011 (RCD)	7-bit Address LID = 1001 (PMIC)	7-bit Address LID = 0010 (TS0)	7-bit Address LID = 0110 (TS1)
DIMM 0 Local Device	1011 000	1001 000	0010 000	0110 000
DIMM 1 Local Device	1011 001	1001 001	0010 001	0110 001
DIMM 2 Local Device	1011 010	1001 010	0010 010	0110 010
DIMM 3 Local Device	1011 011	1001 011	0010 011	0110 011
DIMM 4 Local Device	1011 100	1001 100	0010 100	0110 100
DIMM 5 Local Device	1011 101	1001 101	0010 101	0110 101
DIMM 6 Local Device	1011 110	1001 110	0010 110	0110 110
DIMM 7 Local Device	1011 111	1001 111	0010 111	0110 111

The SPD5 Hub Device monitors the LID code coming from the host. When it detects the host access is for the Target device, it compares the last 3 bits of the HID information (shown in Red) coming from the host against its own unique HID code that it has stored at power on. It compares each 3 bits one at a time. If there is a match, the SPD5 Hub device substitutes that bit with '1' and forward it to the local device interface. If there is a mismatch, the SPD5 Hub device substitutes that bit with '0' and forwards it to the local device interface. As a result, only the targeted local device will see its last three HID bits as '111' and all non-targeted local devices will see its last three HID bits as anything other than '111' which is not a valid code as shown in Table 3.

2.6.6 Local Device Selection Through the SPD5 Hub Device (Before SETHID CCC) (cont'd)

There are two exceptions when SPD5 Hub device does not substitute its own HID code when it forwards it to the local Target interface:

1. Host issues Start followed by 7'h7E with W=0 (or Host issues Start followed by 0xFC).
2. After SPD5 Hub executes SETHID CCC command that Host issues. See clause 2.6.7.

Figure 5 gives an example of Host accessing local RCD Device on DIMM0. The figure shows Host sends 7-bit address '1011 000'. Each SPD5 Hub devices receives this address. Each SPD5 Hub device forward first four bits of binary address '1011' (LID) on the local device interface. Each SPD5 Hub compares last 3 bits of binary address '000' from the host against its own unique HID code and substitutes the bit on the local device interface.

	Hub SPD		RCD		PMIC0		PMIC1		PMIC2		TS0		TS1	
DIMM0	101 0000	50	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F
DIMM1	101 0001	51	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E
DIMM2	101 0010	52	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D
DIMM3	101 0011	53	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C
DIMM4	101 0100	54	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B
DIMM5	101 0101	55	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A
DIMM6	101 0110	56	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1001	59	101 1001	59	101 1001	59	101 1001	59	101 1001	59	101 1001	59
DIMM7	101 0111	57	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1000	58	101 1000	58	101 1000	58	101 1000	58	101 1000	58	101 1000	58

Figure 5 — Example: Host Accessing RCD on DIMM 0

Figure 6 gives another example of Host accessing local Temperature Sensor 0 device on DIMM3. The figure shows Host sends 7-bit address '0010 011'. Each SPD5 hub devices receives this address. Each SPD5 Hub device forward first four bits of binary address '0010' (LID) on the local device interface. Each SPD5 Hub compares last 3 bits of binary address '011' from the host against its own unique HID code and substitutes the bit on the local device interface.

2.6.6 Local Device Selection Through the SPD5 Hub Device (Before SETHID CCC) (cont'd)

	Hub SPD		RCD		PMIC0		PMIC1		PMIC2		TS0		TS1	
DIMM0	101 0000	50	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0100	14	001 0100	14	001 0100	14	001 0100	14	001 0100	14	001 0100	14
DIMM1	101 0001	51	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0101	15	001 0101	15	001 0101	15	001 0101	15	001 0101	15	001 0101	15
DIMM2	101 0010	52	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0110	16	001 0110	16	001 0110	16	001 0110	16	001 0110	16	001 0110	16
DIMM3	101 0011	53	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0111	17	001 0111	17	001 0111	17	001 0111	17	001 0111	17	001 0111	17
DIMM4	101 0100	54	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0000	10	001 0000	10	001 0000	10	001 0000	10	001 0000	10	001 0000	10
DIMM5	101 0101	55	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0001	11	001 0001	11	001 0001	11	001 0001	11	001 0001	11	001 0001	11
DIMM6	101 0110	56	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0010	12	001 0010	12	001 0010	12	001 0010	12	001 0010	12	001 0010	12
DIMM7	101 0111	57	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0011	13	001 0011	13	001 0011	13	001 0011	13	001 0011	13	001 0011	13

Figure 6 — Example: Host Accessing Temperature Sensor 0 on DIMM 3

2.6.7 Local Device Selection Through the SPD5 Hub Device (After SETHID CCC)

When SETHID CCC is registered by the SPD5 Hub device, it stops the 3-bit HID translation for the local Target device as explained in clause 2.6.6. After Host sends SETHID CCC, the Host still access the all Target devices behind the SPD5 Hub as shown in Table 5. There is no change in how Host access the SPD5 Hub device and all local Target devices behind the SPD5 Hub device before or after SETHID CCC.

2.6.8 I²C Target Protocol - Host to SPD5 Hub Device

The SPD5 Hub devices operate on a standard I²C serial interface. Transactions where the SPD5 Hub device is the targeted Target device begin with the Host issuing a START condition followed by a 7-bit SPD5 Hub device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the SPD5 Hub device typically replies with an ACK unless there are conditions when it may passively assert a NACK.

2.6.8 I²C Target Protocol - Host to SPD5 Hub Device (cont'd)

The SPD5 Hub device does not allow any read or write operations to its non-volatile memory when it is busy with internal write operation to non-volatile memory. The host should either check Table 130, “MR48” [3] register status or ensure that Write time (t_w) parameter is satisfied prior to performing another write or read to operations non-volatile memory. If host violates this and performs either write or read operation to non-volatile memory then SPD5 Hub device ACKs the address byte to allow possible volatile register access. However, the SPD5 Hub device NACKs the subsequent write or read operation if MemReg = ‘1’ and sets the Table 134, “MR52” [7] = ‘1’.

The SPD5 Hub device does allow any read or write operation to its volatile memory (i.e., MemReg = ‘0’) when it is busy with internal write operation to non-volatile memory.

To allow compatibility with legacy I²C host controller, the SPD5 Hub device offers two ways to address 1024 bytes of non volatile memory when it is operating in I²C mode only. By default, the SPD5 Hub device accepts 1 byte of address which covers first 128 bytes of non-volatile memory. The host must select the page pointer through volatile register Table 112, “MR11” [2:0] to address the entire 1024 bytes of non-volatile memory.

Alternatively, at initial power on, the host can set the Table 112, “MR11” [3] = ‘1’ to address the entire 1024 bytes of non-volatile memory with 2 bytes of address and hence not required to go through page selection to address entire non-volatile memory.

This 1 byte address mode is only applicable to SPD5 Hub device and it is not applicable to PMIC or TS or RCD device in I²C mode.

The SPD5 Hub device volatile register space does not require the page selection process as all volatile registers are within first 128 bytes.

2.6.8.1 Write Operation - Data Packet

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = ‘1’) or an internal register (MemReg = ‘0’). When MemReg = ‘0’, there is no concept of “Block Address”; Block Address bits are treated simply Upper Address bits.

Table 6 — Write Command Data Packet; Table 13, “MR11” [3] = ‘0’

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	Data								A	
	...								A	
	Data								A	
NOTE 1 In I2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.										

2.6.8.1 Write Operation - Data Packet (cont'd)

Table 7 — Write Command Data Packet; Table 112, “MR11” [3] = ‘1’

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	0	0	0	0	Blk Addr [4:1] ²			A		
	Data								A	
	...								A	
	Data								A	
NOTE 1	In I2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.									
NOTE 2	The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.									

2.6.8.2 Read Operation - Data Packet

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = ‘1’) or an internal register (MemReg = ‘0’). When MemReg = ‘0’, there is no concept of “Block Address”; Block Address bits are treated simply Upper Address bits.

Table 8 — Read Command Data Packet; Table 112, “MR11” [3] = ‘0’

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
Sr	1	0	1	0	HID			R=1	A ²	
	Data								A	
	...								A	
	Data								N	Sr or P
NOTE 1	In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation including another Repeat Start is considered an illegal operation.									
NOTE 2	If Target device NACKs during Repeat Start for any reason, the host my re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. The device may eventually ACK.									

2.6.8.2 Read Operation - Data Packet (cont'd)

Table 9 — Read Command Data Packet; Table 112, “MR11” [3] = ‘1’

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	0	0	0	0	Blk Addr [4:1] ²			A		
Sr	1	0	1	0	HID			R=1	A ³	
	Data								A	
	...								A	
	Data								N	Sr or P
NOTE 1	In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation including another Repeat Start is considered an illegal operation.									
NOTE 2	The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.									
NOTE 3	If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times as it may desire. The device may eventually ACK.									

2.6.8.3 Default Read Address Pointer Mode

During normal operation of the DDR5 DIMM, the host periodically may poll critical information from the same location. An example may be the SPD5 Hub device's temperature readout. To help improve the efficiency of the I²C bus protocol, the SPD5 Hub offers a default read address pointer mode so that whenever the SPD5 Hub device sees the STOP operation on its HSCL and HSDA bus, its read address pointer is always resets to default address. The default read pointer address mode is enabled through register Table 117, “MR18” [4] and default starting address for read operation is selectable through register Table 117, “MR18” [3:2]. This allows host to read the read command data packet as shown in Table 10 compared to as shown in Table 9. The default read address pointer reduces the packet overhead by 3 bytes. The host typically enables this mode when the normal operation of the DDR5 DIMM begins. The default read address pointer mode is only applicable to volatile register space (i.e., MemReg = ‘0’).

Table 10 — Read Command Data Packet with Default Address Pointer Mode

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	1	0	1	0	HID			R=1	A	
	Data								A	
	...								A	
	Data								N	Sr or P

2.6.9 I²C Target Protocol - Host to Local Device Through SPD5 Hub Device

2.6.9.1 Write Operation - Data Packet

Table 11 — Write Command Data Packet (e.g., TS)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	0	0	1	0	HID			W=0	A	
	Address [7:0]								A	
	Data								A	
	Data								A	
	...								A	
	Data								A	
										Sr or P
NOTE 1 In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation, including another Repeat Start, is considered an illegal operation.										

Table 12 — Write Command Data Packet (e.g., PMIC)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	0	1	HID			W=0	A	
	Address [7:0]								A	
	Data								A	
	Data								A	
	...								A	
	Data								A	Sr or P
NOTE 1 In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation, including another Repeat Start, is considered an illegal operation.										

When Host makes any write request to the RCD device, the RCD protocol has PEC check in the last byte. The SPD simply treats the last byte as Data like any other bytes as shown in Table 14. The RCD device requires valid stable input clock (DCK_t, DCK_c), Reset_n and DCS_n to allow any read or write access on its I²C interface.

2.6.9.1 Write Operation - Data Packet (cont'd)

Table 13 — Write Command Data Packet (e.g., RCD; PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	1	1	HID			W=0	A	
	Data (I ² C Bus Command)								A	
	Data (Byte Count=8)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num [7:0])								A	
	Data (Reg Num [7:0])								A	
	Data (Wr Data [31:24])								A	
	Data (Wr Data [23:16])								A	
	Data (Wr Data [15:8])								A	
Data (Wr Data [7:0])								A	Sr or P	
NOTE 1 In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation, including another Repeat Start, is considered an illegal operation.										

Table 14 — Write Command Data Packet (e.g., RCD; PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	1	1	HID			W=0	A	
	Data (I ² C Bus Command)								A	
	Data (Byte Count=8)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num [7:0])								A	
	Data (Reg Num [7:0])								A	
	Data (Wr Data [31:24])								A	
	Data (Wr Data [23:16])								A	
	Data (Wr Data [15:8])								A	
	Data (Wr Data [7:0])								A	
	Data (PEC [7:0])								A	
NOTE 1 In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation, including another Repeat Start, is considered an illegal operation.										

2.6.9.2 Read Operation - Data Packet

Table 15 — Read Command Data Packet (e.g., TS)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	0	0	1	0	HID			W=0	A	
	Address [7:0]								A	
Sr	0	0	1	0	HID			R=1	A ²	
	Data								A	
	Data								A	
	...								A	
	Data								N	
NOTE 1	In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation including, another Repeat Start, is considered an illegal operation.									
NOTE 2	If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire.									

Table 16 — Read Command Data Packet (e.g., PMIC)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	0	1	HID			W=0	A	
	Address [7:0]								A	
Sr	1	0	0	1	HID			R=1	A ²	
	Data								A	
	Data								A	
	...								A	
	Data								N	
NOTE 1	In I2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I2C mode. Any other operation, including another Repeat Start, is considered an illegal operation.									
NOTE 2	If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire.									

When Host makes any read request to the RCD device, the RCD protocol has PEC check for the RCD address information as well as data returned by the RCD. The SPD5 Hub simply treats the PEC information as data byte like any other data byte as shown in Table 18. The SPD5 Hub device does not check for the PEC. The RCD device requires valid stable input clock (DCK_t, DCK_c), Reset_n, and DCS_n to allow any read or write access on its I²C interface.

2.6.9.2 Read Operation - Data Packet (cont'd)

Table 17 — Read Command Data Packet (e.g., RCD; PEC Disabled; Legacy Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	1	1	HID			W=0	A	
	Data (I ² C Bus Command)								A	
	Data (Byte Count=4)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num [7:0])								A	
	Data (Reg Num [7:0])								A	
S	1	0	1	1	HID			W=0	A	
	Data (I ² C Bus Command)								A	
Sr	1	0	1	1	HID			R=1	A ²	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data [31:24])								A	
	Data (Rd Data [23:16])								A	
	Data (Rd Data [15:8])								A	
	Data (Rd Data [7:0])								A	Sr or P
NOTE 1	In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation, including another Repeat Start, is considered an illegal operation.									
NOTE 2	If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire.									

2.6.9.2 Read Operation - Data Packet (cont'd)

Table 18 — Read Command Data Packet (e.g., RCD; PEC Enabled; Legacy Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	1	1	HID			W=0	A	
	Data (I ² C Bus Command)								A	
	Data (Byte Count=4)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num [7:0])								A	
	Data (Reg Num [7:0])								A	
	Data (PEC [7:0])								A	P
S	1	0	1	1	HID			W=0	A	
	Data (I ² C Bus Command)								A	
Sr	1	0	1	1	HID			R=1	A ²	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data [31:24])								A	
	Data (Rd Data [23:16])								A	
	Data (Rd Data [15:8])								A	
	Data (Rd Data [7:0])								A	
	Data (PEC [7:0])								A	Sr or P
NOTE 1 In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation, including another Repeat Start, is considered an illegal operation.										
NOTE 2 If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire.										

2.6.9.2 Read Operation - Data Packet (cont'd)

Table 19 — Read Command Data Packet (e.g., RCD; PEC Disabled; Optimized Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	1	0	1	1	HID			W=0	A	
	Data (I ² C Bus Command)								A	
	Data (Byte Count=4)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num [7:0])								A	
	Data (Reg Num [7:0])								A	
Sr	1	0	1	1	HID			R=1	A ²	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data [31:24])								A	
	Data (Rd Data [23:16])								A	
	Data (Rd Data [15:8])								A	
	Data (Rd Data [7:0])								A	Sr or P
NOTE 1	In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation, including another Repeat Start, is considered an illegal operation.									
NOTE 2	If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire.									

2.6.10 I3C Basic Target Protocol - Host to SPD5 Hub Device

2.6.10.1 Write Operation Data Packet

The SPD5 Hub devices operate on a standard I3C serial interface. Transactions where the SPD5 Hub device is the targeted Target device begin with the Host issuing a START condition followed by a 7-bit SPD5 Hub device address then a write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the SPD5 Hub device typically replies with an ACK unless there are conditions when it may passively assert a NACK. The “T” bit carries Parity information from the Host for each byte.

The SPD5 Hub device does not allow any read or write operations to its non-volatile memory when it is busy with internal write operation to non-volatile memory. The host should either check Table 130, “MR48” [3] register status or ensure that Write time (t_w) parameter is satisfied prior to performing another write or read to operations non-volatile memory. If host violates this and performs either write or read operation to non-volatile memory then SPD5 Hub device always ACKs the address byte. In a subsequent byte, the device ignores the write operation if MemReg = ‘1’ and sets the Table 134, “MR52” [7] = ‘1’ and requests IBI if IBI function is enabled. Subsequently, if host continues to do the read operation with Repeat Start, the SPD5 Hub device NACKs.

The SPD5 Hub device does allow any read or write operation to its volatile memory (i.e., MemReg = ‘0’) when it is busy with internal write operation to non-volatile memory.

2.6.10.1 Write Operation Data Packet (cont'd)

The Packet Error Code (PEC) function is disabled by default when the SPD5 Hub device is put in I3C Basic mode. The host may optionally enable this function through Table 117, “MR18” [7] or DEVCTRL CCC. If enabled, the PEC is appended at the end of all transactions. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length pre-maturely for Write operation.

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = ‘1’) or an internal register (MemReg = ‘0’). When MemReg = ‘0’, there is no concept of “Block Address”; Block Address bits are treated simply Upper Address bits.

Table 20 — Write Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W=0	A ^{1,2,3}	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1] ⁴			T		
	Data								T	
	...								T	
	Data								T	
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).									
NOTE 2	The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 3	The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 4	The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.									
NOTE 5	Repeat Start or Repeat Start with 7'h7E.									

Table 21 — Write Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W=0	A ^{1,2,3}	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			W=0	Blk Addr [4:1] ⁴				T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr ⁵ or P
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).									
NOTE 2	The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 3	The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation									
NOTE 4	The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.									
NOTE 5	Repeat Start or Repeat Start with 7'h7E.									

2.6.10.1 Write Operation Data Packet (cont'd)

The host may optionally allow SPD5 Hub device to request IBI. For this case, the transactions to the SPD5 Hub device begin with the I3C Basic host issuing a START condition followed by 7'h7E and then write bit. If SPD5 Hub device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If SPD5 Hub device has no pending IBI, there is no action taken by SPD5 Hub. Table 22 and Table 23 show the I3C bus write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 23, PEC calculation does not include IBI header byte (7'h7E followed by W=0).

Table 22 — Write Command Data Packet with IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,3}	
Sr	1	0	1	0	HID			W=0	A ^{2,3,4}	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1] ⁵				T	
	Data								T	
	...								T	
	Data								T	
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).									
NOTE 2	See Figure 9 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).									
NOTE 3	The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 4	The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 5	The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.									
NOTE 6	Repeat Start or Repeat Start with 7'h7E.									

2.6.10.1 Write Operation Data Packet (cont'd)

Table 23 — Write Command Data Packet with IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,3}	
Sr	1	0	1	0	HID			W=0	A ^{2,3,4}	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			W=0	Blk Addr [4:1] ⁵				T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr ⁶ or P
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).									
NOTE 2	See Figure 9 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).									
NOTE 3	The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 4	The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 5	The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.									
NOTE 6	Repeat Start or Repeat Start with 7'h7E.									

2.6.10.2 Read Operation Data Packet

The transactions to SPD5 Hub Target device begin with the I3C Basic Host issuing a START condition followed by a 7-bit SPD5 Hub device type identifier then a write bit. All I3C bus data are transmitted with the most significant bit MSB first. During select code transmission, the SPD5 Hub device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 24. The “T” bit carries Parity information from the host prior to Repeated START. After Repeated START, “T” bit carries information from SPD5 Hub device to Host indicating Continuous (‘1’) or Stop (0’) whether it is transmitting the last byte or not.

The Packet Error Code (PEC) function is disabled by default when SPD5 Hub device is put in I3C Basic mode. The host may optionally enable this function through Table 117, “MR18” [7] or DEVCTRL CCC. If enabled, the PEC is appended as shown in Table 25. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length pre-maturely for Read operation

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = ‘1’) or an internal register (MemReg = ‘0’). When MemReg = ‘0’, there is no concept of “Block Address”; Block Address bits are treated simply Upper Address bits.

2.6.10.2 Read Operation Data Packet (cont'd)

Table 24 — Read Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W=0	A ^{1,2,3}	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1] ⁴			T		
Sr	1	0	1	0	HID			R=1	A/N ^{5,6}	
	Data								T=1	
	...								T=1	
	Data								T=1 ^{7,8}	Sr ⁹ or P
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).									
NOTE 2	The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 3	The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 4	The memory size of SPD5 hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.									
NOTE 5	If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors the SPD5 Hub may eventually ACK.									
NOTE 6	See Figure 9 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).									
NOTE 7	See Figure 10 to see how Host ends Target device operation.									
NOTE 8	For NVM read memory access (i.e., MemReg = '1'), when last byte is reached (1024 Byte) or for volatile memory access (i.e., MemReg = '0'), when last byte (i.e., MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 11 to see how Target device ends the operation followed by Host STOP operation.									
NOTE 9	Repeat Start or Repeat Start with 7'h7E.									

2.6.10.2 Read Operation Data Packet (cont'd)

Table 25 — Read Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			W=0	A ^{1,2,3}	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			R=1	Blk Addr [4:1] ⁴			T		
	PEC								T	
Sr	1	0	1	0	HID			R=1	A/N ^{5,6}	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 ⁷	
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).									
NOTE 2	The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 3	The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 4	The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.									
NOTE 5	If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to PEC error parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the SPD5 Hub may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select code of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.									
NOTE 6	See Figure 9 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).									
NOTE 7	See Figure 11 to see how Target device ends the operation followed by Host STOP operation.									
NOTE 8	Repeat Start or Repeat Start with 7'h7E.									

The host may optionally allow SPD5 Hub device to request IBI. For this case, the transactions to the SPD5 Hub device begin with the I3C Basic host issuing a START condition followed by 7'h7E and then write bit. If SPD5 Hub device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If SPD5 Hub device has no pending IBI, there is no action taken by SPD5 Hub. Table 26 and Table 27 show the I3C Basic bus read command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 27, PEC calculation (from Host to SPD5 Hub) does not include IBI header byte (7'h7E followed by W=0).

2.6.10.2 Read Operation Data Packet (cont'd)

Table 26 — Read Command Data Packet with IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,3}	
Sr	1	0	1	0	HID			W=0	A ^{2,3,4}	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1] ⁵			T		
Sr	1	0	1	0	HID			R=1	A/N ^{6,7}	
	Data								T=1	
	...								T=1	
	Data								T=1 ^{8,9}	

NOTE 1 See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).

NOTE 2 See Figure 9 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).

NOTE 3 The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 4 The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.

NOTE 6 See Figure 9 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 7 If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the SPD5 Hub may eventually ACK.

NOTE 8 See Figure 10 to see how Host ends Target device operation.

NOTE 9 For NVM read memory access (i.e., MemReg = '1'), when last byte is reached (1024 Byte) or for volatile memory access (i.e., MemReg = '0'), when last byte (i.e., MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 11 to see how Target device ends the operation followed by Host STOP operation.

NOTE 10 Repeat Start or Repeat Start with 7'h7E.

2.6.10.2 Read Operation Data Packet (cont'd)

Table 27 — Read Command Data Packet with IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,3}	
Sr	1	0	1	0	HID			W=0	A ^{2,3,4}	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			R=1	Blk Addr [4:1] ⁵				T	
	PEC								T	
Sr	1	0	1	0	HID			R=1	A/N ^{6,7}	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 ⁸	Sr ⁹ or P
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).									
NOTE 2	See Figure 9 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).									
NOTE 3	The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 4	The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 5	The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.									
NOTE 6	See Figure 9 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).									
NOTE 7	If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the SPD5 Hub may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.									
NOTE 8	See Figure 11 to see how Target device ends the operation followed by Host STOP operation.									
NOTE 9	Repeat Start or Repeat Start with 7'h7E.									

2.6.10.3 Default Read Address Pointer Mode

This mode works the same exact way as explained in clause 2.6.8.3. Table 28 and Table 29 show the read command data packet for PEC function disabled and enabled respectively. When PEC function is enabled, Table 117, “MR18” [1] sets the number of bytes that SPD5 Hub device sends out followed by the PEC calculation. If PEC is enabled, the host must complete the burst length as indicated in Table 117, “MR18” [1] register. In other words, the host must not interrupt the burst length pre-maturely for default address pointer read operation. The default read address pointer mode is only applicable to volatile register space (i.e., MemReg = ‘0’).

2.6.10.3 Default Read Address Pointer Mode (cont'd)**Table 28 — Read Command Data Packet with Read Address Pointer Mode; PEC Disabled**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			R=1	A ¹	
	Data								T=1	
	...								T=1	
	Data								T=1 ^{2,3}	Sr ⁴ or P
NOTE 1	The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 2	See Figure 10 to see how Host ends Target device operation.									
NOTE 3	When last byte (i.e., MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 11 to see how Target device ends the operation followed by Host STOP operation.									
NOTE 4	Repeat Start or Repeat Start with 7'h7E.									

Table 29 — Read Command Data Packet with Read Address Pointer Mode; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			R=1	A ¹	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 ²	
NOTE 1	The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 2	See Figure 11 to see how Target device ends the operation followed by STOP operation									
NOTE 3	Repeat Start or Repeat Start with 7'h7E.									

Table 30 — Read CMD Data Packet with Read Address Pointer Mode and IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,2}	
Sr	1	0	1	0	HID			R=1	A ^{2,3}	
	Data								T=1	
	...								T=1	
	Data								T=1 ^{4,5}	Sr ⁶ or P
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).									
NOTE 2	The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 3	See Figure 9 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).									
NOTE 4	See Figure 10 to see how Host ends Target device operation.									
NOTE 5	When last byte (i.e., MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 11 to see how Target device ends the operation followed by Host STOP operation.									
NOTE 6	Repeat Start or Repeat Start with 7'h7E.									

2.6.10.3 Default Read Address Pointer Mode (cont'd)

Table 31 — Read CMD Data Packet with Read Address Pointer Mode and IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,2}	
Sr	1	0	1	0	HID			R=1	A ^{2,3}	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 ⁴	
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).									
NOTE 2	The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 3	See Figure 9 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).									
NOTE 4	See Figure 11 to see how Target device ends the operation followed by STOP operation									
NOTE 5	Repeat Start or Repeat Start with 7'h7E.									

2.6.11 I3C Basic Target Protocol - Host to Local Device (Through SPD5 Hub Device)

2.6.11.1 Write Operation - Data Packet

Table 32 to Table 37 show examples of write command data packet for different types of local devices behind the SPD5 Hub. These example do not show the optional IBI header byte that Host may choose to use. All local devices behind SPD5 Hub device also supports the IBI header byte similar to as shown in Table 22 and Table 23. Refer to the device specific data sheet.

Table 32 — Write Command Data Packet (e.g., TS); PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	0	1	0	HID			W=0	A ^{1,2,3}	
	Address [7:0]								T	
	Data								T	
	Data								T	
	...								T	
	Data								T	Sr ⁴ or P
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr; bit [7]).									
NOTE 2	The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 3	The TS device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 4	Repeat Start or Repeat Start with 7'h7E.									

2.6.11.1 Write Operation - Data Packet (cont'd)

Table 33 — Write Command Data Packet (e.g., TS); PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	0	1	0	HID			W=0	A ^{1,2,3}	
	Address [7:0]								T	
	CMD			W=0	0	0	0	0	T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr ⁴ or P
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).									
NOTE 2	The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 3	The TS device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 4	Repeat Start or Repeat Start with 7'h7E.									

Table 34 — Write Command Data Packet (e.g., PMIC); PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	0	1	HID			W=0	A ^{1,2,3}	
	Address [7:0]								T	
	Data								T	
	Data								T	
	...								T	
	Data								T	Sr ⁴ or P
NOTE 1	See Figure 7 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).									
NOTE 2	The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.									
NOTE 3	The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 4	Repeat Start or Repeat Start with 7'h7E.									