

JEDEC STANDARD

PMIC50x0 Power Management IC Standard

JESD301-1A.02

Rev. 1.8.5

(Editorial Revision of JESD301-1A.01, October 2022)

March 2023

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2023
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

DO NOT VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies through entering into a license agreement.
For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107
<https://www.jedec.org/contact>

This page intentionally left blank

DEFINITION OF PMIC5000, PMIC5010 VOLTAGE REGULATOR DEVICE FOR MEMORY MODULE APPLICATIONS

Contents

	Pages
1 Scope	1
2 Device Standard	1
2.1 Description	1
2.1.1 Common Features Summary	2
2.2 Input Supply and Output Regulator Electrical Characteristics	3
2.2.1 Input Supply Electrical Characteristics	3
2.2.2 Switch Regulator Output Electrical Characteristics	4
2.2.3 Switch Regulator Efficiency	9
2.2.4 LDO Output Regulator Characteristics	10
2.2.5 PMIC AC Timing Parameters	11
2.3 I2C, I3C Basic and Interface DC and AC Electrical Characteristics	12
2.4 Thermal Characteristics	17
2.5 Absolute Maximum Rating	18
2.6 Example Schematic	20
2.7 Functional Operation	23
2.7.1 PMIC Input Voltage Supplies and Ramp Condition	23
2.7.2 Power Up Initialization Sequence	23
2.7.3 Power Up Sequence	25
2.7.4 Enabling PMIC Output Switch Voltage Regulators	29
2.7.5 Power Down Output Regulators	30
2.7.6 Power Down Output Regulators During Power On Sequence	31
2.7.7 CAMP Signal	31
2.7.7.1 Register Write Protect Function	32
2.7.7.2 Fail_n Function	32
2.7.7.3 Status Function	32
2.7.8 GSI_n Signal	33
2.7.9 State Transition Diagram	33
2.7.10 Function Interrupt - CAMP and GSI_n Output Signals	35
2.7.11 Input Power Good Status	38
2.7.12 Input Over Voltage Protection	38
2.7.13 Output Power Good Status	39
2.7.14 Output Over Voltage Protection	40
2.7.14.1 DDR5 RDIMM/LRDIMM Environment - Table 166, “Register 0x4F” [7] = ‘0’:	40
2.7.14.2 DDR5 NVDIMM or other Custom Environment: Table 166, “Register 0x4F”[7]=‘1’	40
2.7.15 Output Under Voltage and VIN_Bulk Under Voltage Lockout Protection	41
2.7.15.1 DDR5 RDIMM/LRDIMM Environment - Table 166, “Register 0x4F” [7] = ‘0’:	41

Contents (cont'd)

2.7.15.2	DDR5 NVDIMM or other Custom Environment - Table 166, “Register 0x4F” [7]='1'	41
2.7.16	Output Current Limiter Warning Event	42
2.7.17	Output High Current Consumption Warning Event	42
2.7.18	PMIC LDO Output Failure	43
2.7.19	PMIC High Temperature Warning and Critical Temperature Protection	43
2.7.20	VIN_Mgmt to VIN_Bulk Input Supply Switchover Event	44
2.7.21	Valid VIN_Mgmt Supply Detection in Switchover Mode	44
2.7.22	Packet Error Code (PEC) and Parity Error Event	44
2.8	Analog to Digital Converter (ADC)	45
2.8.1	PMIC Address ID (PID)	45
2.8.2	Error Injection	46
2.9	I2C and I3C Basic Interface Operation	46
2.10	Device Interface - Protocol	46
2.10.1	Serial Address of PMIC Device	47
2.10.2	Switch from I2C Mode to I3C Basic Mode	47
2.10.3	Switch from I3C Basic Mode to I2C Mode	47
2.10.4	I2C Target Protocol	48
2.10.4.1	Write Operation - Data Packet	48
2.10.4.2	Read Operation - Data Packet	48
2.10.4.3	Default Read Address Pointer Mode	49
2.10.5	I3C Basic Target Protocol	49
2.10.5.1	Write Operation - Data Packet	50
2.10.5.2	Read Operation - Data Packet	52
2.10.5.3	Default Read Address Pointer Mode	56
2.10.6	In Band Interrupt (IBI)	62
2.10.6.1	Enabling and Disabling In Band Interrupt Function	62
2.10.6.2	Mechanics of Interrupt Generation	63
2.10.6.3	Interrupt Arbitration	65
2.10.6.4	Clearing Device Status and IBI Status Registers	66
2.10.7	Packet Error Check (PEC) Function	67
2.10.8	Parity Error Check Function	67
2.10.9	Packet Error Check and Parity Error Handling	67
2.10.9.1	Write Command Data Packet Error Handling - PEC Disabled	67
2.10.9.2	Read Command Data Packet Error Handling - PEC Disabled	68
2.10.9.3	Write Command Data Packet Error Handling - PEC Is Enabled	69
2.10.9.4	Read Command Data Packet Error Handling - PEC Is Enabled	70
2.10.10	CCC Packet Error Handling	72
2.10.11	Error Reporting	72
2.10.12	I3C Basic Common Command Codes (CCC)	72
2.10.12.1	ENEC CCC	73
2.10.12.2	DISEC CCC	75
2.10.12.3	RSTDAA CCC	76

Contents (cont'd)

2.10.12.4	SETAASA CCC	77
2.10.12.5	GETSTATUS CCC	77
2.10.12.6	DEVCAP CCC	79
2.10.12.7	SETHID CCC	80
2.10.12.8	DEVCTRL CCC	80
2.10.13	IO Operation	87
2.10.14	Bus Clear	88
2.10.15	Bus Reset	89
2.10.16	Command Truth Table	90
2.11	Device Package and Pinout	91
2.11.1	Package Pinout	91
2.11.2	PMIC Package Pin List	93
2.11.3	Package Mechanical Drawing	95
2.12	Inductor Specification	99
2.12.1	Mechanical Specification	99
2.12.2	Electrical Specification	100
2.13	Application Notes	100
2.13.1	Method to Identify and Map Out DIMM with a PMIC Fault in Shared CAMP Topology	100
3	Registers Space.....	102
3.1	Register Attribute Definition	102
3.2	Register Map Breakdown	103
3.3	Register Memory Protection	103
3.3.1	Steps to Access DIMM Vendor Region Registers	103
3.3.2	Steps to Change DIMM Vendor Region Password	104
3.3.3	Steps to Burn or Program DIMM Vendor Region Registers	104
3.3.4	Host Region Register Map	105
3.3.5	Host Region Registers	110
3.3.5.1	Status Registers	110
3.3.5.2	Clear Registers	123
3.3.5.3	Mask Registers	128
3.3.5.4	Threshold and Configuration Registers	134
3.3.6	DIMM Vendor Region Registers	166
Annex A	(Informative) - Differences between Revisions	191
A.1	Differences between JESD301-1A and JESD301-1 (June 2020)	191
A.2	Differences between JESD301-1A.01 and JESD301-1A (August 2021)	193
A.3	Differences between JESD301-1A.02 and JESD301-1A.01 (October 2022)	193

Contents (cont'd)

List of Figures

Figure 1 — I2C or I3C Basic Bus AC Input Timing Parameter Definition	14
Figure 2 — I3C Basic Bus AC Data Output Timing Parameter Definition	15
Figure 3 — I2C Bus AC Data Output Timing Parameter Definition	15
Figure 4 — Output Slew Rate and Output Timing Reference Load	15
Figure 5 — Output Slew Rate Measurement Points	16
Figure 6 — Rise and Fall Timing Parameter Definition	16
Figure 7 — AC Measurement Waveform	17
Figure 8 — Impulse Waveform for EOS Test (IEC 61000-4-5)	19
Figure 9 — Dual Phase Regulator Example Schematic	20
Figure 10 — Single Phase Regulator Example Schematic	21
Figure 11 — PMIC Power Up Sequence; VIN_Mgmt Followed by VIN_Bulk	25
Figure 12 — PMIC Power Up Sequence; VIN_Bulk Followed by VIN_Mgmt	26
Figure 13 — VIN_Mgmt Input Supply to VIN_Bulk Input Supply Switchover Function	27
Figure 14 — VIN_Bulk Transition	28
Figure 15 — PMIC Power On Timing	29
Figure 16 — PMIC Power Off Timing Due to Internal Fault Condition	31
Figure 17 — High Level State Transitions	34
Figure 18 — Target Open Drain to Controller Push Pull Hand Off Operation	58
Figure 19 — Controller Open Drain (ACK) to Target Push Pull Hand Off Operation	59
Figure 20 — Controller Push Pull to Target Open Drain Hand Off Operation	60
Figure 21 — T=1; Controller Ends Read with Repeated START and STOP Waveform	61
Figure 22 — T=0; Target Ends Read; Controller Generates STOP	62
Figure 23 — PMIC Requests Interrupt, Host Ack Followed by PMIC Device IBI Payload	64
Figure 24 — PMIC Requests Interrupt; Host NACK Followed by STOP	64
Figure 25 — I2C or I3C Basic Bus Reset - PMIC Device	89
Figure 26 — PMIC Pinout - TOP View	91
Figure 27 — PMIC Pinout - BOTTOM View	92
Figure 28 — Package Mechanical Outline	95
Figure 29 — Detail A Drawing	96
Figure 30 — Detail B Drawing	97
Figure 31 — Reference PCB Land Pattern	98
Figure 32 — Reference Drawing and Recommended Land Pattern	99
Figure 33 — Error Log (R05 to R07) Registers Behavior with Power Cycle	111

List of Tables

Table 1 — PMIC Device Type Summary	2
Table 2 — Input Supply DC + AC Specification	3
Table 3 — SWA, SWB1 - Single Phase Regulator; PMIC5000; DC + AC Specification	4
Table 4 — SWA + SWB1 - Dual Phase Regulator; PMIC5000; DC + AC Specification	5
Table 5 — SWA, SWB1 - Single Phase Regulator; PMIC5010; DC + AC Specification	5

Contents (cont'd)

Table 6 — SWA + SWB1 - Dual Phase Regulator; PMIC5010; DC + AC Specification	6
Table 7 — SWC1 - Single Phase Regulator; PMIC5000; DC + AC Specification	6
Table 8 — SWC1 - Single Phase Regulator; PMIC5010; DC + AC Specification	7
Table 9 — SWD1 - Single Phase Regulator; PMIC5000; DC + AC Specification	7
Table 10 — SWD1 - Single Phase Regulator; PMIC5010; DC + AC Specification	8
Table 11 — Efficiency Characteristics; PMIC5000	9
Table 12 — Efficiency Characteristics; PMIC5010	9
Table 13 — LDO Output Regulator DC + AC Specification	10
Table 14 — PMIC AC Timing Parameters	11
Table 15 — I2C, I3C, and Interface DC Electrical Specification	12
Table 16 — Input Capacitance Spec	12
Table 17 — Input Spike Filter Spec	12
Table 18 — Output Ron	12
Table 19 — I2C and I3C Interface AC Characteristics	13
Table 20 — AC Measurement Conditions1	17
Table 21 — Thermal Characteristics	17
Table 22 — Absolute Maximum Rating	18
Table 23 — ESD Requirement	18
Table 24 — EOS Requirement	18
Table 25 — Input Source Condition	19
Table 26 — PMIC Schematic Values	22
Table 27 — Events Interrupt Summary	35
Table 28 — PMIC Response for Clear Command by Host - 1	36
Table 29 — PMIC Response for Clear Command by Host - 2	37
Table 30 — PMIC ID	45
Table 31 — 7-bit Address of PMIC Device	47
Table 32 — Write Command Data Packet	48
Table 33 — Read Command Data Packet	48
Table 34 — Read Command Data Packet with Default Address Pointer Mode	49
Table 35 — Write Command Data Packet; PEC Disabled	50
Table 36 — Write Command Data Packet; PEC Enabled	50
Table 37 — Write Command Data Packet with IBI Header; No Pending IBI, PEC Disabled	51
Table 38 — Write Command Data Packet with IBI Header; No Pending IBI, PEC Enabled	51
Table 39 — Read Command Data Packet; PEC Disabled	52
Table 40 — Read Command Data Packet; PEC Enabled	53
Table 41 — Read Command Data Packet with IBI Header; No Pending IBI, PEC Disabled	54
Table 42 — Read Command Data Packet with IBI Header; No Pending IBI, PEC Enabled	55
Table 43 — Read Command Data Packet with Read Address Pointer Mode; PEC Disabled	56
Table 44 — Read Command Data Packet with Read Address Pointer Mode; PEC Enabled	56
Table 45 — Read Command Data Packet with Read Address Pointer and IBI Header; No Pending IBI; PEC Disabled	57
Table 46 — Read Command Data Packet with Read Address Pointer and IBI Header; No Pending IBI; PEC Enabled	57

Contents (cont'd)

Table 47 — Target Device IBI Payload Packet; PEC is Disabled	63
Table 48 — Target Device IBI Payload Packet; PEC is Enabled	64
Table 49 — Interrupt Arbitration - Among All Devices	65
Table 50 — Write Command Data Packet; PEC Disabled	68
Table 51 — Read Command Data Packet; PEC Disabled	69
Table 52 — Write Command Data Packet; PEC Enabled	70
Table 53 — Read Command Data Packet; PEC Enabled	71
Table 54 — PMIC CCC Support Requirement	73
Table 55 — ENEC CCC - Broadcast	73
Table 56 — ENEC CCC - Broadcast with PEC	74
Table 57 — ENEC CCC - Direct	74
Table 58 — ENEC CCC - Direct with PEC	74
Table 59 — ENEC CCC Byte Encoding	75
Table 60 — DISEC CCC - Broadcast	75
Table 61 — DISEC CCC - Broadcast with PEC	75
Table 62 — DISEC CCC - Direct	76
Table 63 — DISEC CCC - Direct with PEC	76
Table 64 — DISEC CCC Byte Encoding	76
Table 65 — RSTDAA CCC - Broadcast	77
Table 66 — RSTDAA CCC - Broadcast with PEC	77
Table 67 — SETAASA CCC - Broadcast	77
Table 68 — GETSTATUS CCC - Direct	78
Table 69 — GETSTATUS CCC - Direct with PEC	78
Table 70 — GETSTATUS CCC Byte Encoding	78
Table 71 — DEVCAP CCC - Direct	79
Table 72 — DEVCAP CCC - Direct with PEC	79
Table 73 — DEVCAP CCC Byte Encoding	80
Table 74 — SETHID CCC - Broadcast	80
Table 75 — DEVCTRL CCC - Broadcast	81
Table 76 — DEVCTRL CCC - Broadcast with PEC1	82
Table 77 — DEVCTRL CCC Command Definition	83
Table 78 — DEVCTRL CCC Data Payload Definition	84
Table 79 — DEVCTRL CCC Example - Multicast Command to '1001' and '0110' Devices	85
Table 80 — DEVCTRL CCC Example - Broadcast Command to all Devices	85
Table 81 — DEVCTRL CCC Example - Unicast Command to PMIC on DIMM5	86
Table 82 — DEVCTRL CCC Example - Multicast Command to '0010' and '1001' Devices	86
Table 83 — DEVCTRL CCC Example - Multicast Command to '1001' Devices	87
Table 84 — PMIC Device Dynamic IO Operation Mode Switching	88
Table 85 — For I3C Mode Only with PEC Enabled - Command Truth Table	90
Table 86 — PMIC Pin Description	93
Table 87 — Inductor Mechanical Specification	99
Table 88 — Inductor Electrical Specification1	100
Table 89 — Register Base Attributes	102

Contents (cont'd)

Table 90 — Register Attribute Modifier	102
Table 91 — Register Map Breakdown	103
Table 92 — Register Color Coding Scheme	105
Table 93 — Host Region - Register Map	105
Table 94 — Register 0x04	112
Table 95 — Register 0x05	113
Table 96 — Register 0x06	114
Table 97 — Register 0x07	115
Table 98 — Register 0x08	116
Table 99 — Register 0x09	117
Table 100 — Register 0x0A	118
Table 101 — Register 0x0B	119
Table 102 — Register 0x0C	120
Table 103 — Register 0x0D	121
Table 104 — Register 0x0E	122
Table 105 — Register 0x0F	123
Table 106 — Register 0x10	124
Table 107 — Register 0x11	125
Table 108 — Register 0x12	126
Table 109 — Register 0x13	127
Table 110 — Register 0x14	128
Table 111 — Register 0x15	129
Table 112 — Register 0x16	130
Table 113 — Register 0x17	131
Table 114 — Register 0x18	132
Table 115 — Register 0x19	133
Table 116 — Register 0x1A	134
Table 117 — Register 0x1B	135
Table 118 — Register 0x1C	136
Table 119 — Register 0x1D	137
Table 120 — Register 0x1E	138
Table 121 — Register 0x1F	139
Table 122 — Register 0x20	140
Table 123 — Register 0x21	142
Table 124 — Register 0x22	143
Table 125 — Register 0x23	144
Table 126 — Register 0x24	145
Table 127 — Register 0x25	146
Table 128 — Register 0x26	147
Table 129 — Register 0x27	148
Table 130 — Register 0x28	149
Table 131 — Register 0x29	150
Table 132 — Register 0x2A	151

Contents (cont'd)

Table 133 — Register 0x2B	152
Table 134 — Register 0x2C	153
Table 135 — Register 0x2D	154
Table 136 — Register 0x2E	154
Table 137 — Register 0x2F	155
Table 138 — Register 0x30	157
Table 139 — Register 0x31	158
Table 140 — Register 0x32	159
Table 141 — Register 0x33	160
Table 142 — Register 0x34	161
Table 143 — Register 0x35	162
Table 144 — Register 0x37	163
Table 145 — Register 0x38	163
Table 146 — Register 0x39	163
Table 147 — Register 0x3A	164
Table 148 — Register 0x3B	165
Table 149 — Register 0x3C	165
Table 150 — Register 0x3D	165
Table 151 — DIMM Vendor Region - Register Map	166
Table 152 — Register 0x40	168
Table 153 — Register 0x41	169
Table 154 — Register 0x42	170
Table 155 — Register 0x43	171
Table 156 — Register 0x45	172
Table 157 — Register 0x46	173
Table 158 — Register 0x47	174
Table 159 — Register 0x48	175
Table 160 — Register 0x49	176
Table 161 — Register 0x4A	177
Table 162 — Register 0x4B	178
Table 163 — Register 0x4C	179
Table 164 — Register 0x4D	180
Table 165 — Register 0x4E	181
Table 166 — Register 0x4F	182
Table 167 — Register 0x50	183
Table 168 — Register 0x51	185
Table 169 — Register 0x58	186
Table 170 — Register 0x59	187
Table 171 — Register 0x5A	188
Table 172 — Register 0x5B	189
Table 173 — Register 0x5D	190
Table 174 — Register 0x5E	190

DEFINITION of PMIC5000, PMIC5010 VOLTAGE REGULATOR DEVICE for MEMORY MODULE APPLICATIONS

From JEDEC Board Ballot JCB-22-06, formulated under the cognizance of the JC-40.1 Subcommittee on Digital Logic Families and Applications, item 325.29D.

1 Scope

This standard defines the specifications of interface parameters, signaling protocols, and features for PMIC device as used for memory module applications. The designation PMIC5000, PMIC5010 refers to the device specified by this document.

The purpose is to provide a standard for the PMIC5000, PMIC5010 device for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

Unless otherwise noted in the document, any illegal operation is not allowed and device operation is not guaranteed.

NOTE: The designation PMIC5000, PMIC5010 refers to a portion of the part number designation of a series of commercial logic devices common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

The PMIC5000 and PMIC5010 is designed for typical DDR5 RDIMM, DDR5 LRDIMM as well as various types of DDR5 NVDIMM application. The PMIC features four step down switching regulators and three LDO regulators.

The PMIC is designed to support approximately 15 Watts of power. The PMIC is powered from VIN_Bulk input for switching regulators and VIN_Mgmt input for the rest of the PMIC. The PMIC supports selectable interface (I²C or I3C Basic) to fit various application environment. The PMIC device is intended to operate up to 12.5 MHz on a 1.0 V I3C Basic bus or up to 1 MHz on a 1.0 V to 3.3 V I²C bus.

2.1.1 Common Features Summary

Table 1 — PMIC Device Type Summary

Device Type	SWA	SWB	SWC	SWD	Unit
PMIC5000 - Current Capability per Phase	5	5	5	5	A
PMIC5010 - Current Capability per Phase	3	3	3	3	A

- VIN_Bulk input supply range: 4.25 V to 15.0 V
- VIN_Mgmt input supply range: 3.0 V to 3.6 V
- Four step down switching regulators: SWA, SWB, SWC and SWD
- Programmable dual phase and single phase regulator for SWA and SWB
- 3 LDO regulators: VBias, VOUT_1.8V, VOUT_1.0V
- Automatic switchover from VIN_Mgmt input supply to VIN_Bulk input supply
- Error injection capability
- Persistent Error log registers
- Write protect mode and programmable of operation
- Independently programmable output voltages, power up and power down sequence for switch regulators
- Input and output power good status reporting mechanism
- VIN_Bulk input supply protection feature: Input over voltage
- Output switch regulators protection feature: Output over voltage, output under voltage, output current limiter
- Output current and power measurement, output current threshold mechanism
- Temperature measurement, temperature warning threshold, critical temperature shutdown
- Multi Time Programmable Non-Volatile Memory
- Programmable and DIMM specific registers for customization
- General Status Interrupt Function
- Flexible Open Drain IO (I²C) and Push Pull (I3C Basic) IO Support

2.2 Input Supply and Output Regulator Electrical Characteristics

2.2.1 Input Supply Electrical Characteristics

Table 2 — Input Supply DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Bulk Input Supply Voltage DC Voltage	VIN_Bulk	4.25	12	15	V	1,2
Bulk Input Supply Maximum AC Voltage	VIN_Bulk_AC	-	-	18	V	
Bulk Input Supply Maximum Voltage Start up Overshoot	VIN_Bulk_OS_Startup	-	-	33	V*μs	3
Bulk Input Supply Voltage Ramp Up Rate	VIN_Bulk_Ramp_Up	0.1	-	3.0	V/ms	4
Bulk Input Supply Voltage Ramp Down Rate	VIN_Bulk_Ramp_Down	-	-	1.0	V/ms	5
Management Input Supply Voltage	VIN_Mgmt	3.0	3.3	3.6	V	6
Management Input Supply Ramp Up and Down Rate	VIN_Mgmt_Ramp	0.15		3	V/ms	
Minimum Management Input Supply Current	I _{VIN_Mgmt}	110	-	-	mA	7
Bulk Input Supply Current	I _{VIN_Bulk}		-	2.5	A	8
NOTE 1 During first power on, the input voltage supply must reach minimum value based on default from register Table 116, "Register 0x1A" [7:5] + 1.0V for PMIC to detect valid input supply.						
NOTE 2 The PMIC efficiency is optimized for nominal input supply of 12 V or lower. The PMIC efficiency above 13.8 V is degraded and thermal impact must be considered. The PMIC operation above 14.2V should not be greater than 20% duty cycle at any time and should be limited to a maximum contiguous period of 10 minutes.						
NOTE 3 The area under the curve above VIN_Bulk = 15V. VIN_Bulk_AC spec must also be satisfied.						
NOTE 4 The ramp up rate between 300 mV and 8.0 V.						
NOTE 5 The ramp down rate between 8.0 V and 300 mV.						
NOTE 6 During first power on, the input voltage supply must reach minimum value of 2.8 V for PMIC to detect valid input supply.						
NOTE 7 This is a platform spec. The minimum input current delivered by the platform through the DIMM gold finger to deliver the maximum load on LDO outputs (1.8V LDO output + 1.0V LDO output = 25 mA + 20 mA) plus the current required by the PMIC for its own usage.						
NOTE 8 This is a platform spec. The maximum input current delivered by the platform through the DIMM gold finger.						

2.2.2 Switch Regulator Output Electrical Characteristics

Table 3 — SWA, SWB¹ - Single Phase Regulator; PMIC5000; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	V _{out}		1.1		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	5	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	6	A	4
Maximum Load Transient	dI/dt	-	-	5	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5%		2.5%		5
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75%		0.75%		6
NOTE 1 Only applicable if Table 166, “Register 0x4F” [0] = ‘0’.						
NOTE 2 Typical voltage configured in the register Table 123, “Register 0x21” [7:1] for SWA and Table 125, “Register 0x23” [7:1] for SWB.						
NOTE 3 Measured over long period of time. Typically 1 second.						
NOTE 4 Measured over short period of time. Typically ≥ 20 μs but less than 50 μs.						
NOTE 5 The percentage applies to typical voltage configured in the register. Applies across entire PMIC operating temperature range. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, “Input Supply DC + AC Specification”. The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV.						
NOTE 6 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I _{tdc} = 0 A.						

2.2.2 Switch Regulator Output Electrical Characteristics (cont'd)

Table 4 — SWA + SWB¹ - Dual Phase Regulator; PMIC5000; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	Vout		1.1		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	10	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	12	A	4
Maximum Load Transient	dI/dt	-	-	10	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5%		2.5%		5
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75%		0.75%		6
NOTE 1 Only applicable if Table 166, "Register 0x4F" [0], = '1'. NOTE 2 Typical voltage configured in the register Table 123, "Register 0x21" [7:1]. NOTE 3 Measured over long period of time. Typically 1 second. NOTE 4 Measured over short period of time. Typically ≥ 20 μs but less than 50 μs. NOTE 5 The percentage applies to typical voltage configured in the register. Applies across entire PMIC operating temperature range. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, "Input Supply DC + AC Specification". The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV. NOTE 6 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I_{tdc} = 0 A.						

Table 5 — SWA, SWB¹ - Single Phase Regulator; PMIC5010; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	Vout		1.1		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	3	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	3.5	A	4
Maximum Load Transient	dI/dt	-	-	5	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5%		2.5%		5
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75%		0.75%		6
NOTE 1 Only applicable if Table 166, "Register 0x4F" [0], = '1'. NOTE 2 Typical voltage configured in the register Table 123, "Register 0x21" [7:1] for SWA and Table 125, "Register 0x23" [7:1] for SWB. NOTE 3 Measured over long period of time. Typically 1 second. NOTE 4 Measured over short period of time. Typically ≥ 20 μs but less than 50 μs. NOTE 5 The percentage applies to typical voltage configured in the register. Applies across entire PMIC operating temperature range. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, "Input Supply DC + AC Specification". The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV. NOTE 6 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I_{tdc} = 0 A.						

2.2.2 Switch Regulator Output Electrical Characteristics (cont'd)

Table 6 — SWA + SWB¹ - Dual Phase Regulator; PMIC5010; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	V _{out}		1.1		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	6	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	7	A	4
Maximum Load Transient	dI/dt	-	-	10	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5%		2.5%		5
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75%		0.75%		6
NOTE 1 Only applicable if Table 166, “Register 0x4F” [0], = ‘1’. NOTE 2 Typical voltage configured in the register Table 123, “Register 0x21” [7:1]. NOTE 3 Measured over long period of time. Typically 1 second. NOTE 4 Measured over short period of time. Typically ≥ 20 μs but less than 50 μs. NOTE 5 The percentage applies to typical voltage configured in the register. Applies across entire PMIC operating temperature range. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, “Input Supply DC + AC Specification”. The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV. NOTE 6 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I_{tdc} = 0 A.						

Table 7 — SWC¹ - Single Phase Regulator; PMIC5000; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	V _{out}		1.1		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	5	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	6	A	4
Maximum Load Transient	dI/dt	-	-	5	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5%		2.5%		5
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75%		0.75%		6
NOTE 1 There is no note. This is intentional. NOTE 2 Typical voltage configured in the register Table 127, “Register 0x25” [7:1]. NOTE 3 Measured over long period of time. Typically 1 second. NOTE 4 Measured over short period of time. Typically ≥ 20 μs but less than 50 μs. NOTE 5 The percentage applies to typical voltage configured in the register. Applies across entire PMIC operating temperature range. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, “Input Supply DC + AC Specification”. The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV. NOTE 6 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I_{tdc} = 0 A.						

2.2.2 Switch Regulator Output Electrical Characteristics (cont'd)

Table 8 — SWC¹ - Single Phase Regulator; PMIC5010; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	V _{out}		1.1		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	3	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	3.5	A	4
Maximum Load Transient	dI/dt	-	-	5	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5%		2.5%		5
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75%		0.75%		6
NOTE 1 There is no note. This is intentional. NOTE 2 Typical voltage configured in the register Table 127, "Register 0x25" [7:1]. NOTE 3 Measured over long period of time. Typically 1 second. NOTE 4 Measured over short period of time. Typically ≥ 20 μs but less than 50 μs. NOTE 5 The percentage applies to typical voltage configured in the register. Applies across entire PMIC operating temperature range. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, "Input Supply DC + AC Specification". The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV. NOTE 6 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I_{tdc} = 0 A.						

Table 9 — SWD¹ - Single Phase Regulator; PMIC5000; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	V _{out}		1.8		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	5	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	6	A	4
Maximum Load Transient	dI/dt	-	-	5	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5%		2.5%		5
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75%		0.75%		6
NOTE 1 There is no note. This is intentional. NOTE 2 Typical voltage configured in the register Table 129, "Register 0x27" [7:1]. NOTE 3 Measured over long period of time. Typically 1 second. NOTE 4 Measured over short period of time. Typically ≥ 20 μs but less than 50 μs. NOTE 5 The percentage applies to typical voltage configured in the register. Applies across entire PMIC operating temperature range. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, "Input Supply DC + AC Specification". The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV. NOTE 6 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I_{tdc} = 0 A.						

2.2.2 Switch Regulator Output Electrical Characteristics (cont'd)

Table 10 — SWD¹ - Single Phase Regulator; PMIC5010; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	V _{out}		1.8		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	3	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	3.5	A	4
Maximum Load Transient	dI/dt	-	-	5	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5%		2.5%		5
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75%		0.75%		6
NOTE 1 There is no note. This is intentional. NOTE 2 Typical voltage configured in the register Table 129, "Register 0x27" [7:1]. NOTE 3 Measured over long period of time. Typically 1 second. NOTE 4 Measured over short period of time. Typically ≥ 20 μs but less than 50 μs. NOTE 5 The percentage applies to typical voltage configured in the register. Applies across entire PMIC operating temperature range. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, "Input Supply DC + AC Specification". The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV. NOTE 6 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 12.0 V. The regulator output current load I_{tdc} = 0 A.						

2.2.3 Switch Regulator Efficiency

Table 11 — Efficiency Characteristics; PMIC5000

Switch Node Output	Efficiency (% of Max I _{tdc} Load)			Unit	Notes
	25%	50%	100%		
SWA or SWB (Single Phase Regulator Mode)	≥ 87	≥ 92	≥ 89	%	1,2,3,4,5, 6,7,8,9,10
SWA + SWB (Dual Phase Regulator Mode)	≥ 87	≥ 92	≥ 89	%	
SWC	≥ 87	≥ 92	≥ 89	%	
SWD	≥ 87	≥ 92	≥ 89	%	
NOTE 1	VIN_Bulk = 12 V; VIN_Mgmt = 3.3 V				
NOTE 2	The maximum I _{tdc} as specified in appropriate Tables above.				
NOTE 3	When the efficiency of any given output regulator is being measured, all other switching output regulators are disabled.				
NOTE 4	No external load on VOUT_1.8V, VOUT_1.0V LDO is applied.				
NOTE 5	I ² C/I ³ C Basic bus is pulled High and held static. CAMP and GSI_n signals are pulled High and held static.				
NOTE 6	The efficiency includes the buck regulator loss, the PCB loss (≤ 2.5 mΩ) and see clause 2.12 for inductor specification assumption for DCR and ACR.				
NOTE 7	Efficiency calculation equation: (V _{OUT} * I _{OUT}) / [(V _{IN_Bulk} * I _{VIN_Bulk}) + (V _{IN_Mgmt} * I _{IN_Mgmt}); where V _{OUT} , I _{OUT} , V _{IN_Mgmt} , I _{IN_Mgmt} , V _{IN_Bulk} , I _{VIN_Bulk} parameters are actual measured values.				
NOTE 8	Applies at maximum ambient temperature of 65 °C (PMIC Junction temperature of 105 °C). The inductor characteristics noted above applies inductor temperature of 105 °C.				
NOTE 9	The output buck regulator switching frequency can be set to anywhere within 500 KHz to 1000 KHz. For all efficiency qualification testing, the device under test (DUT) must also comply with all PMIC’s electrical characteristics (DC+AC) specifications.				
NOTE 10	For input supply rails, probing is done at the input high frequency filter cap (0.1uF) to PMIC pin. For output rail, probing is done at the output cap location at the inductor load side.				

Table 12 — Efficiency Characteristics; PMIC5010

Switch Node Output	Efficiency (% of Max I _{tdc} Load)			Unit	Notes
	25%	50%	100%		
SWA or SWB (Single Phase Regulator Mode)	≥ 85	≥ 90	≥ 87	%	1,2,3,4,5, 6,7,8,9,10
SWA + SWB (Dual Phase Regulator Mode)	≥ 85	≥ 90	≥ 87	%	
SWC	≥ 85	≥ 90	≥ 87	%	
SWD	≥ 85	≥ 90	≥ 87	%	
NOTE 1 VIN_Bulk = 12 V; VIN_Mgmt = 3.3 V					
NOTE 2 The maximum I _{tdc} as specified in appropriate Tables above.					
NOTE 3 When the efficiency of any given output regulator is being measured, all other switching output regulators are disabled.					
NOTE 4 No external load on VOUT_1.8 V, VOUT_1.0 V LDO is applied.					
NOTE 5 I ² C/I ³ C Basic bus is pulled High and held static. CAMP and GSI_n signals are pulled High and held static.					
NOTE 6 The efficiency includes the buck regulator loss, the PCB loss (≤ 2.5 mΩ) and see clause 2.12 for inductor specification.assumption for DCR and ACR.					
NOTE 7 Efficiency calculation equation: (V _{OUT} * I _{OUT}) / [(V _{IN_Bulk} * I _{VIN_Bulk}) + (V _{IN_Mgmt} * I _{IN_Mgmt})]; where V _{OUT} , I _{OUT} , V _{IN_Mgmt} , I _{IN_Mgmt} , V _{IN_Bulk} , I _{VIN_Bulk} parameters are actual measured values.					
NOTE 8 Applies at maximum ambient temperature of 65 °C (PMIC Junction temperature of 105 °C). The inductor characteristics noted above applies inductor temperature of 105 °C.					
NOTE 9 The output buck regulator switching frequency can be set to anywhere within 500 KHz to 1000 KHz. For all efficiency qualification testing, the device under test (DUT) must also comply with all PMIC’s electrical characteristics (DC+AC) specifications.					
NOTE 10 For input supply rails, probing is done at the input high frequency filter cap (0.1 uF) to PMIC pin. For output rail, probing is done at the output cap location at the inductor load side.					

2.2.4 LDO Output Regulator Characteristics

Table 13 — LDO Output Regulator DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1.8 V LDO Output Voltage	VOUT_1.8V		1.8		V	1
1.8 V LDO Output - Maximum Output Current	I _{tdc_VOUT_1.8V}	-	-	25	mA	2
1.0 V LDO Output Voltage	VOUT_1.0V		1.0		V	3
1.0 V LDO Output - Maximum Output Current	I _{tdc_VOUT_1.0V}	-	-	20	mA	4
NOTE 1	Typical voltage is configured in register Table 133, “Register 0x2B” [7:6]. The min and max values are guaranteed to be within ± 100 mV of programmed value.					
NOTE 2	The maximum output current represents the external load and excludes PMIC’s own internal current consumption. The specified maximum output current is only applicable after PMIC’s 1.8V LDO Power Good status is good (i.e., t1.8V_Ready timing parameter is satisfied). Prior to PMIC’s 1.8V LDO Power Good status (i.e., while PMIC is still ramping up the 1.8 V LDO, the maximum output current load shall be limited to maximum of 10 mA.					
NOTE 3	Typical voltage is configured in register Table 133, “Register 0x2B” [2:1]. The min and max values are guaranteed to be within ± 50 mV of programmed value.					
NOTE 4	The maximum output current represents the external load and excludes PMIC’s own internal current consumption. The specified maximum output current is only applicable after PMIC’s 1.0V LDO Power Good status is good (i.e., t1.0V_Ready timing parameter is satisfied). Prior to PMIC’s 1.0V LDO Power Good status (i.e., while PMIC is still ramping up the 1.0V LDO), the maximum output current load shall be limited to maximum of 5 mA.					

2.2.5 PMIC AC Timing Parameters

Table 14 — PMIC AC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Supply to GSI_n assertion	tInput_PWR_GOOD_GSI_Assertion			10	μs	
Input over voltage condition to GSI_n assertion	tInput_OV_GSI_Assertion	-	-	10	μs	
Input over voltage condition to automatic PMIC VR Disable	tInput_OV_VR_Disable	-	-	20	μs	
Output Voltage Tolerance to GSI_n assertion	tOutput_PWR_GOOD_GSI_Assertion	-	-	10	μs	
Output over voltage condition to automatic PMIC VR Disable	tOutput_OV_VR_Disable	-	-	20	μs	
Output under voltage lockout condition to automatic PMIC VR Disable	tOutput_UV_VR_Disable	-	-	20	μs	
Output current limiter Warning to GSI_n assertion	tOutput_Current_Limiter	-	-	10	μs	
High Temperature Warning to GSI_n assertion	tHigh_Temp_Warning	-	-	10	μs	
Critical Temperature condition to automatic PMIC shut down	tShut_Down_Temp	-	-	10	μs	
VIN_Mgmt input supply stable to VR Enable Command	tVIN_Mgmt_to_Enable	6.5	-	-	ms	
VIN_Bulk input supply stable to VR Enable Command	tVIN_Bulk_to_Enable	6.5	-	-	ms	
VIN_Mgmt input supply stable to VOUT_1.8V output stable	t1.8V_Ready	-	-	3.5	ms	
VOUT_1.8V output supply stable to VOUT_1.0V output stable	t1.0V_Ready	-	-	1.0	ms	1
VOUT_1.8V output supply to PMIC Management Ready	tManagement_Ready	-	-	3	ms	
VR Enable Command to PMIC output regulator ready	tPMIC_PWR_Good_Out	Figure 15			ms	
VR Disable Command to PMIC Output Regulators Off	tPMIC_Output_Off	Figure 16			ms	
CAMP Input Low Pulse Width	tCAMP_Low_Pulse_Width	2			μs	
CAMP Input Low Pulse Width Input Filter	tCAMP_Low_Pulse_Width_Filter	-	-	0.35	μs	
Output Voltage Adjustment in non write protect mode	Δv/Δt	-	1	-	mV/μs	2
NOTE 1 This time is added to t_1.8V_Ready parameter to get total time from VIN_Mgmt input supply.						
NOTE 2 See footnote 4 for registers Table 123, “Register 0x21” [7:1], Table 125, “Register 0x23” [7:1], Table 127, “Register 0x25” [7:1], and Table 129, “Register 0x27” [7:1]. The accuracy is ± 10%						

2.3 I²C, I3C Basic and Interface DC and AC Electrical Characteristics

Table 15 — I²C, I3C, and Interface DC Electrical Specification

Parameter	Symbol	Min	Max	Unit	Notes
Input Low Voltage (CAMP, SDA, SCL)	V _{IL}	-0.3	0.3	V	
Input High Voltage (SDA, SCL)	V _{IH}	0.7	3.6	V	
Input High Voltage (CAMP)	V _{IH}	1.26	3.6	V	
Output Low Voltage (SDA, GSI_n)	V _{OL}	-	0.3	V	1
Output High Voltage (SDA)	V _{OH}	0.75	-	V	
Output Low Current (SDA, GSI_n, CAMP)	I _{OL}	3	-	mA	
Output High Current (SDA)	I _{OH}	-	3	mA	
Output Low Voltage (CAMP)	V _{OL_CAMP}	-	0.3	V	2
Rising Output Slew Rate (SDA)	Slew_Rate	0.1	1	V/ns	3
Falling Output Slew Rate (SDA)		0.1	3	V/ns	
Input Leakage Current	I _{LI}	-	+5	μA	
Output Leakage Current	I _{LO}	-	+5	μA	
NOTE 1 The pullup resistor for GSI_n signal may vary and is typically 1K Ohm.					
NOTE 2 CAMP output is Open Drain output. There is an external pullup resistor to 3.3 V motherboard for standard DDR5 RDIMM/LRDIMM. For other DIMM environment, the external pullup resistor may be pulled to either 1.8 V or 2.5 V or 3.3 V on either on DIMM or on the motherboard.					
NOTE 3 Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load is shown in Figure 4 and Figure 5 shows the timing measurement points. For slew rate measurement, the V _{OH} level shown in Figure 5 is a function of R _{on} value; V _{OH} = {1.0/(R _{on} + 50)} * 50.					

Table 16 — Input Capacitance Spec

Parameter	Symbol	Min	Max	Unit	Notes
Input Capacitance (CAMP, SCL, SDA)	C _{IN}	-	5	pF	

Table 17 — Input Spike Filter Spec

Parameter	Symbol	Test Condition	Min	Max	Unit	Notes
Pulse width of spikes which must be suppressed by the input filter in I ² C mode	t _{SP}	Single glitch, f ≤ 100 KHz	-	-	ns	
		Single glitch, f > 100 KHz	0	50	ns	1
NOTE 1 T _A = 25 °C; f = 400 KHz. Verified by design and characterization only.						

Table 18 — Output Ron

Parameter	Symbol	Min	Max	Unit	Notes
SDA Output Pullup and Pulldown Driver Impedance	R _{ON}	20	100	Ω	1
GSI_n, CAMP Output Pulldown Driver Impedance		40	100	Ω	
NOTE 1 Pulldown Ron = Vout/Iout. Pullup Ron = (VOUT 1.0V - Vout)/Iout.					

2.3 I2C, I3C Basic and Interface DC and AC Electrical Characteristics (cont'd)

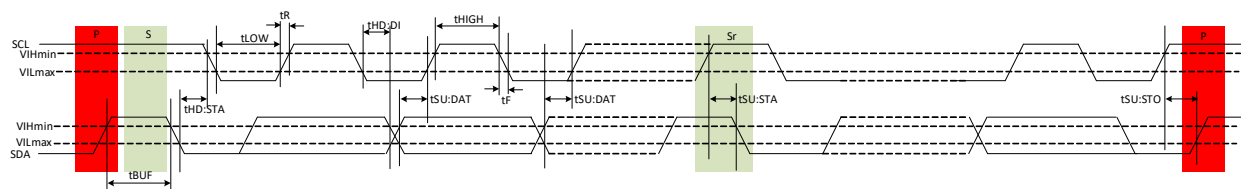
Table 19 — I²C and I3C Interface AC Characteristics

Parameter	Symbol	I ² C Mode - Open Drain		I3C Basic Mode Push-Pull ¹		Unit	Notes
		Min	Max	Min	Max		
Clock Frequency	f_{SCL}	0.01	1	0.01	12.5	MHz	
Clock High Pulse Width Time	t_{High}	260		35		ns	
Clock Low Pulse Width Time	t_{Low}	500		35		ns	
Detect Clock Input Low Time	$t_{TIMEOUT}$	10	50	10	50	ms	
Rise Time	t_R	-	120	-	5	ns	2,3
Fall time	t_F	-	120	0	5	ns	2,3
Data in Setup Time	$t_{SU:DAT}$	50	-	8	-	ns	2,4
Data in Hold Time	$t_{HD:DI}$	0	-	3	-	ns	2,4
Start Condition Setup Time	$t_{SU:STA}$	260	-	12	-	ns	2
Start Condition Hold Time	$t_{HD:STA}$	260	-	30	-	ns	2
Stop Condition Setup Time	$t_{SU:STO}$	260	-	12	-	ns	2
Time between Stop Condition and next Start Condition	t_{BUF}	500	-	500	-	ns	2,5
SDA Data Out Hold Time	$t_{HD:DAT}$	0.5	350	N/A	N/A	ns	6
SCL Falling Clock In to Valid SDA Data Out Time	t_{DOUT}	N/A	N/A	0.5	12	ns	7,8
SCL Rising Clock In to Target SDA Output Off	t_{DOFFT}	N/A	N/A	0.5	12	ns	7,8,9
SCL Rising Clock In to Controller SDA Output Off	t_{DOFFC}	N/A	N/A	0.5	30	ns	7,8,10
SCL Rising Clock In to Controller Driving Data Signal Low	$t_{CL_r_DAT_f}$	N/A	N/A	40	-	ns	11
Bus Available Time (no edges seen on SCL and SDA)	t_{AVAL}	N/A	N/A	1	-	μs	
Time to issue IBI after an event is detected when Bus is available	t_{IBI_ISSUE}	N/A	N/A	-	15	μs	
Time from Clear Register Status to any I3C Basic operation with Start condition to avoid false IBI generation; PEC disabled	$t_{CLR_I3C_CMD_Delay}$	N/A	N/A	4	-	μs	
Time from Clear Register Status to any I3C Basic operation with Start condition to avoid false IBI generation; PEC enabled		N/A	N/A	15	-	μs	
DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/Write Command Delay	$t_{DEVCTRLCCC_DELAY_PEC_DIS}$	3	-	3	-	μs	12,13,14

Table 19 — I²C and I3C Interface AC Characteristics (cont'd)

Parameter	Symbol	I ² C Mode - Open Drain		I3C Basic Mode Push-Pull ¹		Unit	Notes
		Min	Max	Min	Max		
Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode	$t_{WR_RD_DELAY_PEC_EN}$	N/A	N/A	8	-	μs	15,16,17
SETHID CCC or SETAASA CCC followed by any other CCC or Read/Write Command Delay	$t_{I2C_CCC_Update_Delay}$	2.5	-	-	-	μs	
RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command Delay	$t_{I3C_CCC_Update_Delay}$	-	-	2.5	-	μs	
Any CCC followed by RSTDAA CCC delay	t_{CCC_Delay}	N/A	N/A	2.5	-	μs	
NOTE 1 I3C mode with Open Drain operation follows timing values as shown in I²C Mode - Open Drain column. NOTE 2 See Figure 1 for PMIC's input timing definition. NOTE 3 See Figure 6 for voltage threshold definition for rise and fall times. NOTE 4 The input setup time is referenced from SDA VIL or VIH threshold as shown in Figure 1 to SCL VIH threshold as shown in Figure 1. The input hold time is referenced from SCL VIL threshold as shown in Figure 1 to SDA VIL or VIH threshold as shown in Figure 1. NOTE 5 If PEC is enabled, $t_{WR_RD_DELAY_PEC_EN}$ timing parameter applies. NOTE 6 The PMIC device guarantees $t_{HD:DAT}$ value in I²C mode of operation. See Figure 3 for PMIC's output timing definitions as well as SCL clock input threshold level and SDA data output threshold levels. NOTE 7 The PMIC device must be configured in I3C Basic mode to guarantee t_{DOUT} or t_{DOFFT} or t_{DOFFC} value. See Figure 2 for PMIC's output timing definition as well as SCL clock input threshold level and SDA data output threshold levels. NOTE 8 This timing parameter is guaranteed into output timing reference load as shown in Figure 4. NOTE 9 The PMIC device must be configured in I3C Basic mode to guarantee t_{DOFFT} value. See Figure 18. NOTE 10 The PMIC device must be configured in I3C Basic mode to guarantee t_{DOFFC} value. See Figure 19. NOTE 11 See Figure 21. NOTE 12 From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay. NOTE 13 The PMIC sends NACK if Host does not satisfy $t_{DEVCTRLCCC_DELAY_PEC_DIS}$ timing parameter. NOTE 14 This timing parameter restriction is only applicable when PEC function is disabled in PMIC. If PEC is enabled, this timing parameter does not apply. NOTE 15 From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay. NOTE 16 This timing parameter restriction is only applicable when PEC function is enabled in PMIC. If PEC is disabled, this timing parameter does not apply. NOTE 17 The PMIC sends NACK if Host does not satisfy $t_{WR_RD_DELAY_PEC_EN}$ timing parameter.							

The PMIC device follow the I²C or I3C Basic bus timing requirements. Figure 1, Figure 2, and Figure 3 show the timing diagram for Data bus Input and Data Output parameters.

Figure 1 — I²C or I3C Basic Bus AC Input Timing Parameter Definition

2.3 I2C, I3C Basic and Interface DC and AC Electrical Characteristics (cont'd)

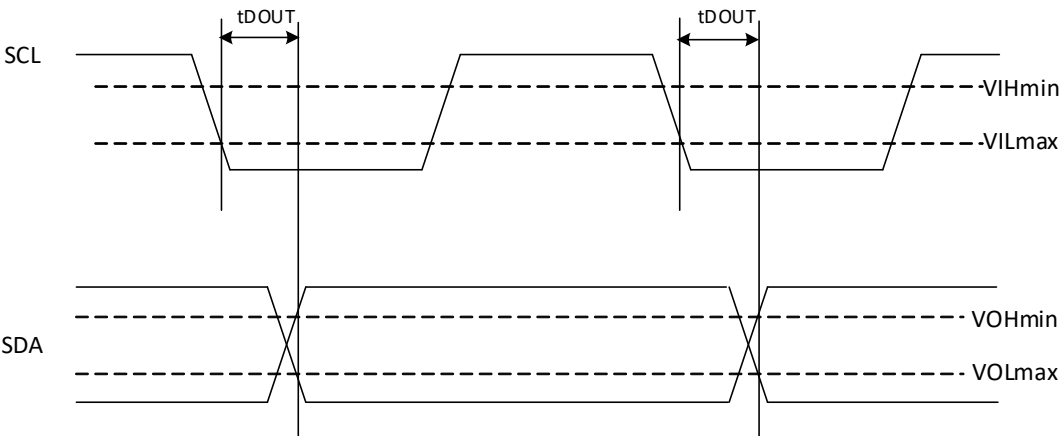


Figure 2 — I3C Basic Bus AC Data Output Timing Parameter Definition

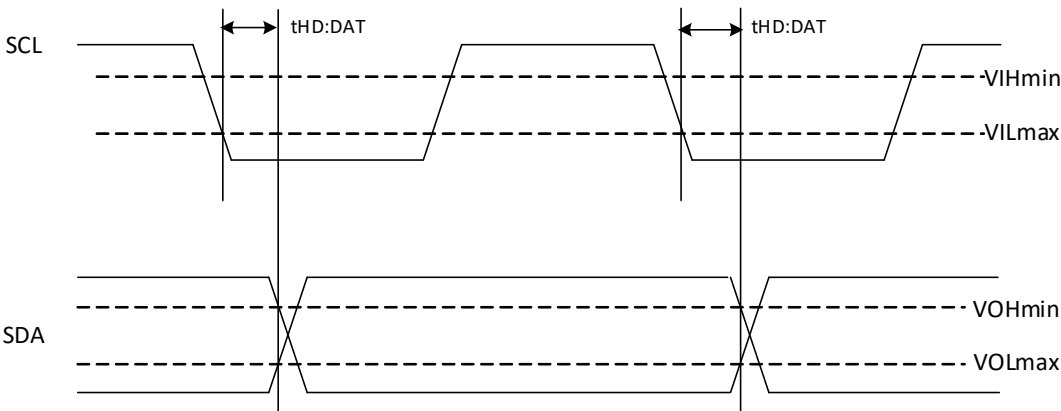


Figure 3 — I²C Bus AC Data Output Timing Parameter Definition

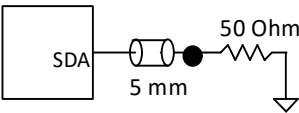


Figure 4 — Output Slew Rate and Output Timing Reference Load

2.3 I²C, I³C Basic and Interface DC and AC Electrical Characteristics (cont'd)

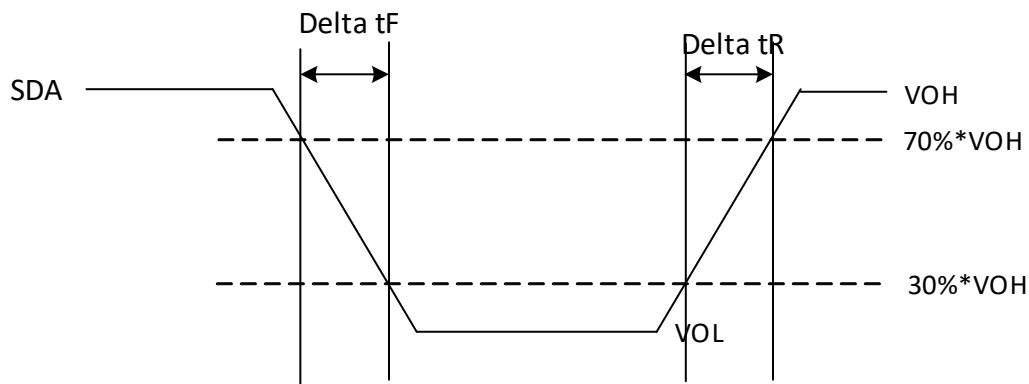


Figure 5 — Output Slew Rate Measurement Points

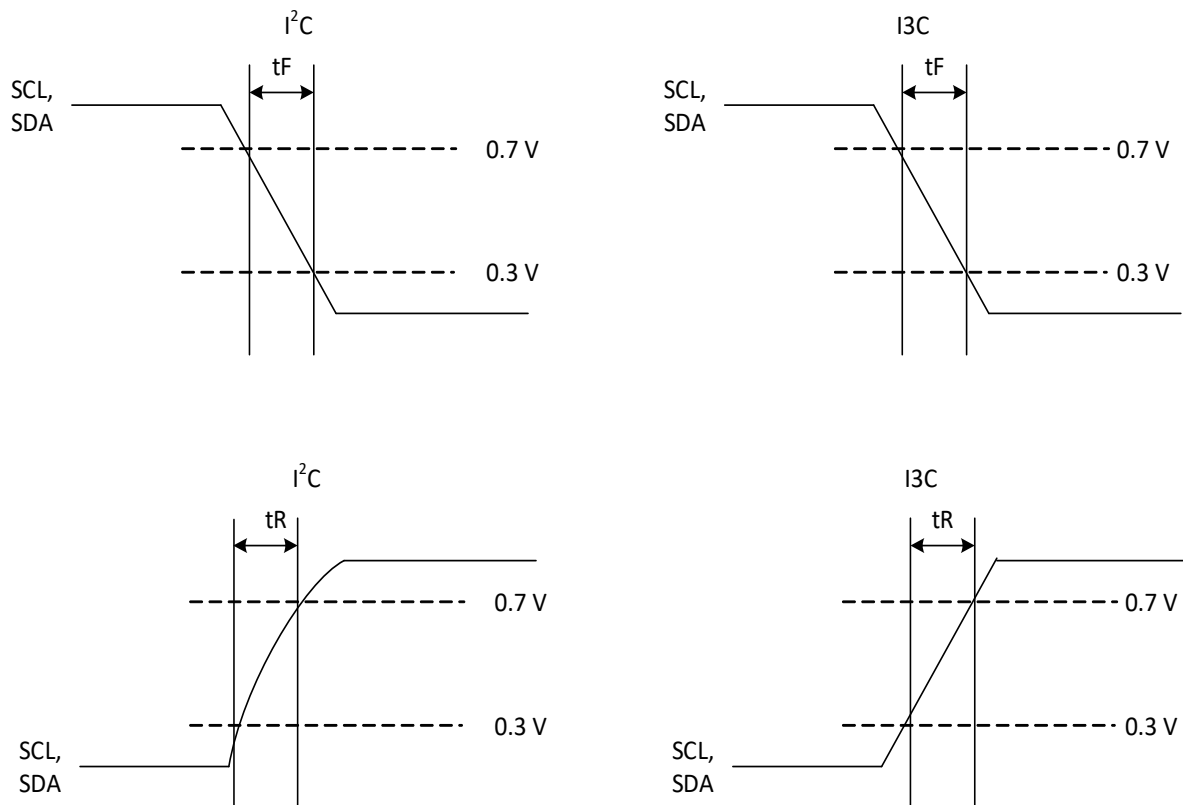


Figure 6 — Rise and Fall Timing Parameter Definition

2.3 I2C, I3C Basic and Interface DC and AC Electrical Characteristics (cont'd)

Table 20 — AC Measurement Conditions¹

Symbol	Parameter	Min	Max	Units
C _L	Load capacitance		40	pF
	Input rise and Fall times - Open Drain	-	TBD	ns
	Input rise and fall times - Push Pull	-	TBD	ns
	Input signal swing levels	0.2 to 0.8		V
	Input and Output timing reference levels	0.3 to 0.7		V
NOTE 1 This AC measurement condition (Table 20 and Figure 7) is only for the test purpose in lab.				

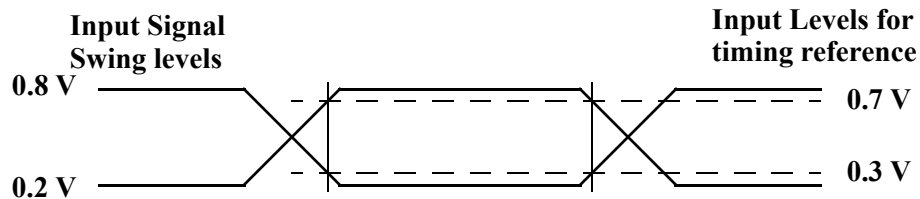


Figure 7 — AC Measurement Waveform

2.4 Thermal Characteristics

Table 21 — Thermal Characteristics

Parameter	Symbol	Maximum Rating	Unit	Notes
Thermal resistance junction to case	Θ_{JC}	TBD	$^{\circ}\text{C}/\text{W}$	1,2,3
Junction operating temperature	T_J	-10 to 125	$^{\circ}\text{C}$	
Case operating temperature	T_C	-10 to TBD	$^{\circ}\text{C}$	4
Storage temperature	T_{STG3}	-55 to 150	$^{\circ}\text{C}$	4
Lead temperature (soldering, 10s)	T_{LEAD}	300	$^{\circ}\text{C}$	4
NOTE 1 The maximum power dissipation is $P_{D(MAX)} = (T_{JMAX} - T_C) / \Theta_{JC}$. Exceeding the maximum allowable power dissipation results in excessive die temperature and the device will enter thermal shutdown.				
NOTE 2 This thermal rating was calculated on JEDEC 51 standard 4 layer board with dimensions 3" x 4.5" in still air conditions. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude and other unlisted variables.				
NOTE 3 This specification is compliant with JESD402-1 Temperature Grade and Measurement Specification for Components and Modules, operating temperature range MT, storage temperature T_{STG3} . See JESD402-1 for details, including measurement point.				
NOTE 4 Soldering temperature, 10 s.				

2.5 Absolute Maximum Rating

The absolute maximum ratings are stress ratings only. Stresses greater than those listed in Table 22, “Absolute Maximum Rating”, Table 23, “ESD Requirement”, and Table 24, “EOS Requirement” may cause permanent damage to the device. Functional operation of the PMIC at absolute maximum ratings is not implied. Exposure to absolute maximum rating condition for extended periods may affect long term reliability.

Table 22 — Absolute Maximum Rating

Pin	Maximum Rating		Unit
	DC	AC	
VIN_BULK	-0.3 to 16.2	TBD (Duration $\leq$ 25 ns)	V
VIN_Mgmt, VBIAS	-0.3 to 6.0	-	V
VOUT_1.8V, VOUT_1.0V	-0.3 to 2.2	-	V
SWA, SWB, SWC, SWD	-0.3 to 16.2	-4.5 to 20 (Duration < 25 ns)	V
SWA_BOOT, SWB_BOOT, SWC_BOOT, SWD_BOOT (to GND)	-0.3 to 21.0	-0.3 to 24 (Duration < 25 ns)	V
SWA_BOOT, SWB_BOOT, SWC_BOOT, SWD_BOOT (to SWx)	-0.3 to 6.0	TBD	V
SWAB_FB_P, SWB_FB_P, SWC_FB_P, SWD_FB_P (to AGND)	-0.3 to 2.2	-	V
SWAB_FB_N, SWC_FB_N, SWD_FB_N/PID	-0.3 to 2.2	-	V
CAMP ¹ , GSI_n	-0.3 to 5.0	-	V
SCL, SDA; I ² C Mode only	-0.3 to 5.0	TBD	V
SCL, SDA; I ³ C Mode only	-0.3 to 2.1	TBD	V
AGND, PGND	-0.3 to 0.3	-	V
NOTE 1 CAMP pins shall withstand the stress when connected to maximum of 15V DC source through 250 Ohm series resistor for 10 seconds.			

Table 23 — ESD Requirement

Test Model	Pin	Maximum Rating	Unit
HBM	All	$\pm$ 2000	V
CDM	All	$\pm$ 500	V

Table 24 — EOS Requirement

Pin	Maximum Rating	Unit	Notes
VIN_BULK	37	V	1,2,3,4
VIN_Mgmt	10	V	
NOTE 1	The test is performed on DDR5 DIMM module without any input capacitor on VIN_BULK and VIN_Mgmt		
NOTE 2	The input source needs to follow the waveform and condition as shown in Figure 8 and Table 25.		
NOTE 3	Probing is performed at the VIN_BULK and VIN_Mgmt pin of PMIC.		
NOTE 4	Each net test is performed individually.		

2.5 Absolute Maximum Rating (cont'd)

Table 25 — Input Source Condition

Item	Value	Notes
T (rise from 30% to 90% of peak)	0.72 μ s (+ 30%)	
T1 (rise time)	1.2 μ s (+ 30%)	T1 = 1.67*T
T2 (duration time to half value)	50 μ s (+ 20%)	
Output Impedance	2 Ω	
VUNDERSHOOT Voltage	30% Max	

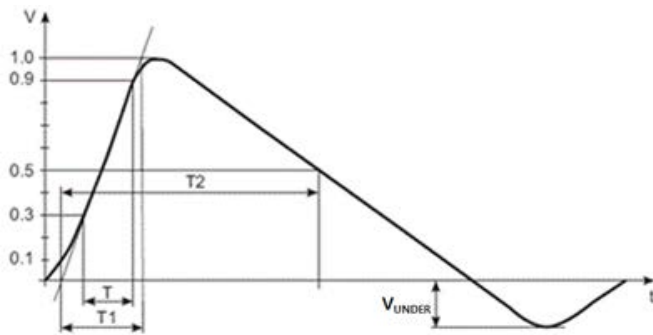


Figure 8 — Impulse Waveform for EOS Test (IEC 61000-4-5)

2.6 Example Schematic

Figure 9 shows an example schematic when PMIC is configured in dual phase regulator mode. Table 26, “PMIC Schematic Values” shows all component details shown in the schematics. Note that capacitors C25, C26, C27, C29, C30, and C31 represent the lump sum of distributed capacitance across the entire DIMM.

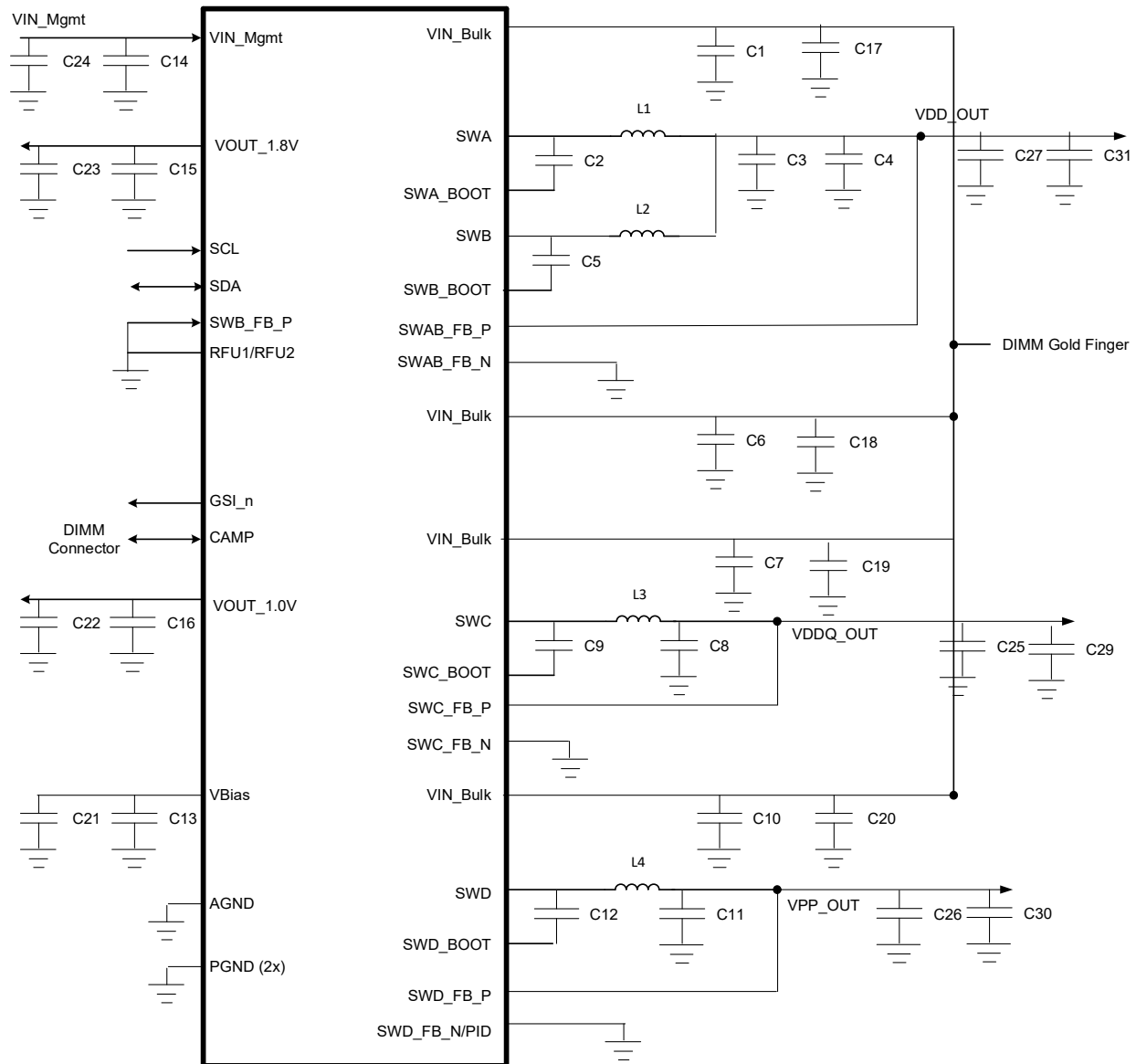


Figure 9 — Dual Phase Regulator Example Schematic

2.6 Example Schematic (cont'd)

Figure 10 shows an example schematic when PMIC is configured in single phase regulator mode. Table 26, “PMIC Schematic Values” shows all component details shown in the schematics. Note that capacitors C25, C26, C27, C28, C29, C30, C31, and C32 represent the lump sum of distributed capacitance across the entire DIMM.

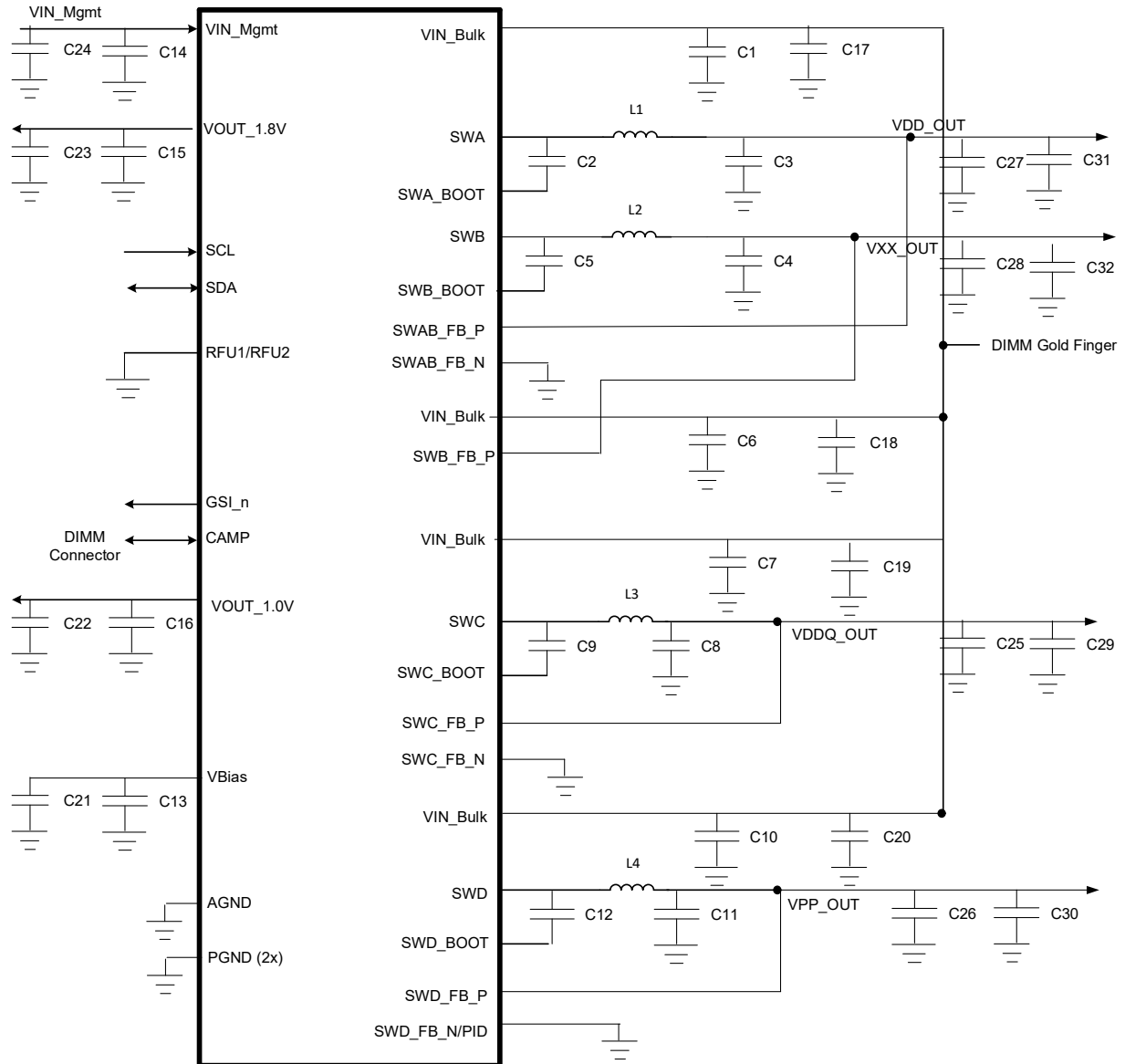


Figure 10 — Single Phase Regulator Example Schematic

2.6 Example Schematic (cont'd)

Table 26 — PMIC Schematic Values

Component	Dual Phase Regulator Mode		Single Phase Regulator Mode		Unit	Comment
	Value	Physical Size/Rating	Value	Physical Size/Rating		
L1	0.47 - 0.68	4.0 x 4.0 x 2.0	0.47 - 0.68	4.0 x 4.0 x 2.0	μH	
L2	0.47 - 0.68	4.0 x 4.0 x 2.0	0.47 - 0.68	4.0 x 4.0 x 2.0	μH	
L3	0.47 - 0.68	4.0 x 4.0 x 2.0	0.47 - 0.68	4.0 x 4.0 x 2.0	μH	
L4	0.68 - 1.2	4.0 x 4.0 x 2.0	0.68 - 1.2	4.0 x 4.0 x 2.0	μH	
C1	2x; 22	25V	2x; 22	25V	μF	
C2	0.1	16V; 0201	0.1	16V; 0201	μF	
C3	3x; 47	6.3V; 0805	3x; 47	6.3V; 0805	μF	
C4	3x; 47	6.3V; 0805	3x; 47	6.3V; 0805	μF	
C5	0.1	16V; 0201	0.1	16V; 0201	μF	
C6	2x; 22	25V	2x; 22	25V	μF	
C7	2x; 22	25V	2x; 22	25V	μF	
C8	3x; 47	6.3V; 0805	3x; 47	6.3V; 0805	μF	
C9	0.1	16V; 0201	0.1	16V; 0201	μF	
C10	2x; 22	25V	2x; 22	25V	μF	
C11	3x; 47	6.3V; 0805	3x; 47	6.3V; 0805	μF	
C12	0.1	16V; 0201	0.1	16V; 0201	μF	
C13	4.7	6.3V; 0402	4.7	6.3V; 0402	μF	
C14	4.7	6.3V; 0402	4.7	6.3V; 0402	μF	
C15	4.7	6.3V; 0402	4.7	6.3V; 0402	μF	
C16	4.7	6.3V; 0402	4.7	6.3V; 0402	μF	
C17	0.1	25V, X6S; 0201	0.1	25V, X6S; 0201	μF	
C18	0.1	25V, X6S; 0201	0.1	25V, X6S; 0201	μF	
C19	0.1	25V, X6S; 0201	0.1	25V, X6S; 0201	μF	
C20	0.1	25V, X6S; 0201	0.1	25V, X6S; 0201	μF	
C21	0.1	6.3V; 0201	0.1	6.3V; 0201	μF	
C22	0.1	6.3V; 0201	0.1	6.3V; 0201	μF	
C23	0.1	6.3V; 0201	0.1	6.3V; 0201	μF	
C24	0.1	6.3V; 0201	0.1	6.3V; 0201	μF	
C25	175	6.3V	175	6.3V	μF	1
C26	175	6.3V	175	6.3V	μF	
C27	350	6.3V	175	6.3V	μF	
C28	N/A	N/A	175	6.3V	μF	
C29	175	6.3V	175	6.3V	μF	1
C30	175	6.3V	175	6.3V	μF	
C31	350	6.3V	175	6.3V	μF	
C32	N/A		175	6.3V	μF	

NOTE 1 These capacitor values represent the distributed capacitance for the entire DIMM assuming max I_{tdc} and $I_{peakmax}$ defined in Electrical characteristics for each SWx. For a given DIMM design, the distributed capacitance for each SWx varies and is a function of I_{tdc} and $I_{peakmax}$ current requirement for that DIMM design. See actual DIMM design for total distributed capacitance.

2.7 Functional Operation

2.7.1 PMIC Input Voltage Supplies and Ramp Condition

The DDR5 PMIC has two input supplies from the platform: VIN_Bulk and VIN_Mgmt.

The VIN_Bulk supply is used by the PMIC for all output regulators except for the VOUT_1.8V and VOUT_1.0V LDO outputs regulators when not in switchover mode. The VIN_Bulk input supply may also be used to generate the internal bias voltage. Note that the VOUT_1.8V LDO output is separate and independent from SWD output, which is for the DRAM VPP rail. The VOUT_1.0V LDO output is separate and independent from SWA, SWB, or SWC.

The PMIC internally generates on its own bias voltage (VBias). At first power on, the VIN_Bulk input supply shall reach a minimum threshold voltage value per register Table 116, “Register 0x1A” [7:5] plus 1.0V offset before it can be detected as a valid input supply to the PMIC. The PMIC filters any non-monotonic noise after this threshold. After power on, with valid VIN_Mgmt input supply while PMIC is operating in non write protect mode of operation, if VIN_Bulk input supply is removed and re-applied, it must reach the same threshold voltage value per Table 116, “Register 0x1A” [7:5] plus 1.0 V offset.

The VIN_Mgmt supply is used to read out its internal non-volatile memory content and to supply VOUT_1.8V and VOUT_1.0V to other devices such as SPD, TS and RCD on the DIMM. At first power on, the VIN_Mgmt supply shall reach a minimum of 2.8V before it can be detected as a valid input supply to the PMIC. At power on, the PMIC floats CAMP signal and then drives CAMP output signal low only when VIN_Mgmt input supply reaches minimum of 2.8 V and PMIC VOUT_1.8V and VOUT_1.0V LDO outputs are valid. VIN_Bulk input supply does not trigger PMIC to drive CAMP output signal low at power on. The VIN_Mgmt supply is strictly a voltage input.

The CAMP output is pulled up to either 1.8 V or 3.3 V on the platform or on the host controller. The CAMP pullup voltage (either 1.8 V or 3.3 V) can be available before or after either VIN_Bulk or VIN_Mgmt is valid and stable. If CAMP pullup voltage is available before VIN_Mgmt or VIN_Bulk is applied, the CAMP signal is high and remains High with no leakage path or damage to the PMIC. When VIN_Mgmt is applied to the PMIC and after VOUT_1.8V and VOUT_1.0V LDO outputs are valid, the PMIC asserts CAMP output low.

Figure 11 and Figure 12 show PMIC power up sequence when power is first applied. The platform can power up VIN_Bulk and VIN_Mgmt supply in any sequence. Figure 11 shows VIN_Mgmt supply ramps up first prior to VIN_Bulk supply. Figure 12 shows VIN_Bulk supply ramps up first prior to VIN_Mgmt supply. The PMIC does not mandate any specific timing relationship between VIN_Bulk and VIN_Mgmt supply.

The PMIC updates register Table 98, “Register 0x08” [7] when VIN_Bulk input supply status is valid.

2.7.2 Power Up Initialization Sequence

During power on, the host shall:

1. Ramp up VIN_Mgmt supply; Ramp up VIN_Bulk supply; (No timing relationship between two supplies)
2. Hold VIN_Mgmt supply stable for a minimum of tVIN_Mgmt_to_Enable time
3. Hold VIN_Bulk supply stable for a minimum of tVIN_Bulk_to_Enable time
4. Query the status of the PMIC status register to determine if it is safe to enable VR.
5. If it is safe to enable, send VR Enable command by setting register Table 140, “Register 0x32” [7] = ‘1’ or by issuing DEVCTRL CCC.

2.7.2 Power Up Initialization Sequence (cont'd)

Once the VIN_Mgmt supply is valid and stable, the PMIC shall drive VOUT_1.8V and VOUT_1.0V supply within t1.8_Rdy and t1.0V_Rdy time. The PMIC shall enable I²C/I3C Basic bus interface function within tManagement_Rdy. The host shall not attempt to access the PMIC's memory registers until tManagement_Rdy timing requirement is satisfied. Further the host shall not attempt to issue VR Enable command until tVIN_Mgmt_to_Enable and tVIN_Bulk_to_Enable timing requirement is satisfied. In Figure 11, the PMIC allows access to its memory registers for indefinite period of time as long as VIN_Mgmt input supply is valid and PMIC does not require VIN_Bulk input supply.

The host may read PMIC's own internal memory content prior to ramping VIN_Bulk supply.

The host, prior to issuing VR Enable command, must keep VIN_Mgmt input supply valid as long as VOUT_1.8V and VOUT_1.0V LDO output are required. If VIN_Mgmt input supply is removed or drops below 2.8 V, the PMIC does not guarantee any operation including VOUT_1.8V and VOUT_1.0V LDO output as well as access to its I²C/I3C Basic interface regardless of VIN_Bulk input supply status.

After host issues VR Enable command to the PMIC, the PMIC offers the input supply switchover function. The PMIC has an automatic internal input supply switchover function from VIN_Mgmt input supply to VIN_Bulk input supply. The PMIC triggers the switchover to VIN_Bulk input supply when VIN_Mgmt input supply drops below the threshold set in register Table 137, "Register 0x2F" [7]. The internal input supply switchover is for PMIC's VOUT_1.8V and VOUT_1.0V LDO output. The PMIC's I²C/I3C Basic interfaces (SCL/SDA) are kept alive when PMIC switches over to VIN_Bulk input supply. Figure 13 shows automatic internal switchover function when VIN_Mgmt input supply drops below the threshold while maintaining its LDO outputs as well as I²C/I3C Basic interfaces. Under the switchover conditions VIN_Mgmt back-feed voltage shall be less than 0.2 V. While PMIC is in switchover mode to VIN_Bulk, the VIN_Mgmt input supply can re-power backup at any time and PMIC switches back to VIN_Mgmt input supply for its LDO outputs and I²C/I3C interface continues to operate as normal.

The PMIC shall power up its output switch regulators when it registers VR Enable command.

After VR Enable command is registered, the PMIC shall complete the following steps within tPMIC_PWR_GOOD_OUT:

1. Check VIN_Bulk, VIN_Mgmt and VBias Power Good status is valid.
2. Power up itself - PMIC executes Power On Sequence Config 0 to Power On Sequence Config 3 registers and configures PMIC internal registers as programmed in DIMM vendor memory space registers.
3. Power up all enabled output switch regulators and ready for normal operation
4. Update status registers Table 98, "Register 0x08" [5:2] and floats CAMP signal.

If PMIC CAMP signal is not pulled High within tPMIC_PWR_GOOD_OUT time, the host can access the PMIC status registers for detailed information after tPMIC_PWR_GOOD_OUT time. The PMIC may NACK for any host request on I²C or I3C bus after VR Enable command until tPMIC_PWR_GOOD_OUT time expires.

Note that in Figure 11 and Figure 12 the specific sequence of ramping the output regulators (VOUT_A, VOUT_B, VOUT_C, and VOUT_D) is for example purpose only. The specific ramp up sequence is configurable through the registers.

Once PMIC's output regulators are running, the PMIC allows VIN_Bulk input supply to vary. Figure 14 shows that VIN_Bulk can go as low as VIN_Bulk Min value (4.25 V) and PMIC output regulators will continue to operate as normal. The VIN_Mgmt input supply can drop and may re-power back up at any time.

2.7.3 Power Up Sequence

Figure 11 shows the power up initialization sequence.

After VIN_Bulk supply is valid and stable, the PMIC powers up its output regulators when the system host sends VR Enable command. The PMIC generates its bias voltage (VBias) on its own using VIN_Bulk input supply. Further it executes Power On Sequence Config0 to Config3 as configured in register Table 152, “Register 0x40” to Table 155, “Register 0x43” to enable its output regulators in the sequence as specified. The PMIC also follows the settings as specified in register 0x44 to register 0x6F for each of the enabled output. The PMIC ensures CAMP signal is floated within maximum of tPMIC_PWR_GOOD_OUT after registering VR Enable command.

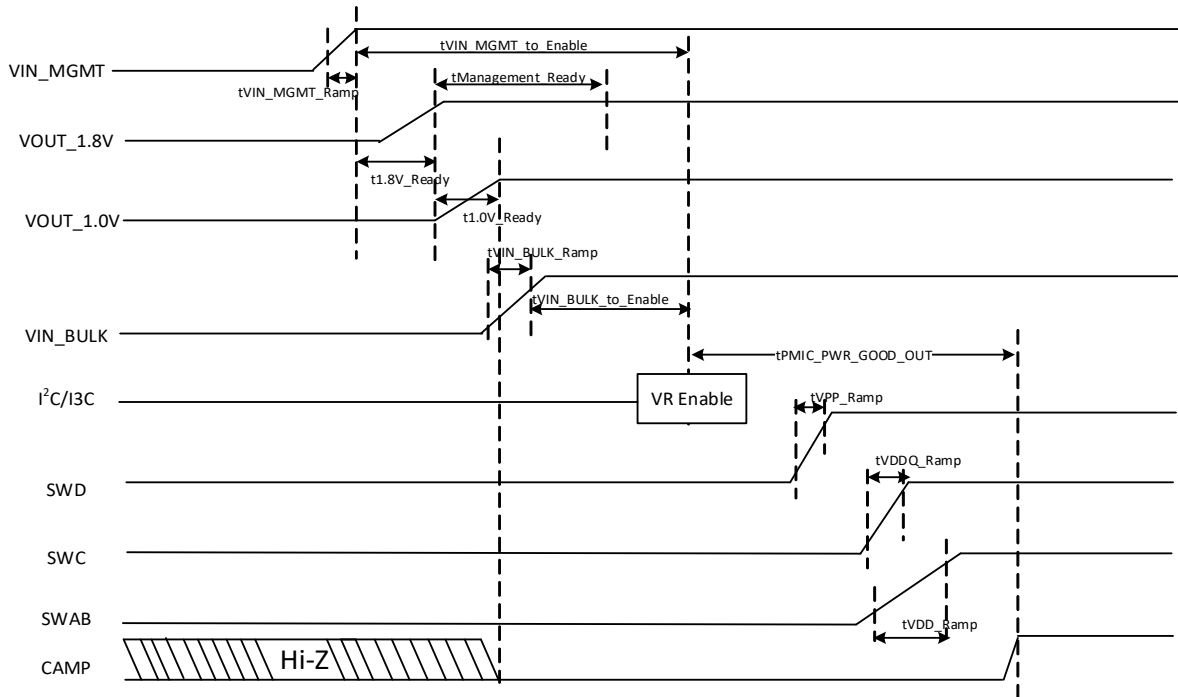


Figure 11 — PMIC Power Up Sequence; VIN_Mgmt Followed by VIN_Bulk

2.7.3 Power Up Sequence (cont'd)

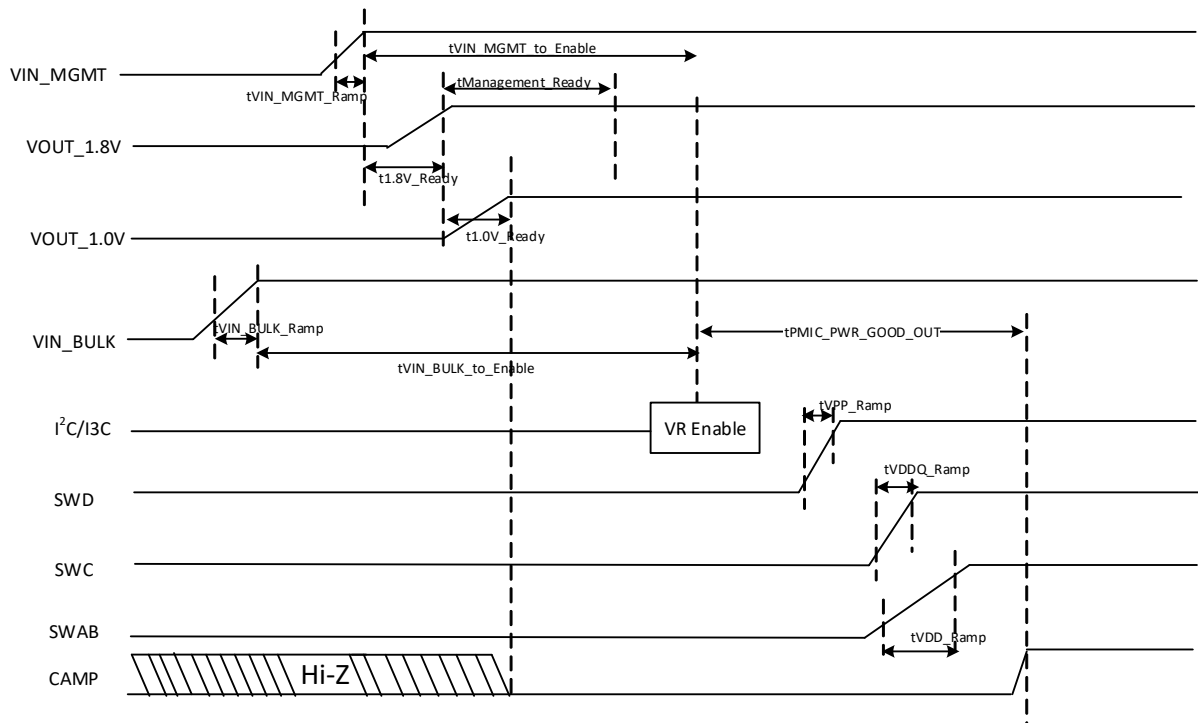


Figure 12 — PMIC Power Up Sequence; VIN_Bulk Followed by VIN_Mgmt

2.7.3 Power Up Sequence (cont'd)

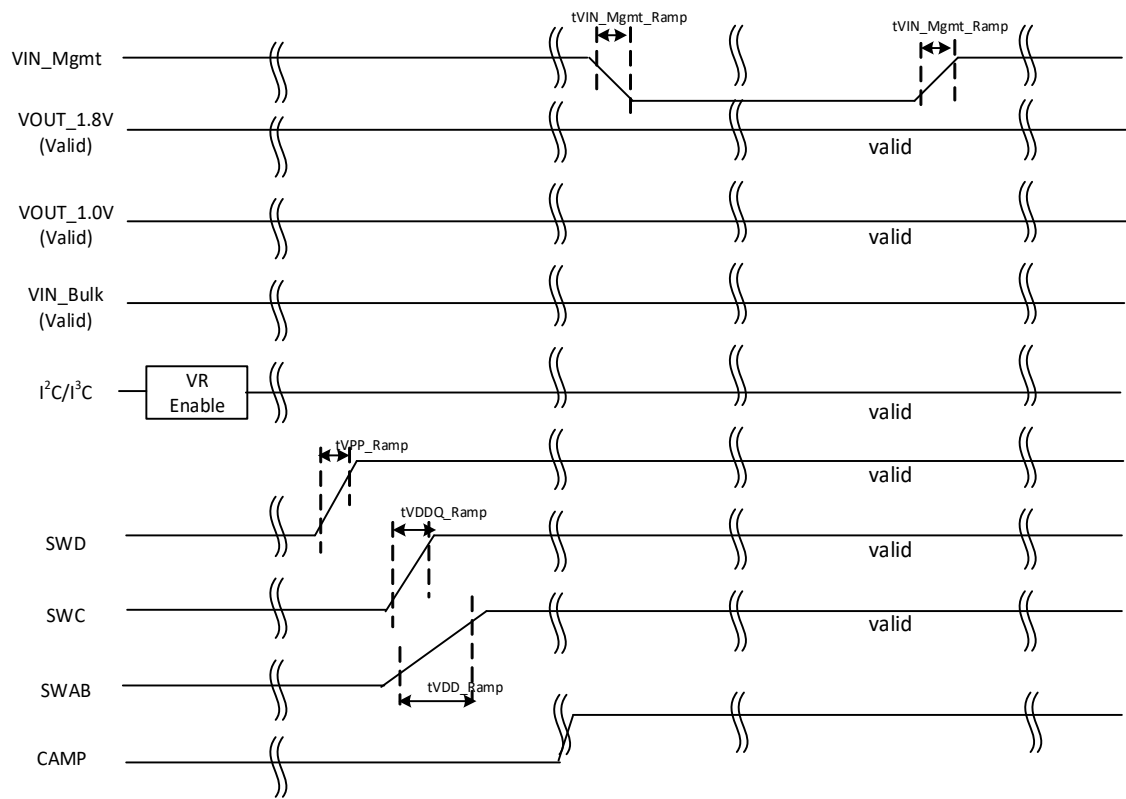


Figure 13 — VIN_Mgmt Input Supply to VIN_Bulk Input Supply Switchover Function

2.7.3 Power Up Sequence (cont'd)

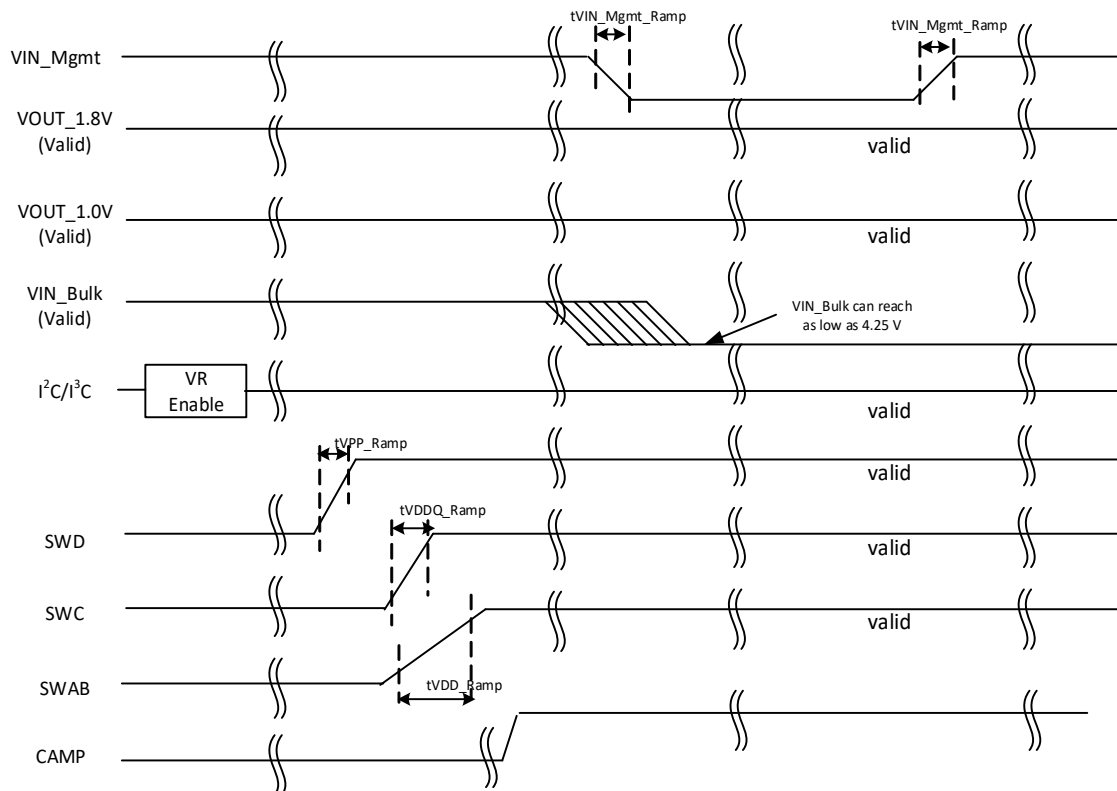


Figure 14 — VIN_Bulk Transition

The timing waveform example in Figure 14 assumes VIN_Bulk threshold is set to 4.25 V in Table 116, "Register 0x1A" [7:5] and hence CAMP signal remains at valid High level.

2.7.4 Enabling PMIC Output Switch Voltage Regulators

After first power on, the PMIC automatically enables VOUT_1.8V and VOUT_1.0V LDO output regulators and primary I²C/I³C Basic port based on valid VIN_Mgmt input.

Figure 15 shows the timing relationship once the PMIC receives VR Enable command and when it floats CAMP output signal; timing parameter tPMIC_PWR_GOOD_OUT applies. This timing parameter is a sum of maximum soft start time and configured delay for each power on sequence config registers that are executed plus additional 5 ms timing margin error. The waveform shows each buck regulator output soft start time and delay time once the soft start time expires for each power on sequence config0 to power on sequence config3 registers. Note that if more than one regulators are enabled in a power on sequence config register and if those regulators have different soft start time programmed, then the larger value of that soft start time is used as a reference for delay timer to start. Each regulator will still follow different soft start time to turn on the buck regulator.

The specific example in Figure 15 uses only three power on sequence config0 to config2 registers and only one buck regulator is enabled in power on sequence config 0 register and power on sequence config 1 register. The power on sequence config 2 register enables dual phase regulator for SWA and SWB.

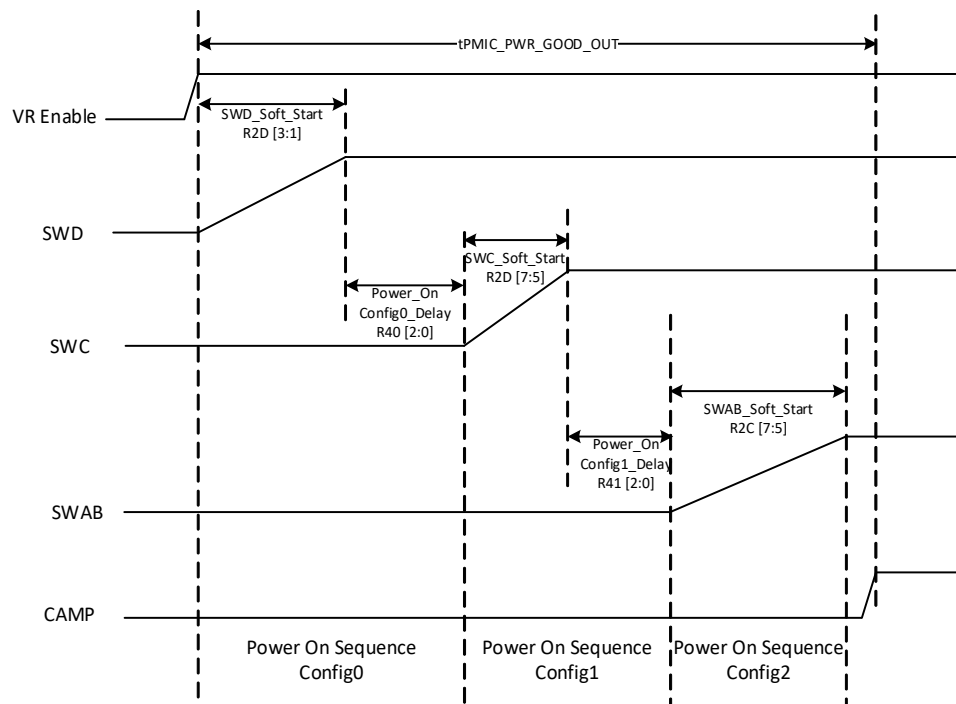


Figure 15 — PMIC Power On Timing

2.7.5 Power Down Output Regulators

Regardless of how PMIC's output regulators are turned on, the PMIC's output regulators are powered down as described below depending on mode of operation.

In non write protect mode of operation, the PMIC allows host to power down any or all output regulators in non write protect mode. The host can disable PMIC's any or all output regulators by any of the three methods below.

1. The VR Disable command (Table 140, "Register 0x32" [7] = '0'). The PMIC executes power off sequence config0 (Table 169, "Register 0x58") to power off sequence config3 (Table 172, "Register 0x5B") to preserve the appropriate voltage relationship as configured by the DIMM vendors. The PMIC keeps the CAMP signal floating (i.e., it remains High) because this is an intentional command from the host and not a fault condition. Note that host can re-enable the PMIC's output regulator by issuing VR Enable command. The PMIC executes power on sequence config 0 to config 3 registers and keeps the CAMP signal floating (i.e it remains High).
2. Configuring one or more bits in Table 137, "Register 0x2F" [6:3] to '0' in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 (Table 169, "Register 0x58") to power off sequence config3 (Table 172, "Register 0x5B") on its own. The PMIC keeps the CAMP signal floating (i.e it remains High) because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in Table 137, "Register 0x2F" [6:3] to '1' in any specific sequence that is desired by the host. The PMIC keeps the CAMP signal floating (i.e., it remains High).
3. By driving CAMP input low. The PMIC executes power off sequence config0 (Table 169, "Register 0x58") to power off sequence config3 (Table 172, "Register 0x5B") to preserve the appropriate voltage relationship as configured by the DIMM vendors.

In write protect mode of operation, the host can disable PMIC's all enabled output regulators by any of the two methods below.

1. Power cycle the PMIC.
2. By driving CAMP input low. The PMIC executes power off sequence config0 (Table 169, "Register 0x58") to power off sequence config3 (Table 172, "Register 0x5B") to preserve the appropriate voltage relationship as configured by the DIMM vendors.

Regardless of the either mode of the operation, the PMIC, on its own, can generate VR Disable command at any time due to one or more events listed in Table 27 under column "Trigger VR Disable". The PMIC executes power off sequence config0 (Table 169, "Register 0x58") to power off sequence config3 (Table 172, "Register 0x5B") to preserve the appropriate voltage relationship as configured by the DIMM vendors. The PMIC may also reset its Vbias LDO regulator.

Figure 16 shows the timing relationship once the PMIC registers VR Disable command internally due to fault. The waveform shows each buck regulator output soft stop time and delay time once the soft stop time expires from each power off sequence config0 to power off sequence config3 registers. Note that if more than one regulators are disabled in a power off sequence config register and if those regulators have different soft stop time programmed, then the larger value of that soft stop time is used as a reference for delay timer to start. Each regulator will still follow different soft stop time to turn off the buck regulator.

The specific example in Figure 16 uses only three power off sequence config0 to config2 registers and only one buck regulator is disabled in power off sequence config 1 register and power off sequence config 2 register. The power off sequence config 0 register disables dual phase regulator for SWA and SWB.

2.7.5 Power Down Output Regulators (cont'd)

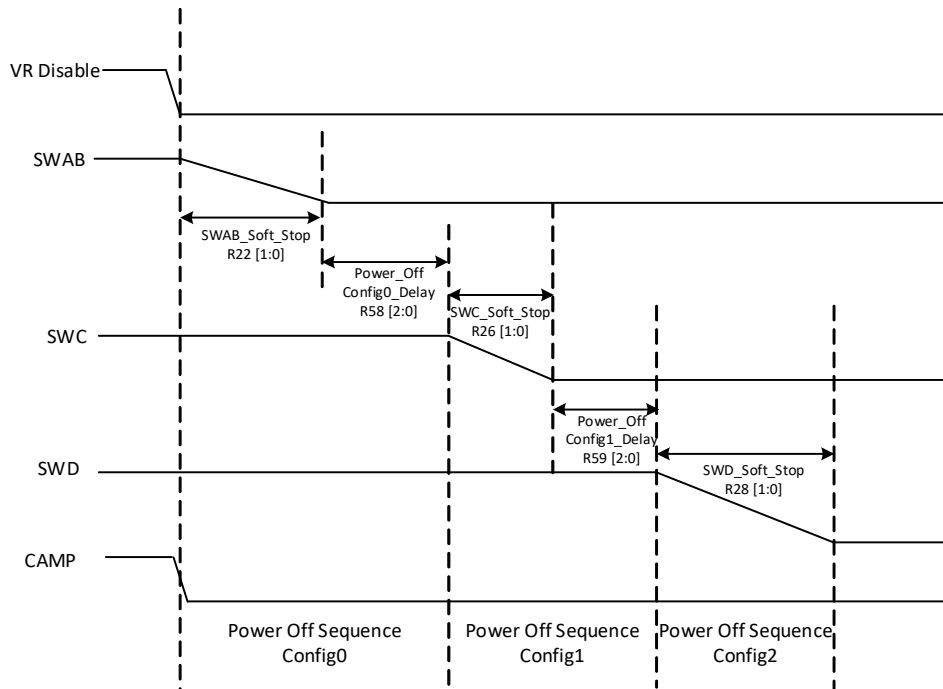


Figure 16 — PMIC Power Off Timing Due to Internal Fault Condition

2.7.6 Power Down Output Regulators During Power On Sequence

During power on, as described in clause 2.7.2, it is possible that PMIC can trigger VR Disable command on its own as described in Table 27, “Events Interrupt Summary” when one or more regulators are already turned on even while other remaining output regulators are not yet turned on because PMIC has not completed the power on sequence config registers. For these type of cases, the PMIC will not execute the remaining power on sequence config registers and will immediately jump to executing the power off sequence config0 to power off sequence config3 registers. The PMIC will update the status registers and error log registers appropriately as normal because it generated VR Disable command on its own. The CAMP output signal would remain low.

2.7.7 CAMP Signal

The CAMP (Control AND Monitor Port) signal provides three different functions.

1. Register write protect function
2. Fail_n function
3. Status function

2.7.7.1 Register Write Protect Function

By default, PMIC register write protect function is enabled (i.e., Table 137, “Register 0x2F” [2] = ‘0’). The CAMP input signal level determines when PMIC enters or exits the write protect mode. The PMIC enters the write protect mode when CAMP signal is at logic level High and Table 137, “Register 0x2F” [2] = ‘0’. PMIC exits the write protect mode when CAMP signal is at logic level Low. When PMIC is in write protect mode, the PMIC does not allow to modify registers Table 111, “Register 0x15” to Table 137, “Register 0x2F”, Table 140, “Register 0x32”, and Table 143, “Register 0x35” in the host region as well as Table 152, “Register 0x40” to Register 0x6F in the DIMM vendor region. These registers are write protected marked with RED color cells in “Register” column in Table 93, “Host Region - Register Map”. The PMIC simply ignores the host request for write operation in write protect mode. PMIC allows all register read access in write protect mode.

Once PMIC is in write protect mode, there are 3 ways PMIC can exit write protect mode:

1. PMIC sees CAMP input signal Low (clause 2.7.7.2)
2. PMIC triggers internal fault event (VIN_Bulk OV, VIN_Bulk UV, SWx_OV, SWx_UV) and asserts CAMP signal low.
3. PMIC goes through power cycle or power down cycle (i.e., simultaneous removal of VIN_Bulk and VIN_Mgmt input supplies)

If Table 137, “Register 0x2F” [2] = ‘1’, the PMIC does not enter write protect mode. The PMIC CAMP input signal has no effect on write protect function. The PMIC allows write and read access to all registers. Caution: The operation of non-write protect mode should be limited to lab and debug environment instead of normal system operation.

2.7.7.2 Fail_n Function

By default, PMIC Fail_n function is enabled (Table 140, “Register 0x32” [4] = ‘0’). When PMIC CAMP input signal transitions from High to Low, the PMIC executes VR Disable command (i.e., execute power off sequence config0 to config3 registers), asserts CAMP signal low (if Table 140, “Register 0x32” [3] = ‘0’), exits the write protect mode and clears Table 140, “Register 0x32” [7] to ‘0’.

If Table 140, “Register 0x32” [4] = ‘1’, the PMIC Fail_n function is disabled. When CAMP signal transition from High to Low, The PMIC does not execute VR Disable command (i.e., does not execute power off sequence config0 to config3 registers), does not assert CAMP signal low, exits the write protect mode and does not clear Table 140, “Register 0x32” [7] to ‘0’.

The Fail_n function is independent of PMIC’s write protect function.

2.7.7.3 Status Function

The PMIC CAMP PWR_GOOD output signal indicates status of VIN_Bulk input supply and all output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_D, VOUT_1.8V, VOUT_1.0V, VBias). Once PMIC receives VR Enable command, the PMIC floats CAMP pin when VIN_Bulk input supply is valid and all enabled output regulator’s (VOUT_A, VOUT_B, VOUT_C, VOUT_D, VOUT_1.8V, VOUT_1.0V, VBias) tolerances are maintained as configured in the appropriate register space. Note that CAMP pin is not affected based on VIN_Mgmt input supply.

At first power up, with stable and valid input supply VIN_Mgmt as well as VOUT_1.8V and VOUT_1.0V LDO outputs, the PMIC asserts CAMP pin low however PMIC updates corresponding status register. Once PMIC receives VR Enable command from the host, the PMIC enables all appropriate output regulators and updates corresponding status registers and enters state called as “Regulation”. At this point, PMIC floats CAMP PWR_GOOD output and the external board pullup resistor pulls the CAMP pin high. Once the CAMP pin is pulled high (i.e., no other PMIC is driving the CAMP pin low), the PMIC enters state stated called as “online” state.

2.7.7.3 Status Function (cont'd)

Once the CAMP pin is high, if PMIC detects any condition either on VIN_Bulk input supply or any of the output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_D, VOUT_1.8V, VOUT_1.0V, VBias) that causes the PMIC to update its status registers to indicate the power status is not good, then PMIC asserts CAMP pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the CAMP pin float even if the condition that triggered the PMIC to assert the CAMP pin no longer exists. In other words, the PMIC's CAMP pin is latched and once latched, it must be explicitly addressed by the host.

Regardless of whether PMIC is operating in write protect mode or not, the PMIC always asserts CAMP signal low to indicate the status if there is a fault event.

2.7.8 GSI_n Signal

General Status Interrupt (GSI_n) is an Open Drain output signal. By default at power on, GSI_n output is disabled. The host can enable the GSI_n output by setting Table 117, "Register 0x1B" [3] = '1'. Typically, GSI_n output is pulled up to 1 K Ω resistor to 1.8 V or 3.3 V. The PMIC asserts GSI_n output for the events as described in Table 27, "Events Interrupt Summary".

2.7.9 State Transition Diagram

Following is a summary of high level description of basic PMIC states.

Offline State:

- VIN_Mgmt is invalid and VIN_Bulk = X (valid or invalid); LDOs are invalid
- All registers are reset to specified default values
- CAMP is Hi-Z

Configuration (non write protect) state:

- At initial configuration state, all registers follow the register attributes as defined and read/write accessible.
- The I²C/I³C bus interface is alive and running.
- LDOs are valid; switch regulators are off
- CAMP is low

Regulation (non write protect) state:

- All registers are read/write accessible.
- All enabled output rails are active
- Internal power good is floated; external CAMP is low

Online (write protect) state:

- All registers are readable. All non protect registers are writable.
- All enabled output rails are active, i.e., PMIC has registered VR Enable command with Table 137, "Register 0x2F" = '0'.
- CAMP is high
- Note: Prior to PMIC registering VR Enable command, PMIC may be configured to not execute VR Enable command and float its CAMP PWR_GOOD output signal (Table 140, "Register 0x32" = 0x08) with default configuration of Table 137, "Register 0x2F" = '0'. In this configuration, PMIC also enters write protect state when CAMP signal is pulled high.

2.7.9 State Transition Diagram (cont'd)

Figure 17 shows high level simplified state diagram. Specific transition details are function of PMIC's configuration register settings (e.g., R2F, R32, etc., as well as CAMP signal and input/output supplies). Please refer to detail functional description and configuration register definition for PMIC operation. Consider an example of a valid PMIC operation: When the PMIC first powers up from an offline state, the PMIC register Table 137, "Register 0x2F" [2] can be configured to '1' followed by VR Enable command. After PMIC turns on all regulators and floats CAMP signal such that it is pulled up High, PMIC is in online state but allows all register write/read access as PMIC is not in write protect state. In this state, the PMIC does allow to clear Table 137, "Register 0x2F" [2] to '0' which will cause PMIC to enter in write protect state as the CAMP signal was already pulled up High and the PMIC was in regulation.

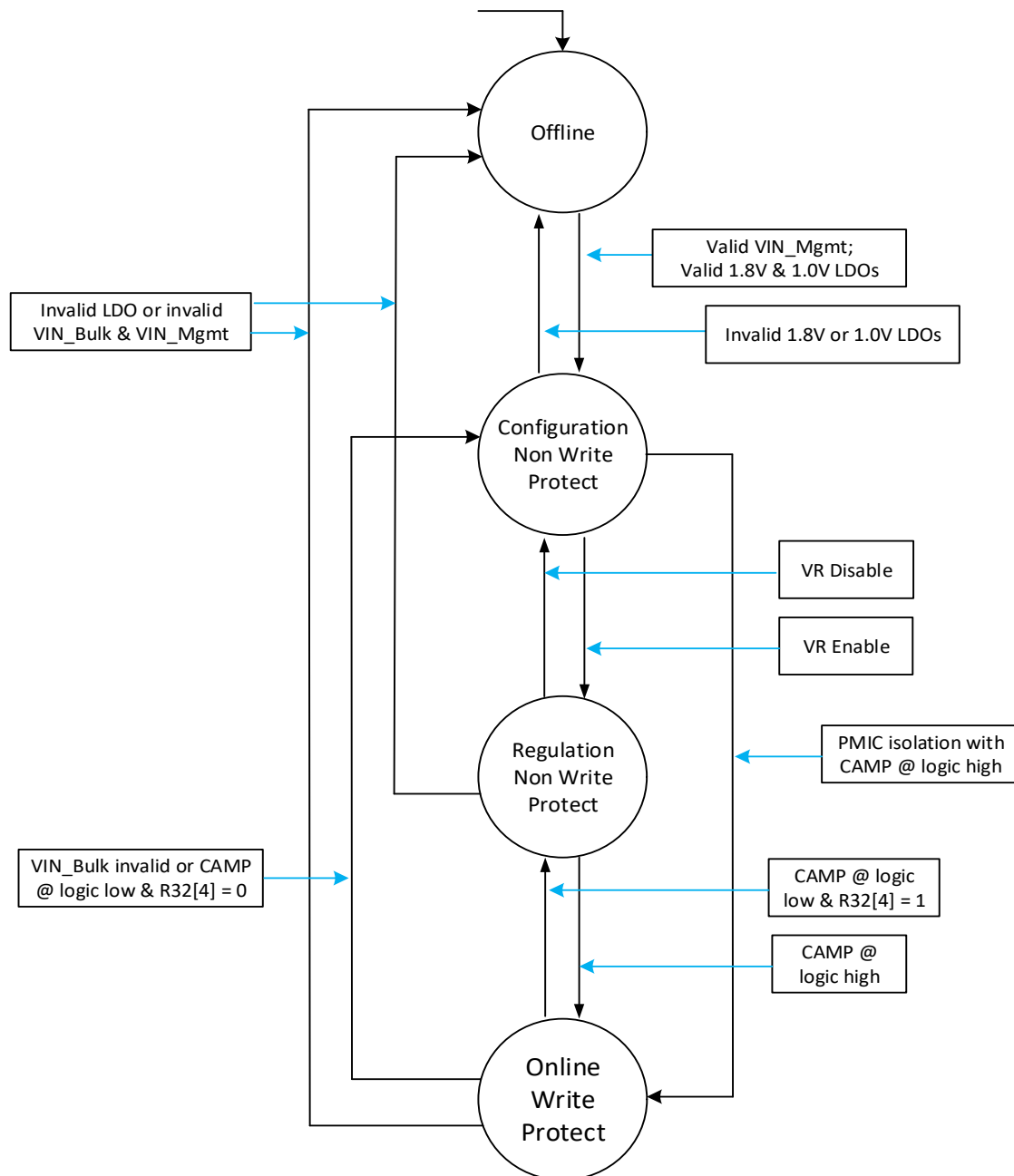


Figure 17 — High Level State Transitions

2.7.10 Function Interrupt - CAMP and GSI_n Output Signals

This clause defines the output functionality of GSI_n pin and CAMP pin.

When mask register bits are not set, the PMIC asserts its GSI_n output and CAMP output signals as shown in Table 27 when any event occurs. The table also highlights 11 events that causes PMIC to generate internally VR Disable command. For remaining events that does not trigger internal VR Disable command, the PMIC continues to operate as normal.

Table 27 — Events Interrupt Summary

Event	Status Bit	Clear Bit	Mask Bit	Threshold Bits	Trigger VR Disable?	CAMP Output	GSI_n Output
VIN_Bulk Power Good	R08 [7]	R10 [7]	R15 [7]	R1A [7:5]	No	Low	Low
VIN_Bulk Over Voltage	R08 [0]	R10 [0]	R15 [0]	R1B [7]	Yes	Low	Low
VIN_Mgmt Over Voltage	R08 [1]	R10 [1]	R15 [1]	R1B [5]	No	High	Low
SWA Output Power Good	R08 [5]	R10 [5]	R15 [5]	R21 [0]; R22 [7:6]	No	Low	Low
SWB Output Power Good	R08 [4]	R10 [4]	R15 [4]	R23 [0]; R24 [7:6]	No	Low	Low
SWC Output Power Good	R08 [3]	R10 [3]	R15 [3]	R25 [0]; R26 [7:6]	No	Low	Low
SWD Output Power Good	R08 [2]	R10 [2]	R15 [2]	R27 [0]; R28 [7:6]	No	Low	Low
1.8 V LDO Power Good	R09 [5]	R11 [5]	R16 [5]	R1A [2]	No	Low	Low
1.0 V LDO Power Good	R33 [2]	R14 [2]	R19 [2]	R1A [0]	No	Low	Low
VBias LDO Power Good	R09 [6]	R11 [6]	R16 [6]	R1A [3]	No	Low	Low
SWA Output Over Voltage	R0A [7]	R12 [7]	R17 [7]	R22 [5:4]	Yes	Low	Low
SWB Output Over Voltage	R0A [6]	R12 [6]	R17 [6]	R24 [5:4]	Yes	Low	Low
SWC Output Over Voltage	R0A [5]	R12 [5]	R17 [5]	R26 [5:4]	Yes	Low	Low
SWD Output Over Voltage	R0A [4]	R12 [4]	R17 [4]	R28 [5:4]	Yes	Low	Low
SWA Output Under Voltage	R0B [3]	R13 [3]	R18 [3]	R22 [3:2]	Yes	Low	Low
SWB Output Under Voltage	R0B [2]	R13 [2]	R18 [2]	R24 [3:2]	Yes	Low	Low
SWC Output Under Voltage	R0B [1]	R13 [1]	R18 [1]	R26 [3:2]	Yes	Low	Low
SWD Output Under Voltage	R0B [0]	R13 [0]	R18 [0]	R28 [3:2]	Yes	Low	Low
VBias LDO Output or VIN_Bulk Input Under Voltage	R33 [3]	R14 [3]	R19 [3]	Vendor Specific	Yes	Low	Low
SWA Output Current Limit	R0B [7]	R13 [7]	R18 [7]	R20 [7:6]	No	High	Low
SWB Output Current Limit	R0B [6]	R13 [6]	R18 [6]	R20 [5:4]	No	High	Low
SWC Output Current Limit	R0B [5]	R13 [5]	R18 [5]	R20 [3:2]	No	High	Low
SWD Output Current Limit	R0B [4]	R13 [4]	R18 [4]	R20 [1:0]	No	High	Low
SWA Output High Current/Power	R09 [3]	R11 [3]	R16 [3]	R1C [7:2]	No	High	Low
SWB Output High Current/Power	R09 [2]	R11 [2]	R16 [2]	R1D [7:2]	No	High	Low
SWC Output High Current/Power	R09 [1]	R11 [1]	R16 [1]	R1E [7:2]	No	High	Low
SWD Output High Current/Power	R09 [0]	R11 [0]	R16 [0]	R1F [7:2]	No	High	Low
High Temperature Warning	R09 [7]	R11 [7]	R16 [7]	R1B [2:0]	No	High	Low
Critical Temperature	R08[6]	N/A	N/A	R2E [2:0]	Yes	Low	Low
VIN_Mgmt to VIN_Bulk Switchover	R09 [4]	R11 [4]	R16 [4]	R2F [7]	No	High	Low
Valid VIN_Mgmt in Switchover State	R33 [4]	R14 [4]	R19 [4]	N/A	No	High	Low
PEC Error	R0A [3]	R12 [3]	R17 [3]	N/A	No	High	Low
Parity Error	R0A [2]	R12 [2]	R17 [2]	N/A	No	High	Low

The host is expected to read appropriate status registers to determine and isolate the cause of the GSI_n signal assertion or CAMP signal assertion. The host may attempt to clear or mask the appropriate corresponding interrupt event. The PMIC keeps the GSI_n signal asserted or CAMP signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the host. Table 28 and Table 29 show the PMIC's response of GSI_n signal and CAMP output signal for each event before and after host issues the Clear command. Table 28 and Table 29 assume that all mask bits are either '0' or '1' for simplicity.

2.7.10 Function Interrupt - CAMP and GSI_n Output Signals (cont'd)

Table 28 — PMIC Response for Clear Command by Host - 1

	Event Occurred; All Mask Bits = '0'		Clear Command; Event Not Present; All Mask Bits = '0'		Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'	
			R2F [1:0] = '00' or '01' or '10'		R2F [1:0] = '00'		R2F [1:0] = '00'	
Event	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output
VIN_Bulk Power Good	Low	Low	High	High	Low	High	High	High
VIN_Bulk Over Voltage	Low	Low	Low	High	Low	High	Low	High
VIN_Mgmt Over Voltage	High	Low	High	High	High	High	High	High
SWA Output Power Good	Low	Low	High	High	Low	High	High	High
SWB Output Power Good	Low	Low	High	High	Low	High	High	High
SWC Output Power Good	Low	Low	High	High	Low	High	High	High
SWD Output Power Good	Low	Low	High	High	Low	High	High	High
1.8 V LDO Power Good	Low	Low	High	High	Low	High	High	High
1.0 V LDO Power Good	Low	Low	High	High	Low	High	High	High
VBias LDO Power Good	Low	Low	High	High	Low	High	High	High
SWA Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
VBias LDO Output or VIN_Bulk Input Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWD Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current/Power	High	Low	High	High	High	High	High	High
SWB Output High Current/Power	High	Low	High	High	High	High	High	High
SWC Output High Current/Power	High	Low	High	High	High	High	High	High
SWD Output High Current/Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	P/C	P/C	Low	Low	P/C	P/C
VIN_Mgmt to VIN_Bulk Switchover	High	Low	High	High	High	High	High	High
Valid VIN_Mgmt in Switchover	High	Low	High	High	High	High	High	High
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

2.7.10 Function Interrupt - CAMP and GSI_n Output Signals (cont'd)

Table 29 — PMIC Response for Clear Command by Host - 2

	Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'		Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'	
	R2F [1:0] = '01'		R2F [1:0] = '01'		R2F [1:0] = '10'		R2F [1:0] = '10'	
Event	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output
VIN_Bulk Power Good	High	Low	High	High	High	High	High	High
VIN_Bulk Over Voltage	Low	Low	Low	High	Low	High	Low	High
VIN_Mgmt Over Voltage	High	Low	High	High	High	High	High	High
SWA Output Power Good	High	Low	High	High	High	High	High	High
SWB Output Power Good	High	Low	High	High	High	High	High	High
SWC Output Power Good	High	Low	High	High	High	High	High	High
SWD Output Power Good	High	Low	High	High	High	High	High	High
1.8 V LDO Power Good	High	Low	High	High	High	High	High	High
1.0 V LDO Power Good	High	Low	High	High	High	High	High	High
VBias LDO Power Good	High	Low	High	High	High	High	High	High
SWA Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
VBias LDO Output or VIN_Bulk Input Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWD Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current/Power	High	Low	High	High	High	High	High	High
SWB Output High Current/Power	High	Low	High	High	High	High	High	High
SWC Output High Current/Power	High	Low	High	High	High	High	High	High
SWD Output High Current/Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	P/C	P/C	Low	Low	P/C	P/C
VIN_Mgmt to VIN_Bulk Switchover	High	Low	High	High	High	High	High	High
Valid VIN_Mgmt in Switchover	High	Low	High	High	High	High	High	High
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Note that when host masks any of the event in appropriate register, it only masks the assertion of GSI_n output signal or assertion of CAMP output signal. The PMIC functional behavior remains the same as noted for each event other than assertion of GSI_n output signal and assertion of CAMP output signal.

2.7.11 Input Power Good Status

There is one possibility where PMIC recognizes the input supply fail.

1. VIN_Bulk goes below the threshold set in register Table 116, “Register 0x1A” [7:5].

When this event occurs for a period longer than $t_{\text{Input_PWR_GOOD_GSI_Assertion}}$ time then PMIC sets the register Table 98, “Register 0x08” [7] and drives GSI_n and CAMP output signal as shown in Table 27 at the same time. The PMIC allows access to all registers and PMIC continues to operate as normal as long as VIN_Bulk input remains above 4.25 V. See also clause 2.7.15. The host is responsible for taking any specific action. The host may clear the VIN_Bulk input power good status register by writing ‘1’ to register Table 98, “Register 0x08” [7] or by writing ‘1’ to global status clear register Table 110, “Register 0x14” [0]. If the input power not good condition is still present then PMIC will continue to drive GSI_n and CAMP output signal as in Table 27 and the status register Table 98, “Register 0x08” [7] will remain at ‘1’. If the input power not good condition persists, the host may set the appropriate mask register to remove GSI_n or CAMP output signal as shown in Table 28 and Table 29.

Note that after VR enable command, when VIN_Mgmt input goes below the threshold set in register Table 137, “Register 0x2F” [7], it is reported as switchover event as described in clause 2.7.20. Prior to VR Enable command, the VIN_Mgmt is always required to be above 2.8 V to guarantee PMIC’s functionality as described in clause 2.7.2.

2.7.12 Input Over Voltage Protection

An input over voltage protection mechanism is implemented to limit the voltages to the PMIC. The PMIC actively monitors the input voltage VIN_Bulk and VIN_Mgmt rail.

There are two possibilities where PMIC recognizes the input over voltage event.

1. VIN_Mgmt input goes above the threshold set in register Table 117, “Register 0x1B” [5].
2. VIN_Bulk input goes above the threshold set in register Table 117, “Register 0x1B” [7].

When either one or both event occurs for a period longer than $t_{\text{Input_OV_GSI_Assertion}}$ time then PMIC sets the register Table 98, “Register 0x08” [1:0] accordingly and drives GSI_n output signal as shown in Table 27 at the same time. Note that at this point, the PMIC does not assert CAMP output signal. The PMIC allows access to all registers and PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may clear the VIN_Mgmt or VIN_Bulk input over voltage status register by writing ‘1’ to register Table 106, “Register 0x10” [1:0] appropriately or by writing ‘1’ to global status clear register Table 110, “Register 0x14” [0]. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status register Table 98, “Register 0x08” [1:0] will remain at ‘1’.

In non write protect mode, if VIN_Bulk input supply over voltage condition persists greater than $t_{\text{Input_OV_VR_Disable}}$ time then PMIC internally generates VR Disable command and disables all of its switching output regulators and asserts CAMP signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the CAMP signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the VIN_Bulk input over voltage status register as well as any other relevant status registers individually or by writing ‘1’ to global status clear register Table 110, “Register 0x14” [0] which triggers the GSI_n signal to be de-asserted. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status register Table 98, “Register 0x08” [0] will remain at ‘1’. Once the status register is cleared and GSI_n output signal is de-asserted, the host may re-enable the PMIC’s output switching regulator by issuing VR Enable command. The PMIC enables output switching regulators and ensures CAMP signal is floated when all of its output regulators are normal and input over voltage condition is no longer present.

In write protect mode, if VIN_Bulk input supply over voltage condition persists greater than $t_{\text{Input_OV_VR_Disable}}$ time then PMIC internally generates VR Disable command and disables all of its switching output regulators by executing Power Off Sequence configuration registers, asserts CAMP signal low and returns to configuration mode. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active.