

JEDEC STANDARD

PMIC5100 Power Management IC Standard

**JESD301-2
Rev. 1.03**

October 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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PMIC5100 POWER MANAGEMENT IC STANDARD

(From JEDEC Board Ballot JCB-22-07, formulated under the cognizance of the JC-40.1 Subcommittee on Digital Logic Families and Applications, item 336.01C).

1 Scope

This standard defines the specification of interface parameters, signaling protocols, and features for PMIC devices used for memory module applications. The designation PMIC5100 refers to the device specified by this document.

The purpose is to provide a standard for the PMIC5100 device for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

Unless otherwise noted in the document, any illegal operation is not allowed and device operation is not guaranteed.

NOTE: The designation PMIC5100 refers to a portion of the part number designation of a series of commercial logic devices common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

1.1 Device Standard

1.1.1 Description

The PMIC5100 is designed for typical DDR5 SODIMM as well as DDR5 UDIMM. The PMIC features three step down switching regulators and two LDO regulators.

The PMIC is designed to support approximately TBD Watts of power. The PMIC is powered from VIN_Bulk input for the entire PMIC including the switching regulators and LDO output regulators. The PMIC supports selectable interface (I²C or I3C Basic) to fit various application environment. The PMIC device is intended to operate up to 12.5 MHz on a 1.0 V I3C Basic bus or up to 1 MHz on 1.0 V to 3.3 V I²C bus.

1.1.2 Common Feature Summary

- VIN_Bulk input supply range: 4.25 V to 5.5 V
- Three step down switching regulators: SWA, SWB, and SWC
- Programmable dual phase and single phase regulator for SWA and SWB
- 2 LDO regulators: VOUT_1.8V, VOUT_1.0V
- Error injection capability
- Persistent error log registers
- Secure mode and programmable mode of operation
- Independently programmable output voltages, power up and power down sequence for switch regulators
- Output power good status reporting mechanism
- VIN_Bulk input supply protection feature: Input over voltage
- Output switch regulators protection features: Output over voltage, output under voltage, output current limiter
- Output current and power measurement, output current threshold mechanism
- Temperature measurement, temperature warning threshold, critical temperature shutdown
- Multi Time Programmable (MTP) Non-Volatile Memory
- Programmable and DIMM specific registers for customization
- General Status Interrupt (GSI) function
- Flexible Open Drain IO (I²C) and Push Pull (I3C Basic) IO support
- Flexible mechanism to enable switch regulators (with VR_EN pin or VR Enable command on I²C or I3C Basic interface)
- Idle Power State (P1 State)

2 PMIC Pin List and Package

2.1 Pin List

Table 1 — PMIC Pin Description

Pin Count	Pin Name	Type	Description
3	VIN_Bulk_A VIN_Bulk_B VIN_Bulk_C	I	5 V power input supply to the PMIC for SWA, SWB and SWC respectively. All three VIN_Bulk input pins must be connected to the 5 V input supply even if one or more output regulators are not intended to be used.
1	VIN	I	5 V power input supply to the PMIC for analog circuits.
2	PGND	PWR	Power Ground. Connects to DIMM ground plane.
1	AGND	PWR	Analog Ground. Connects to DIMM ground plane.
1	SWA	O	Switch node A output buck regulator. This pin connects to L1 power inductor. In single phase regulator mode of operation, the SWA output must not be connected to SWB output even if they are configured to same exact output voltage. In dual phase regulator mode of operation, the SWA and SWB outputs are connected.
1	SWB	O	Switch node B output buck regulator. This pin connects to L2 power inductor. In single phase regulator mode of operation, the SWA output must not be connected to either SWB output even if they are configured to same exact output voltage. In dual phase regulator mode of operation, the SWA and SWB outputs are connected.
1	SWC	O	Switch node C output buck regulator. This pin connects to L3 power inductor.
1	BOOT_SWA	PWR	Bootstrap node for SWA high side NMOS driver. This pin connects to SWA through a high quality capacitor.
1	BOOT_SWB	PWR	Bootstrap node for SWB high side NMOS driver. This pin connects to SWB through a high quality capacitor.
1	BOOT_SWC	PWR	Bootstrap node for SWC high side NMOS driver. This pin connects to SWC through a high quality capacitor.
1	SWA_FB_P	I	Switch node A output buck regulator positive feedback. In single phase or dual phase regulator mode of operation, this pin connects to DIMM power plane load.
1	SWB_FB_P	I	Switch node B output buck regulator positive feedback. In single phase regulator mode of operation, this pin connects to DIMM power plane load. In dual phase regulator mode of operation, this pin is connected to GND.
1	SWC_FB_P	I	Switch node C output buck regulator positive feedback. This pin connects to DIMM power plane load.
1	VOUT_1.8V	O	1.8V LDO Output.
1	VOUT_1.0V	O	1.0V LDO Output
1	PWR_GOOD	IO	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceeds the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin transitions from high to low. The LDO outputs shall remain on.
1	VR_EN	I	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This pin shall not be left floating. If it is not used, it shall be tied to GND.
1	SCL	I	Clock input for I ² C and I ³ C Basic bus management interface.
1	SDA	IO	Data input and output for I ² C and I ³ C Basic bus management interface.
1	GSI_n	O	General Status Interrupt. Open Drain Output. This PMIC asserts this pin low to communicate any or more events to host. This pin stays asserted until the appropriate registers are explicitly cleared and event is no longer present.
1	PID	I	PMIC ID pin for I ² C and I ³ C Basic bus.
4	NC		No Connect. This pin is not connected internally in the package to the die. Typical application connects this pin to GND on PCB for better thermal performance.

2.2 Package

2.2.1 Flip Chip QFN Package (3 mm x 4 mm)

- 28 pins (24 Functional pins; 4 dummy corner pins)
- 3 mm x 4 mm Maximum Package Outline

2.2.2 Mechanical Drawing

The drawing and dimension for 28 pins FC QFN package.

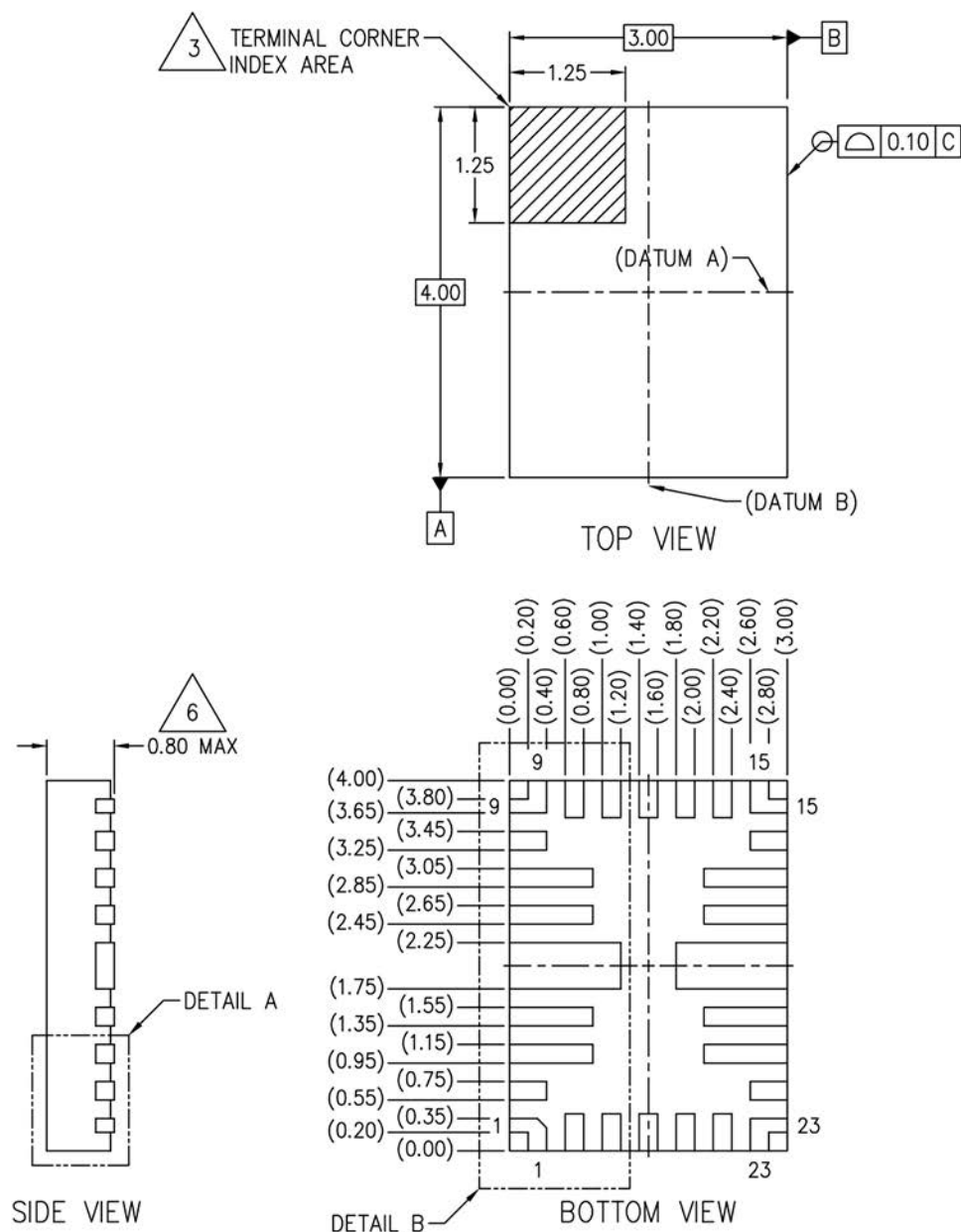


Figure 1 — QFN Package Mechanical Drawing

2.2.2 Mechanical Drawing (cont'd)

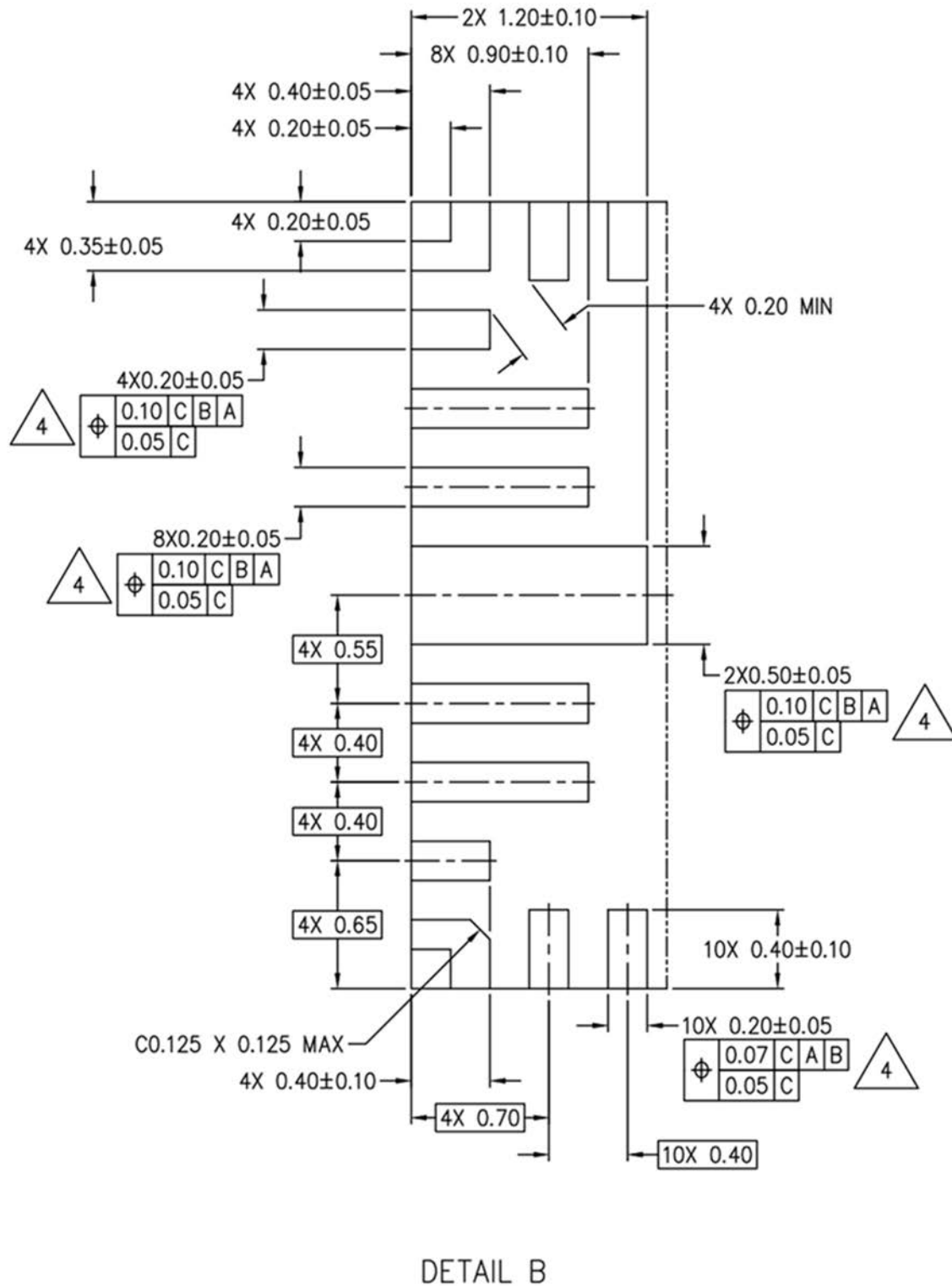


Figure 2 — QFN Package Mechanical Drawing - Detail Dimensions

2.2.2 Mechanical Drawing (cont'd)

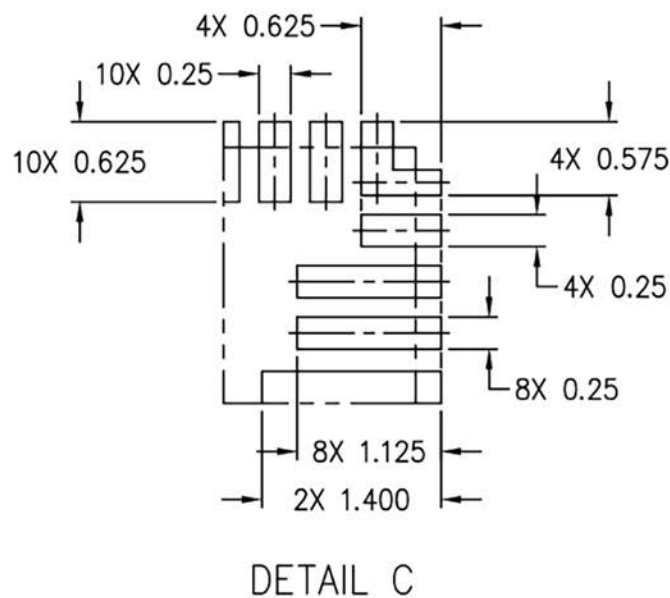
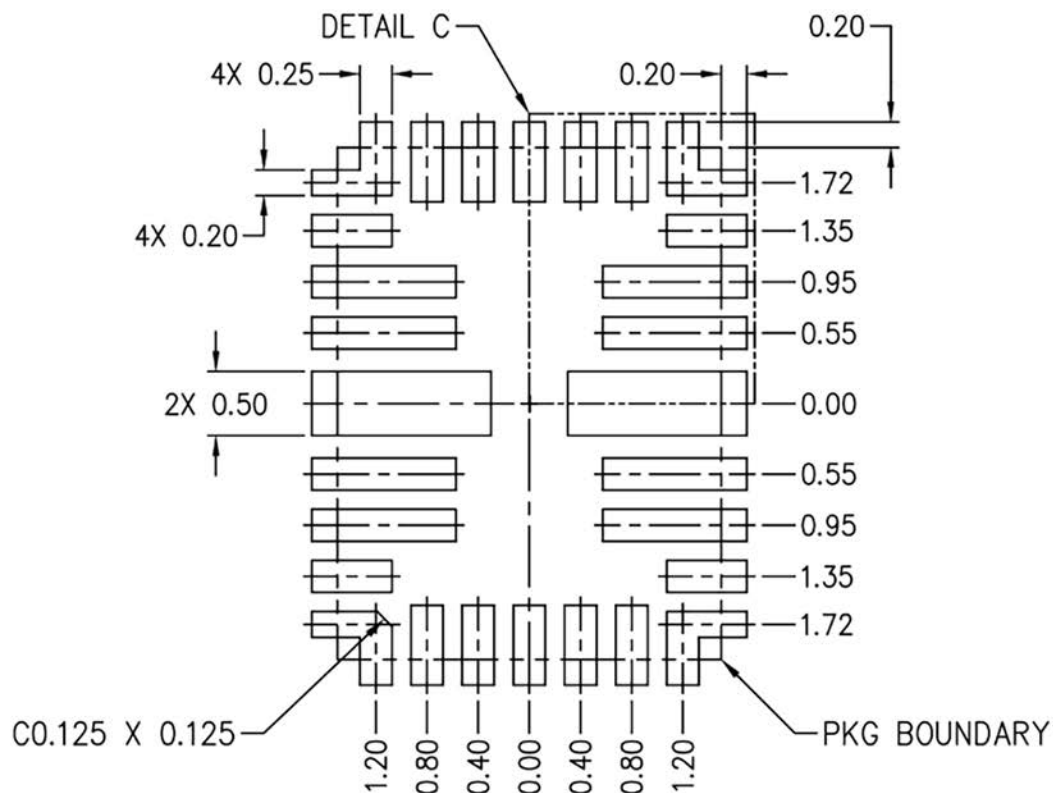


Figure 3 — Recommended PCB Pattern (Units: mm)

2.2.3 Pinout (FC QFN Package - 28 Pins)

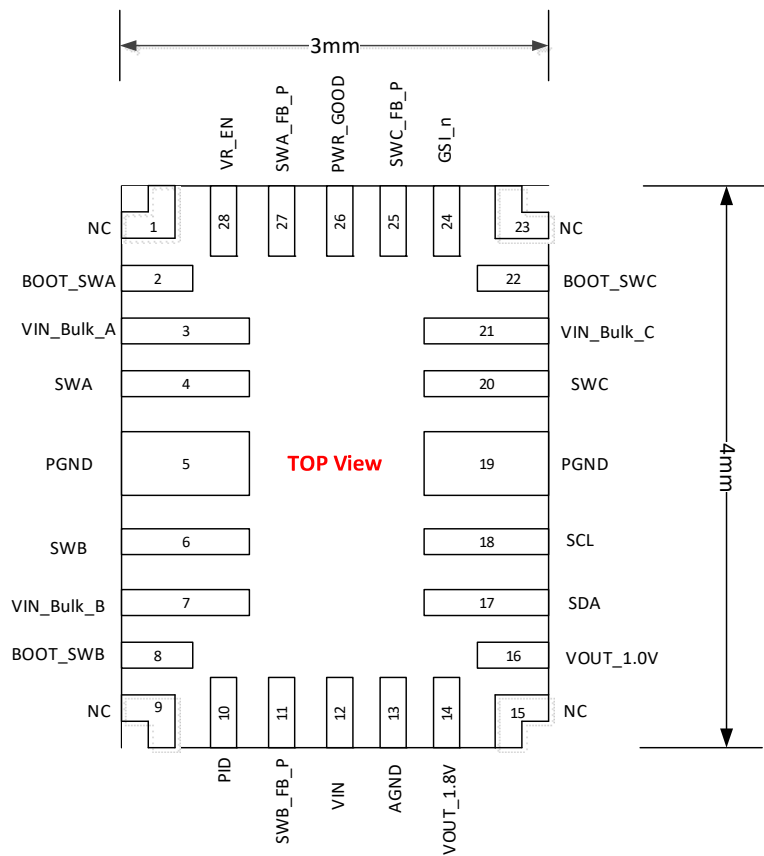


Figure 4 — FC QFN Package Pinout - 28 Pins (Top View)

2.2.3 Pinout (FC QFN Package - 28 Pins) (cont'd)

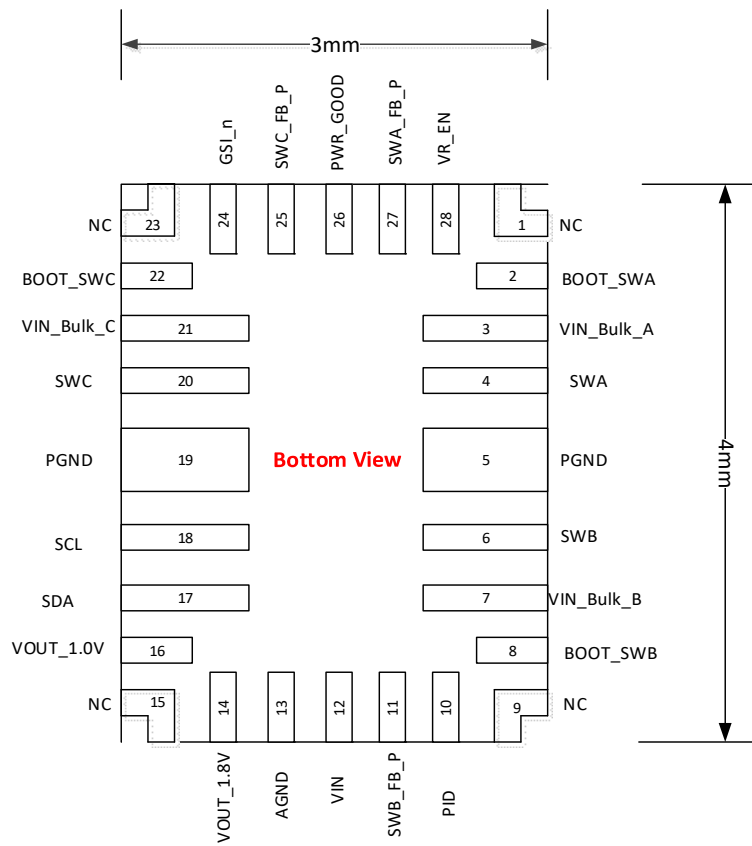


Figure 5 — FC QFN Package Pinout - 28 Pins (Bottom View)

3 Electrical Characteristics

3.1 Input Supply Electrical Characteristics

Table 2 — Input Supply DC + AC Specification¹

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Bulk Input Supply Voltage	VIN_Bulk	4.25	5.0	5.5	V	2
Bulk Input Supply Maximum AC Voltage	VIN_Bulk_AC	-	-	6.5	V	
Bulk Input Supply Voltage Ramp Up Rate	VIN_Bulk_Ramp_Up	0.1	-	3.0	V/ms	3
Bulk Input Supply Voltage Ramp Down Rate	VIN_Bulk_Ramp_Down	0.5	-	1.0	V/ms	4
Bulk Input Supply Voltage Start Up Overshoot	VIN_Bulk_OS_STARTUP	-	-	TBD	V*μs	5
Maximum Input Current for VIN_Bulk Input Supply Voltage	I _{VIN_Bulk}	0.05	-	2.0	A	6
VIN_Bulk Input Quiescent Current	I _{VIN_Bulk_Quiescent}	-	-	25	μA	7
VIN_Bulk Input Idle Current	I _{VIN_Bulk_Idle}	-	-	TBD	μA	8
NOTE 1 Input supply is referred in this table are VIN_Bulk and VIN.						
NOTE 2 During first power on, the input voltage supply must reach minimum 4.25 V for PMIC to detect valid input supply.						
NOTE 3 The ramp up rate between 300 mV and 4.0 V.						
NOTE 4 The ramp down rate between 4.0 V and 300 mV.						
NOTE 5 The area under the curve above VIN_Bulk = TBD V. VIN_Bulk_AC spec must also be satisfied.						
NOTE 6 The minimum input current requirement is to deliver the maximum output current on VOUT_1.8V and VOUT_1.0V LDO plus the current required by the PMIC for its own use. The maximum input current PMIC may see on its all VIN_Bulk input.						
NOTE 7 VIN_Bulk = 5.0 V. Measured at room temperature. All circuitry including output regulators and LDOs are off. VR_EN signal is static Low or High; GSI_n signal is pulled High. I ² C or I3C Basic interface access is not allowed and bus is pulled High. PID signal is pulled either High or Low.						
NOTE 8 VIN_Bulk = 5.0 V. Measured at room temperature. All output regulators and LDOs are on with 0 A output load. VR_EN signal is static Low or High. GSI_n signal is pulled High. I ² C or I3C Basic interface access is allowed and bus is pulled High. PID signal is pulled either High or Low						

3.2 Switch Regulator Output Electrical Characteristics

Table 3 — SWA, SWB¹ - Single Phase Regulator; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	V _{out}		1.1		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	4	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	5	A	4
Maximum Load Transient	dI/dt	-	-	7	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%	5,6
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75		0.75	%	7
NOTE 1 Only applicable if Table 164, “Register 0x4F” [0], = ‘0’.						
NOTE 2 Typical voltage configured in the register Table 121, “Register 0x21” [7:1] for SWA and Table 125, “Register 0x25” [7:1] for SWB.						
NOTE 3 Measured over long period of time. Typically 1 second.						
NOTE 4 Measured over short period of time. Typically ≥ 20 μs but less than 50 μs.						
NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, “Input Supply DC + AC Specification1”. The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV.						
NOTE 6 Applies across entire PMIC operating temperature range.						
NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 5.0V. The regulator output current load I _{tdc} = 0 A.						

Table 4 — SWA + SWB¹ - Dual Phase Regulator; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	V _{out}		1.1		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	8	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	10	A	4
Maximum Load Transient	dI/dt	-	-	14	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%	5,6
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75		0.75	%	7
NOTE 1 Only applicable if Table 164, “Register 0x4F” [0], = ‘1’.						
NOTE 2 Typical voltage configured in the register Table 121, “Register 0x21” [7:1].						
NOTE 3 Measured over long period of time. Typically 1 second.						
NOTE 4 Measured over short period of time. Typically ≥ 20 μs but less than 50 μs.						
NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, “Input Supply DC + AC Specification1”. The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV.						
NOTE 6 Applies across entire PMIC operating temperature range.						
NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 5.0 V. The regulator output current load I _{tdc} = 0 A.						

3.2 Switch Regulator Output Electrical Characteristics (cont'd)

Table 5 — SWC¹ - Single Phase Regulator; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	V _{out}		1.8		V	2
Maximum Continuous DC Current Load	I _{tdc}	0	-	1	A	3
Maximum Peak Instantaneous Current	I _{peakmax}	-	-	2	A	4
Maximum Load Transient	dI/dt	-	-	2.5	A/μs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%	5,6
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75		0.75	%	7

NOTE 1 There is no note. This is intentional.

NOTE 2 Typical voltage configured in the register Table 127, "Register 0x27" [7:1].

NOTE 3 Measured over long period of time. Typically 1 second.

NOTE 4 Measured over short period of time. Typically $\geq 20 \mu\text{s}$ but less than $50 \mu\text{s}$.

NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 2, "Input Supply DC + AC Specification1". The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and not to exceed TBD mV.

NOTE 6 Applies across entire PMIC operating temperature range.

NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 5.0 V. The regulator output current load I_{tdc} = 0 A.

3.3 LDO Output Regulator Characteristics

Table 6 — LDO Output Regulator DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1.8 V LDO Output Voltage	V _{OUT_1.8V}		1.8		V	1
1.8 V LDO Output - Maximum Output Current	I _{tdc_VOUT_1.8V}	-	-	25	mA	2
1.0 V LDO Output Voltage	V _{OUT_1.0V}		1.0		V	3
1.0 V LDO Output - Maximum Output Current	I _{tdc_VOUT_1.0V}	-	-	20	mA	4

NOTE 1 Typical voltage is configured in register Table 131, "Register 0x2B" [7:6]. The min and max values are guaranteed to be within ± 100 mV of programmed value.

NOTE 2 The maximum output current represents the external load only and excludes PMIC's own internal current consumption. The specified maximum output current is only applicable after PMIC's 1.8V LDO Power Good status is good (i.e., $t_{1.8V_Ready}$ timing parameter is satisfied). Prior to PMIC's 1.8V LDO Power Good Status (i.e., while PMIC is still ramping up the 1.8V LDO), the maximum output current shall be limited to maximum of 10 mA.

NOTE 3 Typical voltage is configured in register Table 131, "Register 0x2B" [2:1]. The min and max values are guaranteed to be within ± 50 mV of programmed value.

NOTE 4 The maximum output current represents the external load only and excludes PMIC's own internal current consumption. The specified maximum output current is only applicable after PMIC's 1.0V LDO Power Good status is good (i.e., $t_{1.0V_Ready}$ timing parameter is satisfied). Prior to PMIC's 1.0V LDO Power Good Status (i.e., while PMIC is still ramping up the 1.0V LDO), the maximum output current shall be limited to maximum of 5 mA.

3.4 I²C or I3C Basic DC and AC Electrical Characteristics

Table 7 — I²C, I3C Basic and Logic Interface DC Electrical Specification

Parameter	Symbol	Min	Max	Unit	Notes
Input Low Voltage (PWR_GOOD, SDA, SCL, VR_EN)	V _{IL}	-0.3	0.3	V	
Input High Voltage (SDA, SCL)	V _{IH}	0.7	3.6	V	
Input High Voltage (PWR_GOOD, VR_EN)		1.26	3.6	V	
Output Low Voltage (SDA)	V _{OL}	-	0.3	V	
Output Low Voltage (PWR_GOOD, GSI_n)		-	0.3	V	1
Output High Voltage (SDA)	V _{OH}	0.75	-	V	
Output Low Current (SDA)	I _{OL}	-	3	mA	
Output Low Current (PWR_GOOD, GSI_n)		-	3	mA	
Output High Current (SDA)	I _{OH}	-3	-	mA	
Rising Output Slew Rate (SDA)	Slew_Rate	0.1	1	V/ns	2
Falling Output Slew Rate (SDA)		0.1	3	V/ns	
Input Leakage Current	I _{LI}	-	± 5	μA	
Output Leakage Current	I _{LO}	-	± 5	μA	

NOTE 1 PWR_GOOD, GSI_n output is Open Drain output. There is an external pullup resistor to 1.8 V or 3.3 V on the board or other device.

NOTE 2 Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load is shown in Figure 9 and Figure 10 shows the timing measurement points. For slew rate measurement, the V_{OH} level shown in Figure 10 is a function of R_{on} value; V_{OH} = {1.0/(R_{on} + 50)} * 50.

Table 8 — Input Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Capacitance (PWR_GOOD, SCL, SDA, VR_EN)	C _{IN}	-	5	pF	

Table 9 — Input Spike Filter

Parameter	Symbol	Test Condition	Min	Max	Unit	Notes
Pulse width of spikes which must be suppressed by the input filter in I ² C mode	t _{SP}	Single glitch, f < 100 KHz	-	-	ns	
		Single glitch, f > 100 KHz	-	50	ns	1

NOTE 1 T_A = 25 °C; f = 400 KHz. Verified by design and characterization only.

Table 10 — Output Ron

Parameter	Symbol	Min	Max	Unit	Notes
SDA Output Pullup and Pulldown Driver Impedance	R _{ON}	20	100	Ω	1
GSI_n, PWR_GOOD Output Pulldown Driver Impedance		40	100	Ω	2

NOTE 1 Pulldown Ron = Vout/Iout. Pullup Ron = (VOUT_1.0V - Vout)/I

NOTE 2 Pulldown Ron = Vout/Iout

3.4 I²C or I3C Basic DC and AC Electrical Characteristics (cont'd)

Table 11 — I²C and I3C Interface AC Characteristics

Parameter	Symbol	I ² C Mode - Open Drain		I3C Basic Mode Push-Pull ¹		Unit	Notes
		Min	Max	Min	Max		
Clock Frequency	f _{SCL}	0.01	1	0.01	12.5	MHz	
Clock High Pulse Width Time	t _{High}	260		35		ns	
Clock Low Pulse Width Time	t _{Low}	500		35		ns	
Detect Clock Input Low Time	t _{TIMEOUT}	10	50	10	50	ms	
Rise Time	t _R	-	120	-	5	ns	2,3
Fall time	t _F	-	120	0	5	ns	2,3
Data in Setup Time	t _{SU:DAT}	50	-	8	-	ns	2,4
Data in Hold Time	t _{HD:DI}	0	-	3	-	ns	2,4
Start Condition Setup Time	t _{SU:STA}	260	-	12	-	ns	2
Start Condition Hold Time	t _{HD:STA}	260	-	30	-	ns	2
Stop Condition Setup Time	t _{SU:STO}	260	-	12	-	ns	2
Time between Stop Condition and next Start Condition	t _{BUF}	500	-	500	-	ns	2,5
SDA Data Out Hold Time	t _{HD:DAT}	0.5	350	N/A	N/A	ns	6
SCL Falling Clock In to Valid SDA Data Out Time	t _{DOUT}	N/A	N/A	0.5	12	ns	7,8
SCL Rising Clock In to Target SDA Output Off	t _{DOFFT}	N/A	N/A	0.5	12	ns	8,9
SCL Rising Clock In to Controller SDA Output Off	t _{DOFFC}	N/A	N/A	0.5	30	ns	8,10
SCL Rising Clock In to Controller Driving Data Signal Low	t _{CL_r_DAT_f}	N/A	N/A	40	-	ns	11
Bus Available Time (no edges seen on SCL and SDA)	t _{AVAIL}	N/A	N/A	1	-	μs	
Time to issue IBI after an event is detected when Bus is available	t _{IBI_ISSUE}	N/A	N/A	-	15	μs	
Time from Clear Register Status to any I3C operation with Start condition to avoid false IBI generation; PEC disabled	t _{CLR_I3C_CMD_Delay}	N/A	N/A	4	-	μs	
Time from Clear Register Status to any I3C operation with Start condition to avoid false IBI generation; PEC enabled		N/A	N/A	15	-	μs	
DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/Write Command Delay	t _{DEVCTRLCCC_DELAY_PEC_DIS}	3	-	3	-	μs	12,13,14

Table 11 — I²C and I3C Interface AC Characteristics (cont'd)

Parameter	Symbol	I ² C Mode - Open Drain		I3C Basic Mode Push-Pull ¹		Unit	Notes
		Min	Max	Min	Max		
Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode	$t_{WR_RD_DELAY_PEC_EN}$	N/A	N/A	8	-	μs	15,16,17
SETHID CCC or SETAASA CCC followed by any other CCC or Read/Write Command Delay	$t_{I2C_CCC_Update_Delay}$	2.5	-	N/A	N/A	μs	
RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command Delay	$t_{I3C_CCC_Update_Delay}$	-	-	2.5	-	μs	
Any CCC followed by RSTDAA CCC Delay	t_{CCC_Delay}	N/A	N/A	2.5	-	μs	
NOTE 1 I3C Basic mode with Open Drain operation follows timing values as shown in I²C Mode - Open Drain column. NOTE 2 See Figure 6 for PMIC's input timing definition. NOTE 3 See Figure 11 for voltage threshold definition for rise and fall times. NOTE 4 The input setup time is referenced from SDA VIL or VIH threshold as shown in Figure 11 to SCL VIH threshold as shown in Figure 11. The input hold time is referenced from SCL VIL threshold as shown in Figure 11 to SDA VIL or VIH threshold as shown in Figure 11. NOTE 5 If PEC is enabled, $t_{WR_RD_DELAY_PEC_EN}$ timing parameter applies. NOTE 6 The PMIC device guarantees $t_{HD:DAT}$ value in I²C mode of operation. See Figure 8 for PMIC's output timing definitions as well as SCL clock input threshold level and SDA data output threshold levels. NOTE 7 The PMIC device must be configured in I3C Basic mode to guarantee t_{DOUT} value. See Figure 7 for PMIC's output timing definition as well as SCL clock input threshold level and SDA data output threshold levels. NOTE 8 This timing parameter is guaranteed into output timing reference load as shown in Figure 9. NOTE 9 The PMIC device must be configured in I3C Basic mode to guarantee t_{DOFFT} value. See Figure 35. NOTE 10 The PMIC device must be configured in I3C Basic mode to guarantee t_{DOFFC} value. See Figure 35. NOTE 11 See Figure 38. NOTE 12 From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay. NOTE 13 The PMIC sends NACK if Host does not satisfy $t_{DEVCTRLCCC_DELAY_PEC_DIS}$ timing parameter. NOTE 14 This timing parameter restriction is only applicable when PEC function is disabled in PMIC. If PEC is enabled, this timing parameter does not apply. NOTE 15 From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay. NOTE 16 This timing parameter restriction is only applicable when PEC function is enabled in PMIC. If PEC is disabled, this timing parameter does not apply. NOTE 17 The PMIC sends NACK if Host does not satisfy $t_{WR_RD_DELAY_PEC_EN}$ timing parameter.							

The PMIC device follow the I²C bus and I3C Basic bus input timing requirements as shown in Figure 6 and Table 11 and output timing requirement as shown in Figure 7

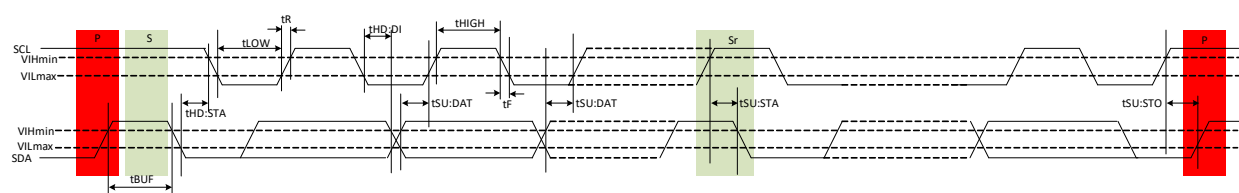


Figure 6 — I2C or I3C Basic Bus AC Input Timing Parameter Definition

3.4 I2C or I3C Basic DC and AC Electrical Characteristics (cont'd)

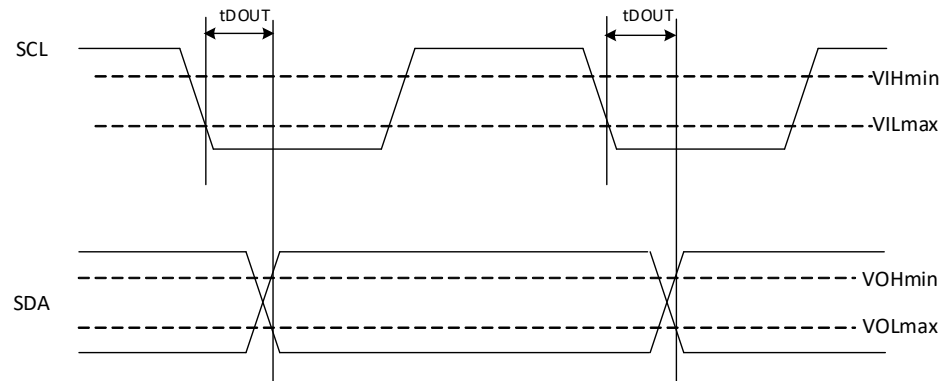


Figure 7 — I3C Basic Bus AC Output Timing Parameter Definition

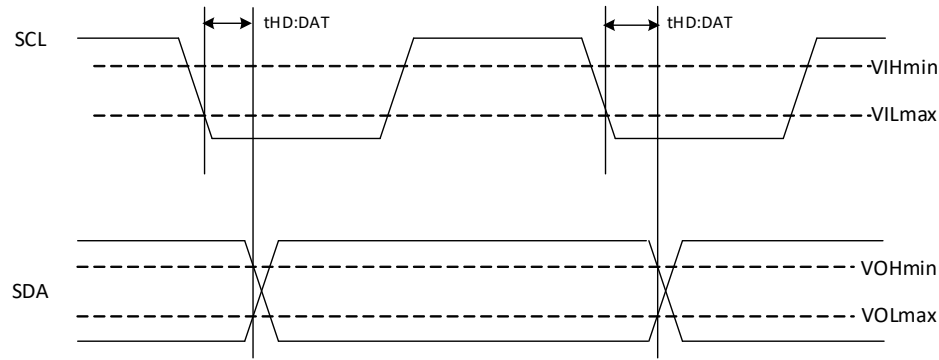


Figure 8 — I²C Bus AC Output Timing Parameter Definition

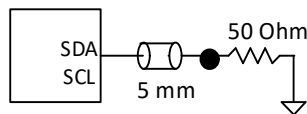


Figure 9 — Output Slew Rate and Output Timing Reference Load

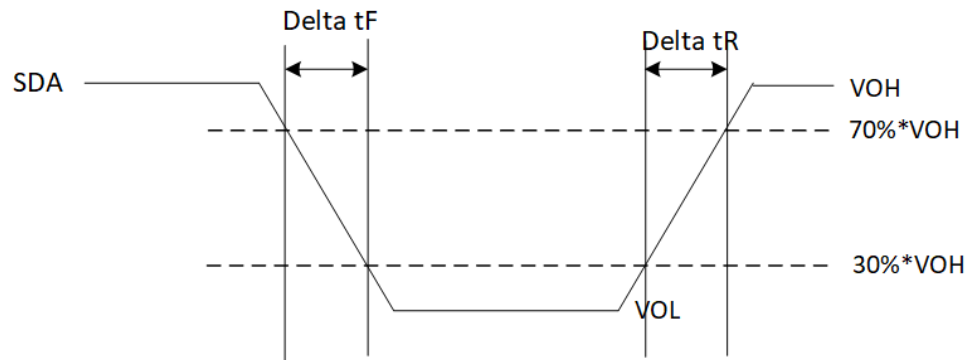


Figure 10 — Output Slew Rate Measurement Points

3.4 I²C or I³C Basic DC and AC Electrical Characteristics (cont'd)

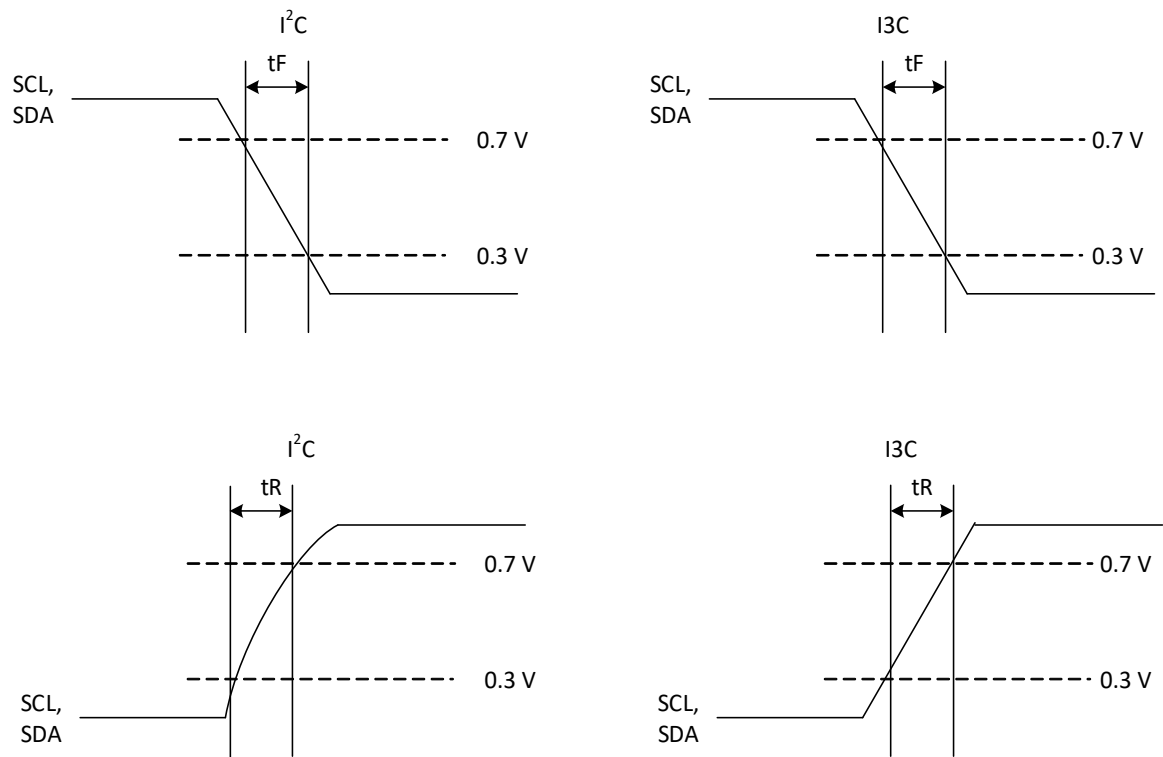


Figure 11 — Input Rise and Fall Timing Parameter Definition

3.5 Measurement Condition

Table 12 — AC Measurement Conditions¹

Symbol	Parameter	Min	Max	Units
C _L	Load capacitance		40	pF
	Input rise and Fall times - Open Drain	-	TBD	ns
	Input rise and fall times - Push Pull	-	TBD	ns
	Input signal swing levels	0.2 to 0.8		V
	Input levels for timing reference	0.3 to 0.7		V
NOTE 1 This AC measurement condition (Table 12 and Figure 12) is only for the test purpose in lab.				

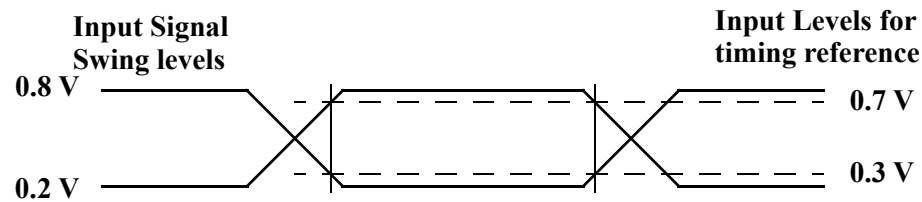


Figure 12 — AC Measurement Waveform

3.6 PMIC AC Timing Parameters

Table 13 — PMIC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Supply to GSI_n assertion	tInput_PWR_GOOD_GSI_Assertion			10	μs	
Input over voltage condition to GSI_n assertion	tInput_OV_GSI_Assertion	-	-	10	μs	
Input over voltage condition to automatic PMIC VR Disable	tInput_OV_VR_Disable	-	-	20	μs	
Output Voltage Tolerance to GSI_n assertion	tOutput_PWR_GOOD_GSI_Assertion	-	-	10	μs	
Output over voltage condition to automatic PMIC VR Disable	tOutput_OV_VR_Disable	-	-	20	μs	
Output under voltage lockout condition to automatic PMIC VR Disable	tOutput_UV_VR_Disable	-	-	20	μs	
Output current limiter Warning to GSI_n assertion	tOutput_Current_Limiter	-	-	10	μs	
High Temperature Warning to GSI_n assertion	tHigh_Temp_Warning	-	-	10	μs	
Critical Temperature condition to automatic PMIC shut down	tShut_Down_Temp	-	-	10	μs	
VIN_Bulk input supply stable to VR Enable Command	tVIN_Bulk_to_VR_Enable	6.5	-	-	ms	
VIN_Bulk input supply stable to VOUT_1.8V output stable	t1.8V_Ready	-	-	2.5	ms	
VOUT_1.8V output supply stable to VOUT_1.0V output stable	t1.0V_Ready	-	-	1.0	ms	1
VOUT_1.8V output supply to PMIC Management Ready	tManagement_Ready	-	-	3	ms	
VR Enable Command to PMIC output regulator ready	tPMIC_PWR_Good_Out	Figure 25			ms	
VR Disable Command to PMIC Output Regulators Off	tPMIC_Output_Off	Figure 33			ms	
PWR_GOOD Input Low Pulse Width	tPWR_GOOD_Low_Pulse_Width	2	0	0	μs	
PWR_GOOD Input Low Pulse Width Input Filter	tPWR_GOOD_Low_Pulse_Width_Filter	-	-	0.35	μs	
Output Voltage Adjustment in Programmable Mode	Δv/Δt	-	1	-	mV/μs	2
NOTE 1 This time is added to t1.8V_Ready parameter to get total time from VIN_Bulk input supply.						
NOTE 2 See footnote 4 for registers Table 121, “Register 0x21” [7:1], Table 125, “Register 0x25” [7:1], and Table 127, “Register 0x27” [7:1]. The accuracy is ± 10%.						

3.7 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed in Table 14, “Absolute Maximum Rating” and Table 15, “ESD Requirement” and Table 16, “EOS Requirement” may cause permanent damage to the device. Functional operation of the DDR5 PMIC at absolute maximum ratings is not implied. Exposure to absolute maximum rating condition for extended periods may affect long term reliability.

Table 14 — Absolute Maximum Rating

Pin	Maximum Rating		Unit
	DC	AC	
VIN_BULK, VIN	-0.3 to 6	TBD (Duration $\leq$ 25 ns)	V
VOUT_1.8V, VOUT_1.0V	-0.3 to 2.2	-	V
SWA, SWB, SWC	-0.3 to 6	-3 to 9 (Duration < 25 ns)	V
BOOT_SWA, BOOT_SWB, BOOT_SWC (to GND)	-0.3 to 12	-0.3 to 15 (Duration < 25 ns)	V
BOOT_SWA, BOOT_SWB, BOOT_SWC (to SWx)	-0.3 to 6	TBD	V
SWA_FB_P, SWB_FB_P, SWC_FB_P (to AGND)	-0.3 to 2.2	-	V
PWR_GOOD, GSI_n, VR_EN	-0.3 to 5.0	-	V
SCL, SDA; I ² C Mode only	-0.3 to 5.0		
SCL, SDA; I ³ C Mode only	-0.3 to 2.1		
PID	-0.3 to 2.2	TBD	V
AGND, PGND	-0.3 to 0.3	-	V

3.8 ESD Requirements

Table 15 — ESD Requirement

Test Model	Pin	Maximum Rating	Unit
HBM	All	$\pm$ 2000	V
CDM	All	$\pm$ 500	V

Table 16 — EOS Requirement

Pin	Maximum Rating	Unit	Notes
VIN_BULK	10	V	1,2,3,4
NOTE 1 The test is performed on DDR5 DIMM module without any input capacitor on VIN_BULK			
NOTE 2 The input source needs to follow the waveform and condition as shown in Figure 13 and Table 17.			
NOTE 3 Probing is performed at the VIN_BULK pin of PMIC.			
NOTE 4 Applies to VIN_Bulk and VIN pin.			

Table 17 — Input Source Condition

Item	Value	Notes
T (rise from 30% to 90% of peak)	0.72 μ s (+ 30%)	
T1 (rise time)	1.2 μ s (+ 30%)	T1 = 1.67*T
T2 (duration time to half value)	50 μ s (+ 20%)	
Output Impedance	2 Ω	
V_UNDERSHOOT Voltage	30 % Max	

3.8 ESD Requirements (cont'd)

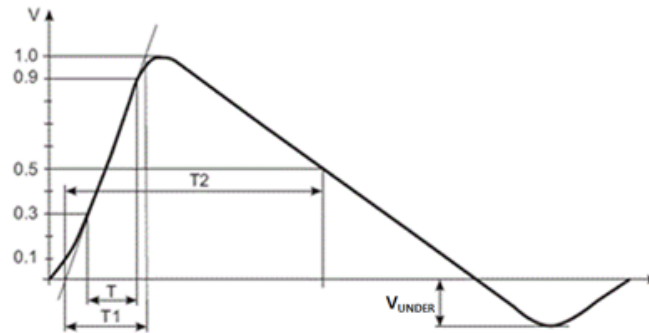


Figure 13 — Impulse Waveform for EOS Test (IEC 61000-4-5)

3.9 Thermal Characteristics

Table 18 — Thermal Characteristics

Parameter	Symbol	Maximum Rating	Unit	Notes
Thermal resistance junction to case	Θ_{JC}	TBD	$^{\circ}\text{C}/\text{W}$	1,2,3
Junction operating temperature	T_J	-10 to 125	$^{\circ}\text{C}$	
Case operating temperature	T_C	-10 to TBD	$^{\circ}\text{C}$	3
Storage temperature	T_{STG3}	-55 to 150	$^{\circ}\text{C}$	3
Lead temperature (soldering, 10 s)	T_{LEAD}	260	$^{\circ}\text{C}$	3
NOTE 1 The maximum power dissipation is $P_{D(MAX)} = (T_{JMAX} - T_C) / \Theta_{JC}$. Exceeding the maximum allowable power dissipation results in excessive die temperature and the device will enter thermal shutdown.				
NOTE 2 This thermal rating was calculated on JEDEC 51 standard 4 layer board with dimensions 3" x 4.5" in still air conditions. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.				
NOTE 3 This specification is compliant with JESD402-1 Temperature Grade and Measurement Standard for Components and Modules, operating temperature range MT, storage temperature range T_{STG3} . See JESD402-1 for details, including measurement point.				

4 Performance Characteristics

4.1 Efficiency

4.1.1 Efficiency with Inductor Footprint

Table 19 — Efficiency Characteristics¹

Switch Node Output	Efficiency	Efficiency (% of Max Itdc Load)				Unit	Notes
	Light Load ²	25%	50%	75%	100%		
SWA or SWB (Single Phase Regulator Mode)	83	≥ 90	≥ 88	≥ 85	≥ 82	%	3,4,5,6,7,8, 9,10,11,12
SWA + SWB (Dual Phase Regulator Mode)	83	≥ 90	≥ 88	≥ 85	≥ 82	%	
SWC	85	≥ 90	≥ 89	≥ 87	≥ 85	%	
NOTE 1 The efficiency numbers assume the inductor specification as noted in Clause 4.2.							
NOTE 2 Light Load is defined as 100 mA for SWA and SWB for single phase regulator mode; 200 mA for SWA+SWB for dual phase regulator mode; 50 mA for SWC.							
NOTE 3 VIN_Bulk = 5 V							
NOTE 4 The maximum Itdc as specified in Table appropriately.							
NOTE 5 When the efficiency of any given output regulator is being measured, all other switching output regulators are disabled.							
NOTE 6 No external load on VOUT_1.8V, VOUT_1.0V LDO is applied.							
NOTE 7 I ² C/I ² C Basic bus is pulled High and held static. PWR_GOOD and GSI_n signals are pulled High and held static.							
NOTE 8 The efficiency includes the buck regulator loss, the PCB loss (< 4 mΩ or less). See Clause 4.2 for inductor specification assumption for DCR and ACR.							
NOTE 9 Efficiency calculation equation: (V _{OUT} * I _{OUT}) / [(V _{IN_Bulk} * I _{VIN_Bulk})+(V _{IN} * I _{VIN})]; where V _{OUT} , I _{OUT} , V _{IN_Bulk} , I _{VIN_Bulk} , V _{IN} , I _{VIN} parameters are actual measured values.							
NOTE 10 Applies at maximum ambient temperature of 65 °C (PMIC Junction temperature of 105 °C). The DCR characteristics noted above applies inductor temperature of 105 °C.							
NOTE 11 The output buck regulator switching frequency can be set to 750 KHz.							
NOTE 12 For input supply rail, probing is done at the input high frequency filter cap (0.1 uF) to PMIC pin. For output rail, probing is done at the output cap location at the inductor load side.							

4.2 Inductor Specification

4.2.1 Mechanical Specification

The inductor package dimensions and its recommended land patterns are defined in Table 20.

Table 20 — Inductor Mechanical Specification; SWA, SWB

Package Size		Reference Drawing	Recommended Land Pattern
L (mm)	3.4 Max	Figure 14 (Left Picture)	Figure 14 (Right Picture)
W (mm)	3.2 Max		
H (mm)	1.2 Max		

4.2.1 Mechanical Specification (cont'd)

Table 21 — Inductor Mechanical Specification; SWC

Package Size		Reference Drawing	Recommended Land Pattern
L (mm)	2.7 Max	Figure 15 (Left Picture)	Figure 15 (Right Picture)
W (mm)	2.2 Max		
H (mm)	1.2 Max		

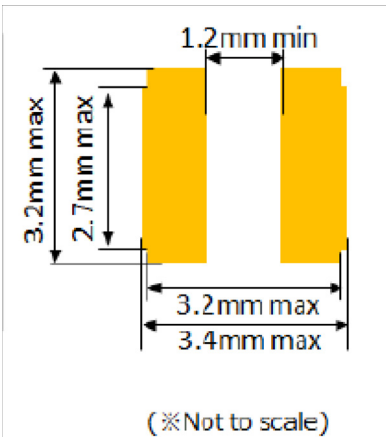
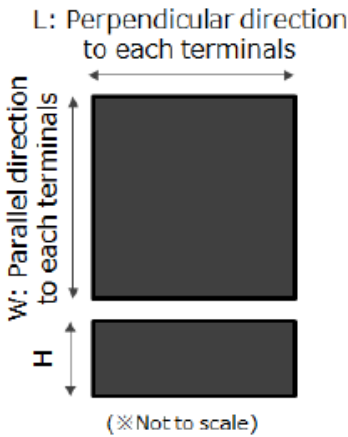


Figure 14 — Reference Drawing and Recommended Land Pattern; SWA, SWB

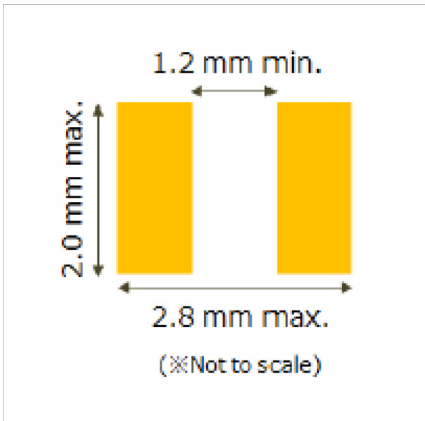
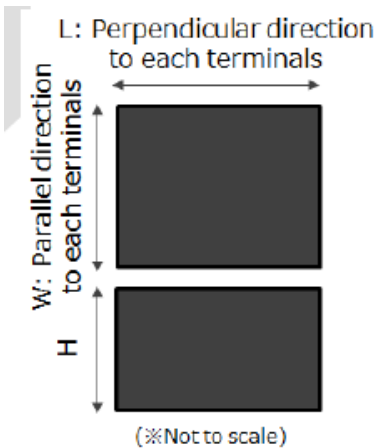


Figure 15 — Reference Drawing and Recommended Land Pattern; SWC

4.2.2 Electrical Specification

The inductor electrical specifications are defined in Table 22 and Table 23.

Table 22 — Inductor Electrical Specification; SWA, SWB¹

Package Height (mm)	L @ 0.5-1 MHz; 0 Bias (μH)	Max DCR (mΩ)	Max ACR @ 1 MHz ^{2,3} (mΩ)	Min L @ 6 A (Ipeakmax of ⁴ (μH)
1.2 Max	0.47 ± 20%	14.5	93	0.30
	0.68 ± 20%	18.5	113	0.38
NOTE 1 Test condition: Ambient Temperature = 20 ± 2 °C; Ambient Humidity = 65 ± 5% Rh NOTE 2 ACR definition: ACR = Rs @ 1 MHz - DCR. Measured current (1 MHz/sinusoidal): 0.49 A rms for 0.47 μH, 0.34 A rms for 0.68 μH; with no DC Bias for all cases. NOTE 3 For Rs measurement, it is recommended to measure by Iwatsu SY-8218 (BH Analyzer, with NF IE-1125B), its upper compatible instruments or other instruments which is guaranteed on the measurement accuracy by inductor vendors. NOTE 4 Minimum inductance is defined at DC bias current given by definition in Ipeakmax; Table 3, Table 4, and Table 5.				

Table 23 — Inductor Electrical Specification; SWC¹

Package Height (mm)	L @ 0.5-1 MHz; 0 Bias (μH)	Max DCR (mΩ)	Max ACR @ 1 MHz ^{2,3} (mΩ)	Min L @ 2 A (Ipeakmax of ⁴ (μH)
1.2 Max	1.0 ± 20%	48.0	182	0.56
	1.5 ± 20%	75.0	300	0.82
NOTE 1 Test condition: Ambient Temperature = 20 ± 2 °C; Ambient Humidity = 65 ± 5% Rh NOTE 2 ACR definition: ACR = Rs @ 1 MHz - DCR. Measured current (1 MHz/sinusoidal): 0.33A rms for 1.0 μH, 0.22A rms for 1.5 μH; with no DC Bias for all cases. NOTE 3 For Rs measurement, it is recommended to measure by Iwatsu SY-8218 (BH Analyzer, with NF IE-1125B), its upper compatible instruments or other instruments which is guaranteed on the measurement accuracy by inductor vendors. NOTE 4 Minimum inductance is defined at DC bias current given by definition in Ipeakmax; Table 3, Table 4, and Table 5.				

5 DDR5 DIMM Schematic

Figure 16 shows an example schematic when PMIC is configured in dual phase regulator mode. Table 24, “PMIC Schematic Values” shows all component details shown in the schematics. Note that capacitors C25, C26, and C27 represent the lump sum of distributed capacitance across the entire DIMM.

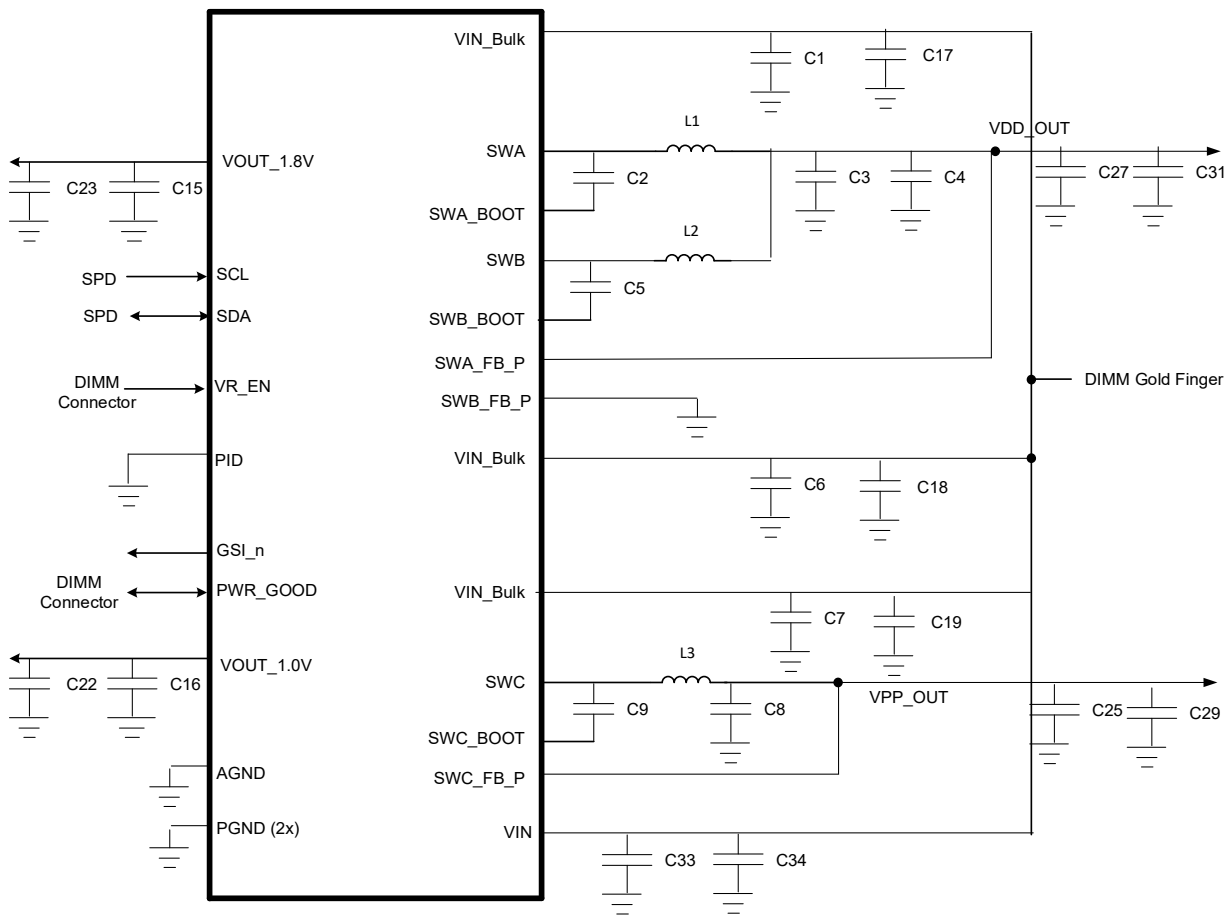


Figure 16 — Dual Phase Regulator - DDR5 DIMM Schematic

5 DDR5 DIMM Schematic (cont'd)

Figure 17 shows an example schematic when PMIC is configured in single phase regulator mode. Table 24, “PMIC Schematic Values” shows all component details shown in the schematics. Note that capacitors C25, C26, C27, and C28 represent the lump sum of distributed capacitance across the entire DIMM.

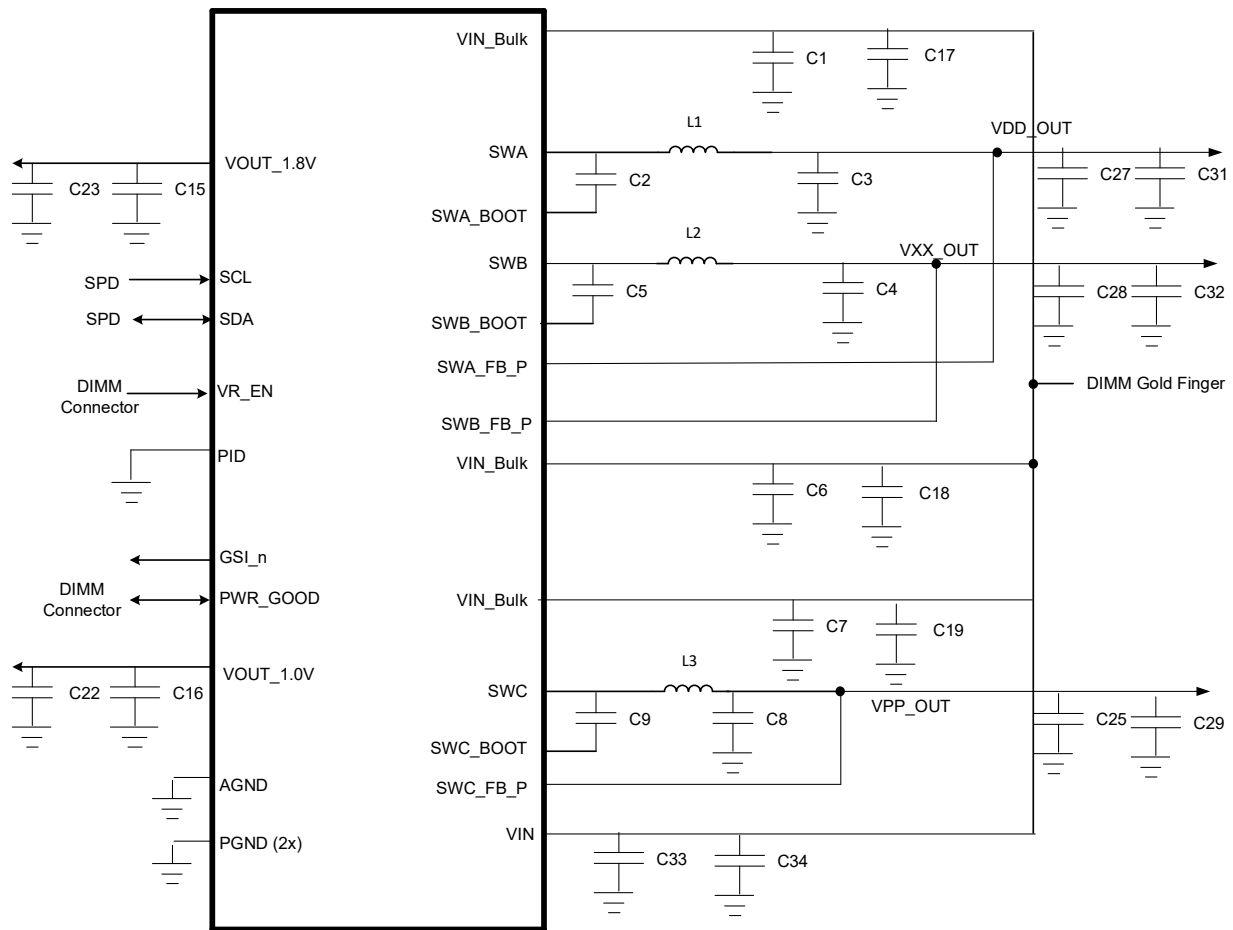


Figure 17 — Single Phase Regulator - DDR5 PMIC Schematic

5 DDR5 DIMM Schematic (cont'd)

Table 24 — PMIC Schematic Values

Component	Dual Phase Regulator Mode		Single Phase Regulator Mode		Unit	Comment
	Value	Physical Size	Value	Physical Size		
L1	0.68	3.2 mm x 3.2 mm x 1.2 mm	0.68	3.2 mm x 3.2 mm x 1.2 mm	μH	1
L2	0.68	3.2 mm x 3.2 mm x 1.2 mm	0.68	3.2 mm x 3.2 mm x 1.2 mm	μH	1
L3	1.5	2.7 mm x 2.2 mm x 1.2 mm	1.5	2.7 mm x 2.2 mm x 1.2 mm	μH	2
C1	22 (2x)	10 V	22 (2x)	10 V	μF	
C2	0.1	10 V; 0201	0.1	10 V; 0201	μF	
C3	47 (2x)	6.3 V; 0603	47 (2x)	6.3 V; 0603	μF	
C4	47 (2x)	6.3 V; 0603	47 (2x)	6.3 V; 0603	μF	
C5	0.1	10 V; 0201	0.1	10 V; 0201	μF	
C6	22 (2x)	10 V	22 (2x)	10 V	μF	
C7	22 (2x)	10 V	22 (2x)	10 V	μF	
C8	47 (2x)	6.3 V; 0603	47 (2x)	6.3 V; 0603	μF	
C9	0.1	10 V; 0201	0.1	10 V; 0201	μF	
C15	4.7	6.3 V; 0402	4.7	6.3 V; 0402	μF	
C16	4.7	6.3 V; 0402	4.7	6.3 V; 0402	μF	
C17	0.1	10 V; 0201	0.1	10 V; 0201	μF	
C18	0.1	10 V; 0201	0.1	10 V; 0201	μF	
C19	0.1	10 V; 0201	0.1	10 V; 0201	μF	
C22	0.1	6.3 V; 0201	0.1	6.3 V; 0201	μF	
C23	0.1	6.3 V; 0201	0.1	6.3 V; 0201	μF	
C33	0.1	10 V; 0201	0.1	10 V; 0201	μF	
C34	4.7	10 V; 0402	4.7	10 V; 0402	μF	
C25	75	6.3 V	75	6.3 V	μF	3
C27	350	6.3 V	175	6.3 V	μF	
C28	N/A	N/A	175	6.3 V	μF	
C29	75	6.3 V	75	6.3 V	μF	3
C31	350	6.3 V	175	6.3 V	μF	
C32	N/A	N/A	175	6.3 V	μF	
NOTE 1	The usage of 0.47 μH inductor may be allowed by the PMIC vendor.					
NOTE 2	The usage of 1.0 μH inductor may be allowed by the PMIC vendor.					
NOTE 3	These capacitor values represent the distributed capacitance for the entire DIMM assuming max I _{tdc} and I _{peakmax} defined in Electrical Characteristics for each SWx. For a given DIMM design, the distributed capacitance for each SWx varies and is a function of I _{tdc} and I _{peakmax} current requirement for that DIMM design. See actual DIMM design for total distributed capacitance.					

5 DDR5 DIMM Schematic (cont'd)

Figure 18 and Figure 19 show PMIC and passive component layout example for DDR5 SODIMM and DDR5 UDIMM. This layout is for reference and final layout may vary.

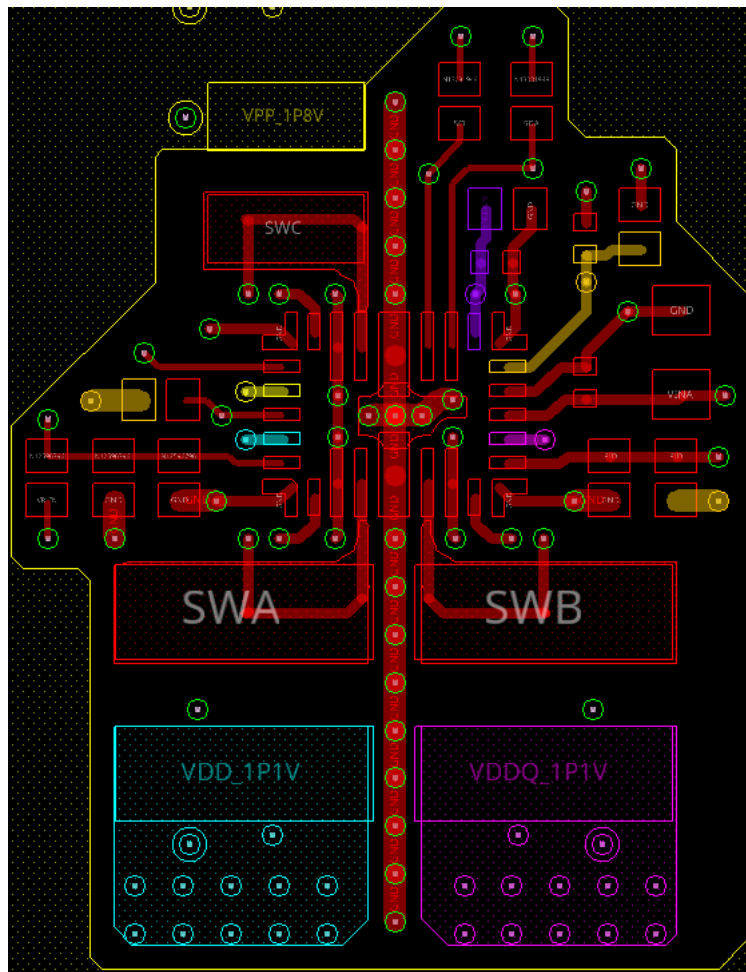


Figure 18 — DDR5 DIMM PMIC Layout Example - Top Layer

5 DDR5 DIMM Schematic (cont'd)

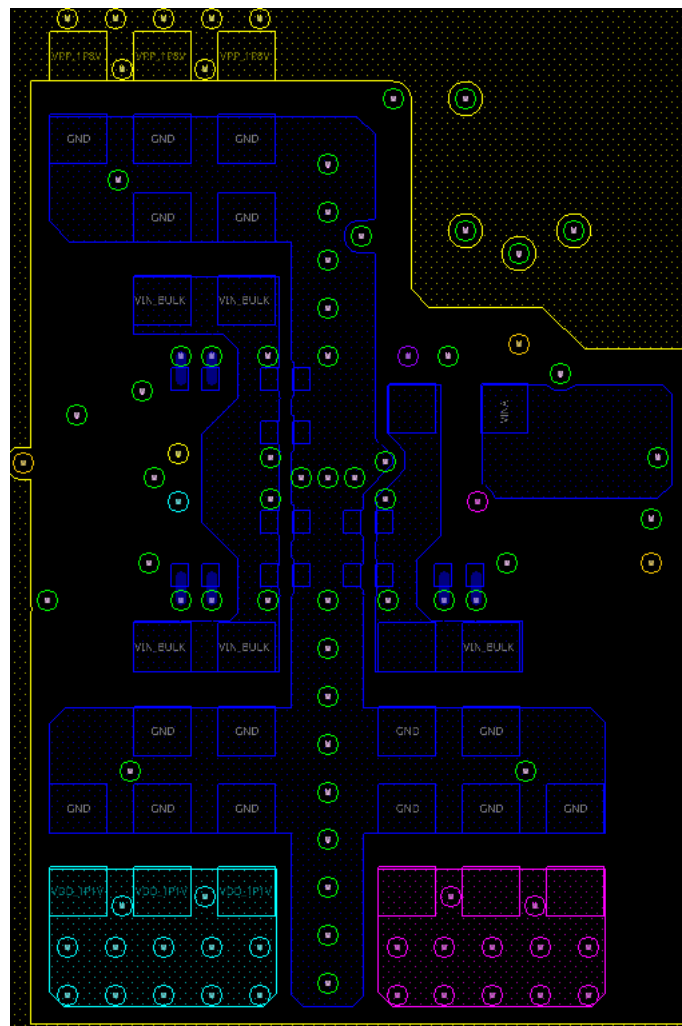


Figure 19 — DDR5 DIMM PMIC Layout Example - Bottom Layer

6 Functional Operation

6.1 PMIC Input Voltage Supply and Ramp Condition

The DDR5 PMIC has one input supply from the platform: VIN_Bulk.

The VIN_Bulk supply is used by the PMIC for all three switch (SWA, SWB, SWC) output regulators and two LDO outputs (VOUT_1.8V and VOUT_1.0V) regulators. Note that the VOUT_1.8V LDO output is separate and independent from SWC output, which is for the DRAM VPP rail. The VOUT_1.0V LDO output is separate and independent from SWA or SWB.

At first power on, the VIN_Bulk input supply shall reach a minimum threshold voltage of 4.25 V before it can be detected as a valid input supply to the PMIC.

Once the VIN_Bulk supply is valid and stable, the PMIC shall assert PWR_GOOD output low, drive VOUT_1.8V and VOUT_1.0V supply within $t_{1.8V_Ready}$ and $t_{1.0V_Ready}$ time respectively. The PMIC drives PWR_GOOD output signal low only when VIN_Bulk input supply reaches minimum of 4.25 V. The PWR_GOOD output is pulled up to either 1.8 V or 3.3 V on the platform or on the host controller.

The PWR_GOOD pullup voltage (either 1.8 V or 3.3 V) can be available before or after VIN_Bulk is valid and stable. If PWR_GOOD pullup voltage is available before VIN_Bulk is applied, the PWR_GOOD signal is High and remains High with no leakage path or damage to the PMIC. When VIN_Bulk is applied to the PMIC, the PMIC asserts PWR_GOOD output low.

The PMIC shall enable I²C/I3C bus interface function within tManagement_Ready. The host shall not attempt to access the PMIC's memory registers until tManagement_Ready timing requirement is satisfied.

6.2 Power Up Initialization Sequence

During power on, the host shall:

1. Ramp up VIN_Bulk supply.
2. Hold VIN_Bulk supply stable for a minimum of tVIN_Bulk_to_VR_Enable time.
3. Hold VR_EN pin to static low or high. There is no timing relationship required on VR_EN pin with respect to VIN_Bulk input supply ramp up as long as VR_EN pin is held to static level to either low or high.
4. During VIN_Bulk ramp, if VR_EN signal is held low, it can transition to high only once. Once high, it shall remain high. The VR_EN signal is not allowed to transition to low during VIN_Bulk ramp up.
5. If VR_EN pin is held High during VIN_Bulk ramp up or transitions to High during VIN_Bulk ramp up, the PMIC turns on its output rails.
6. If VR_EN pin is held Low during VIN_Bulk Ramp, assert VR_EN signal High to turn on PMIC output rails. Alternatively, host can issue VR Enable command by setting register Table 138, "Register 0x32" [7] = '1' via I²C/I3C Basic bus or via DEVCTRL CCC to turn on PMIC output rails.

6.2.1 Power Up Sequence

Figure 20 to Figure 23 show examples of PMIC power up initialization sequence. Note that the specific sequence of ramping the output regulators (SWA, SWB, SWC) is for example purpose only. The specific ramp up sequence is configurable through power on sequence configuration registers.

After VR Enable command is registered on the I²C or I3C Basic bus or VR_EN pin is registered high, the PMIC shall complete the following steps within tPMIC_PWR_GOOD_OUT:

1. Check VIN_Bulk Power Good status is valid.
2. Power up itself - PMIC executes Power On Sequence Config 0 (Table 149, “Register 0x40”) to Power On Sequence Config 2 (Table 151, “Register 0x42”) registers and configures PMIC internal registers as programmed in DIMM vendor memory space registers.
3. Power up all enabled output switch regulators and ready for normal operation
4. Update status registers Table 96, “Register 0x08” [5,3:2] and floats PWR_GOOD signal within maximum of tPMIC_PWR_GOOD_OUT time.

If PMIC PWR_GOOD signal is not floated within tPMIC_PWR_GOOD_OUT time, the host can access the PMIC status registers for detailed information after tPMIC_PWR_GOOD_OUT time. The PMIC may NACK for any host request on I²C or I3C Basic bus after VR Enable command (either with VR_EN pin high or on I²C/I3C Basic Bus) until tPMIC_PWR_GOOD_OUT time expires.

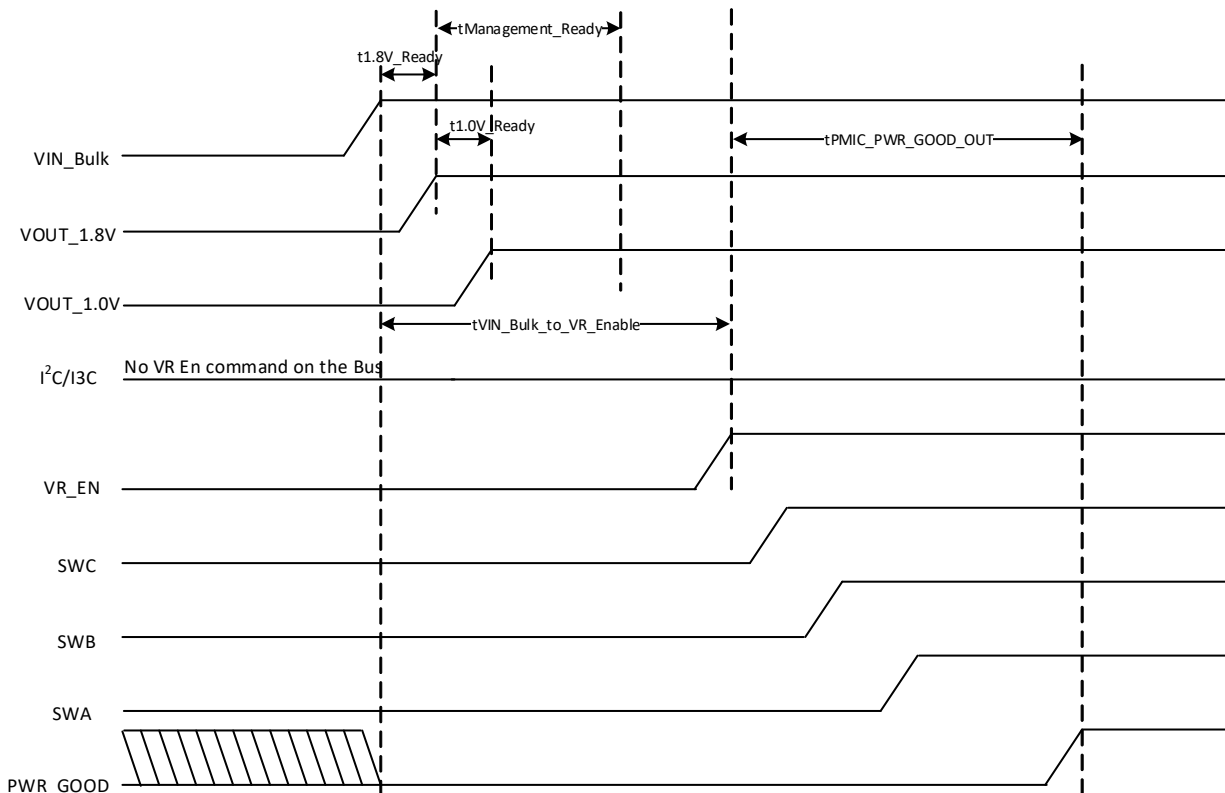


Figure 20 — Power Up Sequence; VR_EN Pin High after VIN_Bulk Ramp; No Bus Command

6.2.1 Power Up Sequence (cont'd)

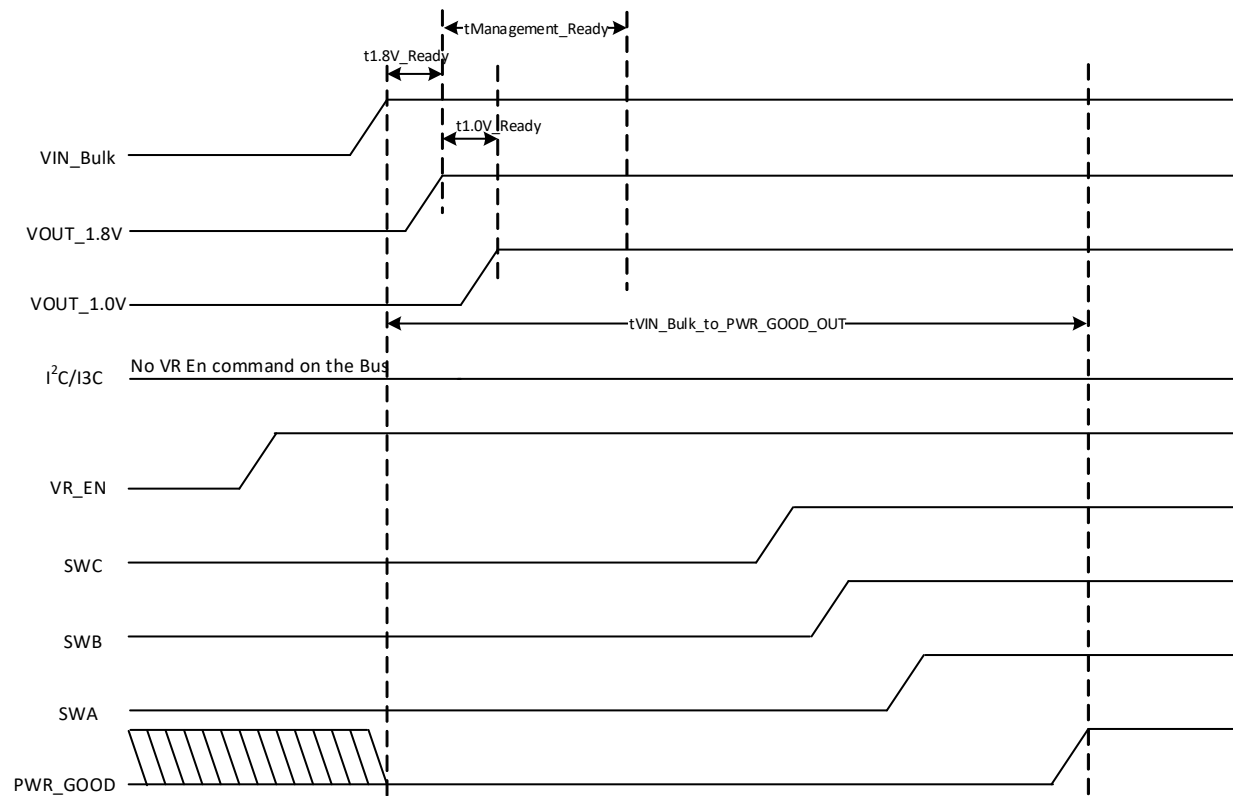


Figure 21 — Power Up Sequence; VR_EN Pin High before VIN_Bulk Ramp; No Bus Command

6.2.1 Power Up Sequence (cont'd)

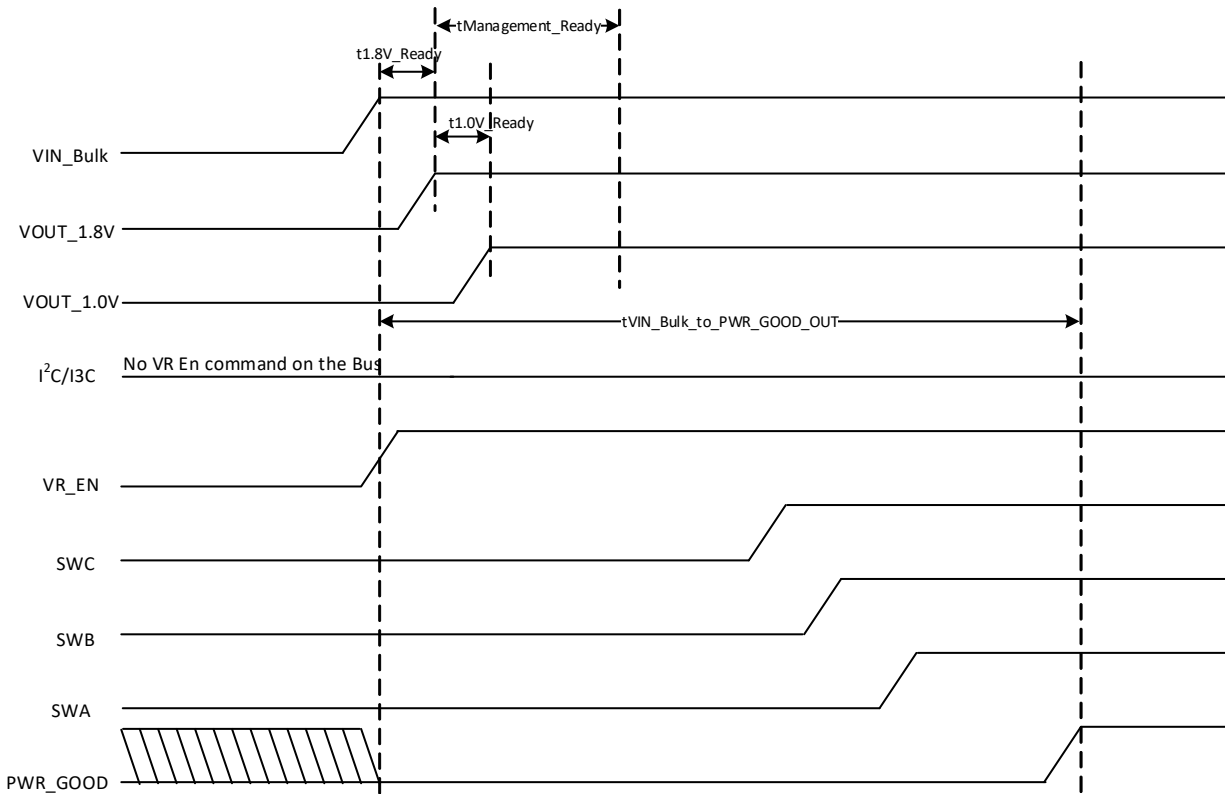


Figure 22 — Power Up Sequence; VR_EN Pin High during VIN_Bulk Ramp; No Bus Command

6.2.1 Power Up Sequence (cont'd)

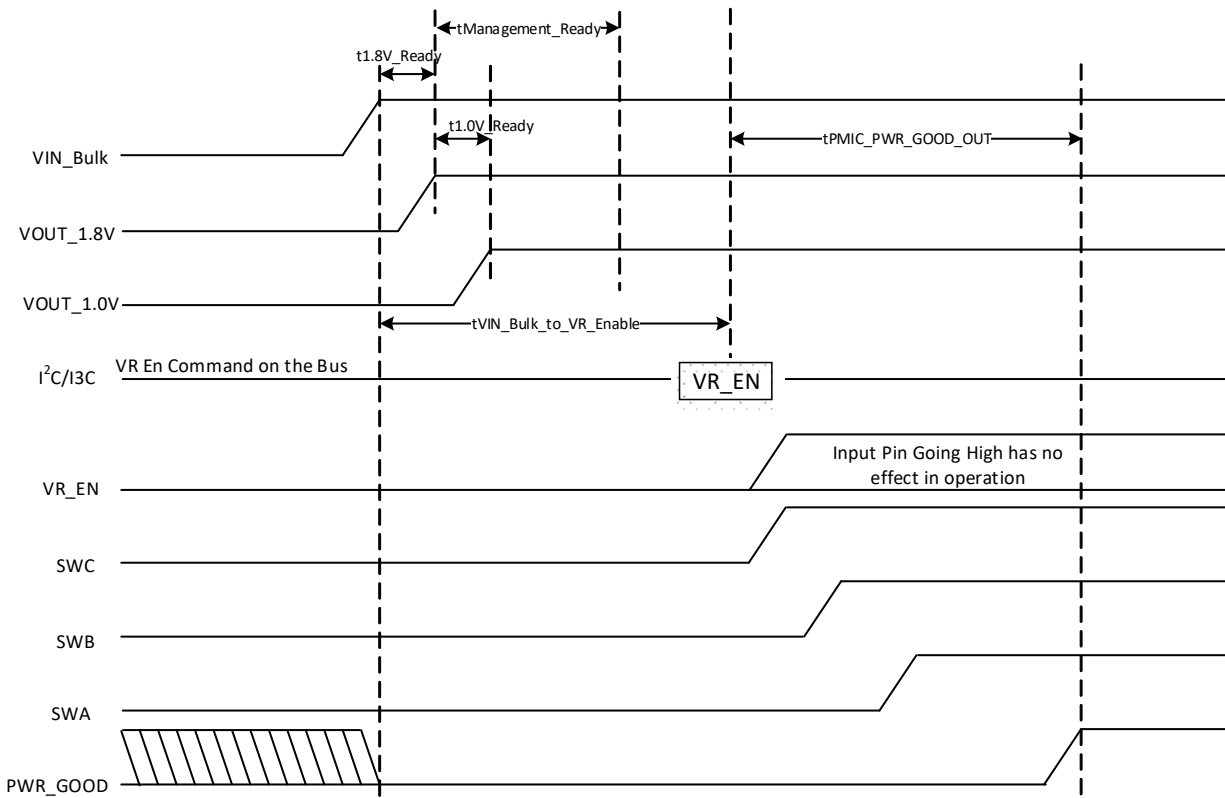


Figure 23 — PMIC Power Up Sequence; with Bus Command

6.2.1 Power Up Sequence (cont'd)

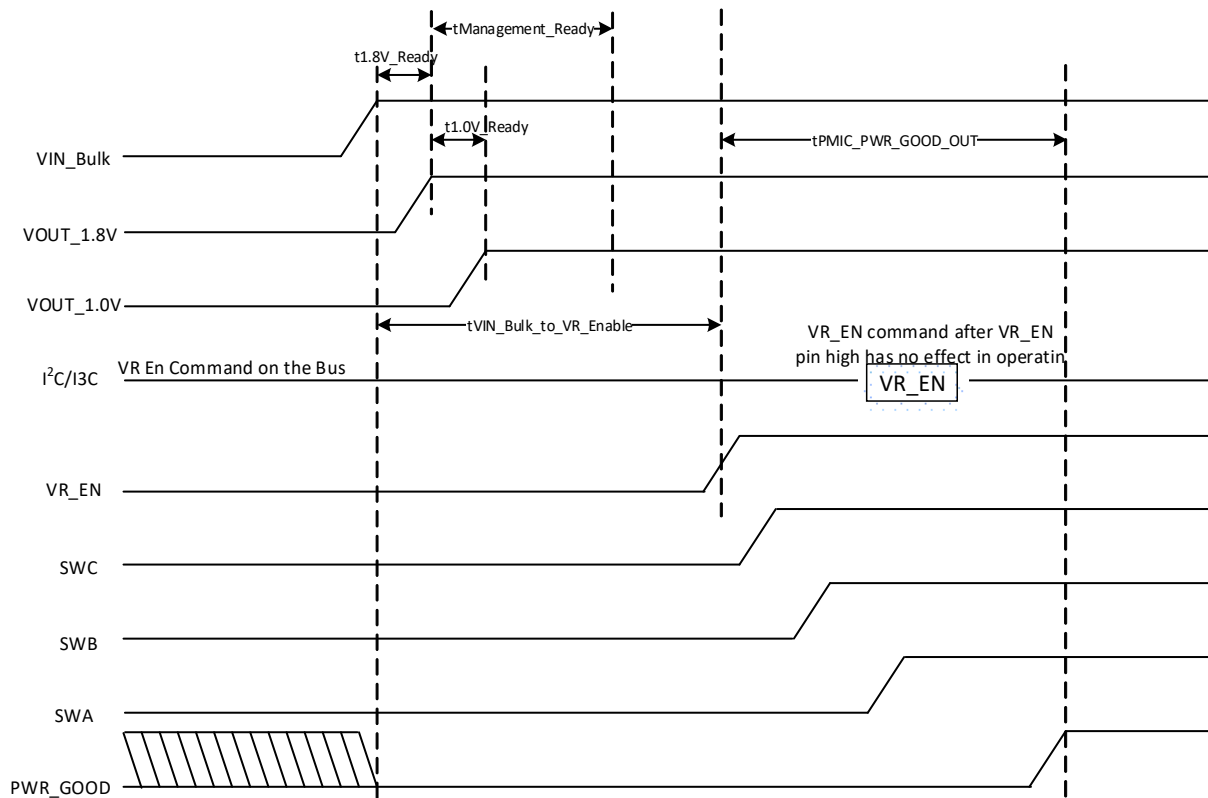


Figure 24 — PMIC Power Up Sequence; with VR_EN Pin followed by Bus Command

6.3 PMIC Output Rail Turn On Timing

The Figure 25 shows the timing relationship once the PMIC receives VR Enable command (either with VR_EN pin or on I²C/I³C Basic bus) and when it floats PWR_GOOD output signal; timing parameter t_{PMIC_PWR_GOOD_OUT} applies. This timing parameter is a sum of maximum soft start time and configured delay for each power on sequence configuration registers that are executed plus additional 5 ms timing margin error. The waveform shows each buck regulator output soft start time and delay time once the soft start time expires for each power on sequence config0 to power on sequence config2 registers. Note that if more than one regulators are enabled in a power on sequence config register and if those regulators have different soft start time programmed, then the larger value of that soft start time is used as a reference for delay timer to start. Each regulator will still follow different soft start time to turn on the buck regulator.

The specific example in Figure 25 uses three power on sequence config0 to config2 registers and only one buck regulator is enabled in each power on sequence config 0 to config 2 registers.

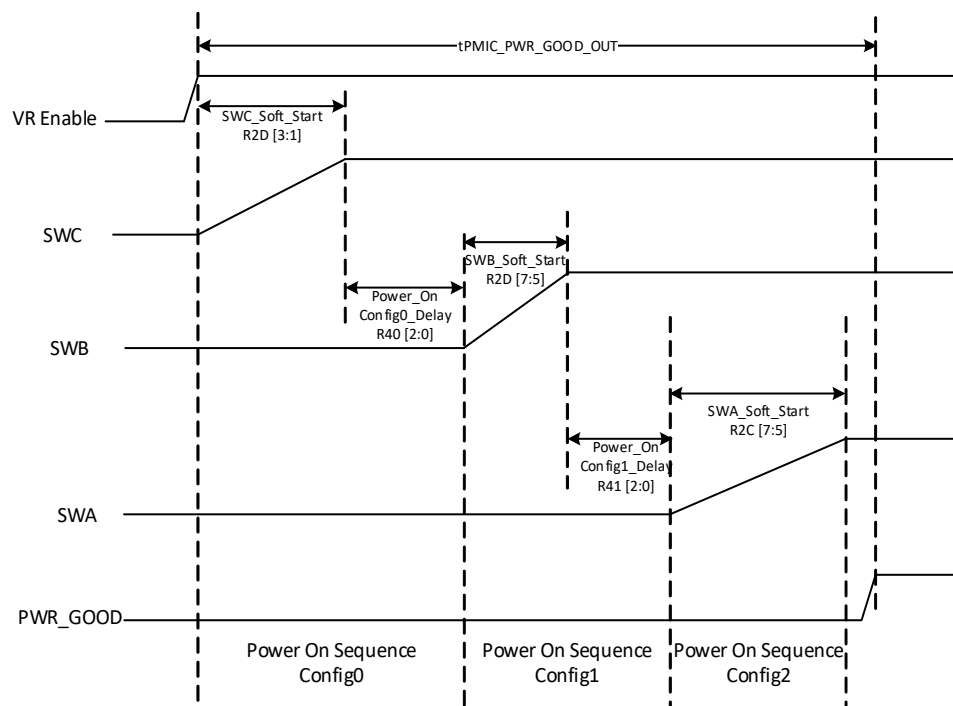


Figure 25 — PMIC Power On Timing

6.4 Secure Mode and Programmable Mode of Operation

Prior to issuing VR Enable command (either with VR_EN pin or on I²C/I3C Basic bus), the host must configure the register Table 135, “Register 0x2F” [2] appropriately as desired. The PMIC offers two modes of operation after VR Enable command (either with VR_EN pin or on I²C/I3C Basic bus) is registered.

1. Programmable Mode - In this mode, independent of when host issues VR Enable command (either with VR_EN pin or on I²C/I3C Basic bus), the PMIC allows modification to any register in the host region as desired by the host and PMIC responds appropriately.
2. Secure Mode - In this mode, after host issues VR Enable command (either with VR_EN pin or on I²C/I3C Basic bus), the PMIC does not allow modification to registers Table 109, “Register 0x15” to Table 135, “Register 0x2F”, Table 138, “Register 0x32” [7,5:0] in the host region as well as Table 149, “Register 0x40” to Register 0x6F in the DIMM vendor region. These registers are write protected marked with RED color cells in “Register” column in Table 90, “Host Region - Register Map” and in Table 91, “DIMM Vendor Region - Register Map”. The PMIC simply ignores the host request. Throughout this entire standard, when it refers to as PMIC allows access to the registers, it refers to write operation to the registers that are not write protected in secure mode or programmable mode. There is no restriction for the read operation in secure mode or programmable mode. The host must power cycle the PMIC to make any modification. The PMIC power cycle is defined as complete removal of VIN_Bulk input supply to the PMIC and this definition is applied to the entire standard. The PMIC does allow modification to any other remaining registers that are not marked in **RED colored** cells in “Register” column in Table 90, “Host Region - Register Map” with I²C or I3C Basic bus. The Secure Mode is only applicable once VR Enable command (either with VR_EN pin or on I²C/I3C Basic bus) is registered. This is important because by default Table 135, “Register 0x2F” [2] = ‘0’ when PMIC is first powered up. Prior to VR Enable command (either with VR_EN pin or on I²C/I3C Basic bus), PMIC allows modification to any registers in the host region.

Note that there is one exception in Secure mode of operation. The exception is for register Table 138, “Register 0x32” [7]. This register can get updated with VR_EN pin assertion/de-assertion or PWR_GOOD signal input assertion to low or when PMIC internally generates its own VR Disable command due to some fault condition. This register cannot be updated with I²C or I3C Basic bus command or with DEVCTRL CCC command.

6.5 Power Down Output Regulators

Regardless of how PMIC's output regulators are turned on (with VR_EN pin or with VR Enable command on I²C/I³C Basic bus), the PMIC's output regulators are powered down as described below depending on PMIC's mode of operation.

6.5.1 Programmable Mode Operation; R1A[4] = '0'

The PMIC allows host to power down any or all output regulators by any of the three methods below.

1. The VR Disable command (Table 138, "Register 0x32" [7] = '0' or VR_EN pin transitions to low). The PMIC executes power off sequence config0 (Table 167, "Register 0x58") to power off sequence config2 (Table 169, "Register 0x5A") to preserve the appropriate voltage relationship as configured in the registers. The PMIC controls the PWR_GOOD signal as following in bullet a and bullet b:
 - a. If VR Disable command with a pin (i.e., VR_EN pin transitions to Low), PMIC asserts PWR_GOOD signal Low. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC executes power on sequence config 0 to power on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. See Figure 26. The PMIC does not require power cycle.
 - b. If VR Disable command on a I²C/I³C Bus (i.e., Table 138, "Register 0x32" [7] = '0'), PMIC keeps the PWR_GOOD signal floating because this is an intentional command from the host and not a fault condition. The host can re-enable the PMIC's output regulators by issuing VR_EN command on the I²C/I³C bus (i.e., Table 138, "Register 0x32" [7] = '1'). The PMIC executes power on sequence config 0 to power on sequence config 2 registers and continues to float the PWR_GOOD signal until tPMIC_PWR_GOOD_OUT time at which point, PMIC assumes normal control of PWR_GOOD signal. See Figure 27. The PMIC does not require power cycle.
 - c. The simultaneous usage of VR_EN pin and I²C/I³C bus command to turn on/off the PMIC is not allowed. If the VR_EN pin transitions to Low first, the PWR_GOOD signal follows as described in bullet a and PWR_GOOD signal remains low even if there is a subsequent I²C/I³C bus command as described in bullet b.
2. Configuring one or more bits in Table 135, "Register 0x2F" [6,4:3] to '0' in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 (Table 167, "Register 0x58") to power off sequence config2 (Table 169, "Register 0x5A") on its own. The PMIC keeps the PWR_GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in Table 135, "Register 0x2F" [6,4:3] to '1' in any specific sequence that is desired by the host. The PMIC keeps the PWR_GOOD signal floating. The PWR_GOOD signal behavior is same as in Figure 27.
3. If Table 138, "Register 0x32" [5] = '1', driving PWR_GOOD input low. The PMIC executes power off sequence config0 (Table 167, "Register 0x58") to power off sequence config2 (Table 169, "Register 0x5A") to preserve the appropriate voltage relationship as configured in the registers and drives PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. If host re-enables PMIC's output regulators by issuing VR_EN command on the I²C/I³C Basic bus (i.e., Table 138, "Register 0x32" [7] = '1'), the PMIC executes power on sequence config 0 to power on sequence config 2 registers and floats PWR_GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.