

JEDEC STANDARD

TS511X, TS521X Serial Bus Thermal Sensor Device Standard

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TS511X, TS521X Serial Bus Thermal Sensor Device Standard

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DEFINITION of TS521X, TS511X THERMAL SENSING DEVICE for MEMORY MODULE APPLICATIONS

(From JEDEC Board Ballot JCB-23-25, formulated under the cognizance of the JC-40.1 Subcommittee on Digital Logic Families and Applications, committee item # 401.04).

1 Scope

This standard defines the specifications of interface parameters, signaling protocols, and features for fifth generation Temperature Sensor (TS5) as used for memory module applications. These device operate on I²C and I3C two-wire serial bus interface. The designation TS521X and TS511X refers to the device specified by this document.

The purpose is to provide a standard for the TS5 device for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

Unless otherwise noted in the document, any illegal operation is not allowed and device operation is not guaranteed.

NOTE: The designation TS521X and TS511X refers to a portion of the part number designation of a series of commercial logic devices common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

The TS521X and TS511X device incorporate thermal sensing capability which is controlled and read over two wire bus. TS5 device operate from a nominal 1.8 V nominal power supply (VDDSPD) and a 1.0 V nominal power supply (VDDIO). The TS5 device is intended to operate up to 12.5 MHz on a 1.0V I3C Basic bus or up to 1 MHz on a 1.0 V to 3.3 V (Grade dependent) I²C bus. The TS5 devices are intended to interface to I²C or I3C Basic buses which have multiple devices on a shared bus, and must be uniquely addressed with fixed addressing on the same bus. All TS5 devices respond to specific pre-defined device select codes on the two-wire bus.

2.2 Common Features Summary

Table 1 — Device Part Numbers and Feature Summary

Part Number	Serial Numbers	Thermal Sensor	Temperature Range	Bus Pullup Nominal Voltage Range	Device Grade
TS5111	No	Yes	-40 °C to 125 °C	1.0 V to 3.3 V	A
TS5110	No			1.0 V to 1.2 V	B
TS5211	Yes	Yes	-40 °C to 125 °C	1.0 V to 3.3 V	A
TS5210	Yes			1.0 V to 1.2 V	B

2.2 Common Features Summary (cont'd)

- Two wire bus serial interface (I²C and I3C Basic operation modes)
- Up to 12.5 MHz transfer rate
- 1.8 V and 1.0 V power supply input
- Packaged in 6 ball WLCSP
- Packet Error Check (PEC) Function
- Parity Error Check Function
- Bus Reset Function
- Two unique addresses selected by SA pin
- In Band Interrupt (IBI) (Transparent Mode of Operation)
- 6 ball WLCSP Package device Functional Diagram

3 Device Power Up

The TS5 device has one VDDSPD supply input and one VDDIO supply input.

In order to prevent inadvertent operations during power up, a Power On Reset (POR) circuit is included. On cold power on, VDDSPD input supply must rise monotonically between VPON and VDDSPD_{min} without ringback for device to turn on.

The TS5 device uses VDDIO input for its IO levels and it must reach VDDIO_{min} to ensure proper operation of I²C or I3C Basic interface.

Once the VDDSPD and VDDIO supply is valid and stable, the TS5 device shall:

1. Within $t_{\text{Sense_SA}}$ time, sense its SA pin to automatically configure the LID code based on what is detected on SA pin.
2. Enable I²C interface within t_{INIT} time and be ready to receive the command from the controller. The TS5 device is ready for operation after t_{INIT} time.

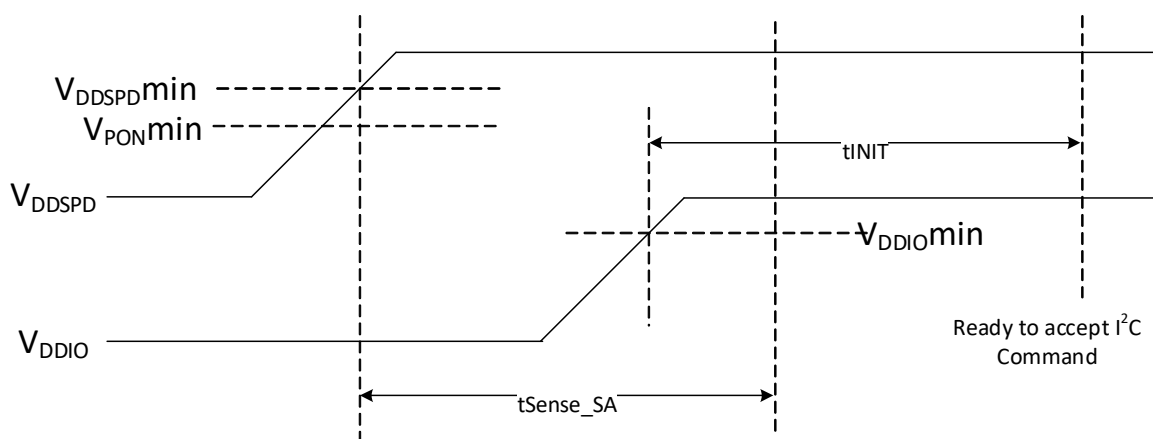


Figure 1 — Device Power Up Sequence

4 Device Reset and Initialization

At power down (phase during which VDDSPD input supply decreases continuously), as soon as VDDSPD input supply drops below the $V_{DDSPD_{min}}$, the device does not guarantee the operation.

On warm power cycling, the VDDSPD and VDDIO input supply must remain below V_{POFF} for t_{POFF} and must meet cold power on reset timing when restoring the power.

5 I²C and I3C Basic Operation

At power on, by default, the TS5 device comes up in I²C mode of operation. Following applies in I²C mode:

1. The maximum operation speed is limited to 1 MHz
2. In-band interrupts are not supported
3. Bus reset is supported.
4. Parity check is not supported except for supported CCCs.
5. Packet Error check is not supported.

The TS5 device shall operate in the I²C mode until put into I3C Basic mode via command.

The controller may put the TS5 device in I3C Basic mode by issuing SETAASA CCC.

Following applies in I3C mode.

1. The maximum operation speed is up to 12.5 MHz
2. In-band interrupts are supported
3. Bus reset is supported.
4. Parity check is always enabled by default.
5. Packet error check is supported and by default is disabled.

6 Device Interface - Protocol

The 7-bit serial address of the TS5 device applies to both I²C and I3C Basic mode of operation identically.

6.1 Serial Address of TS5 Device

The TS5 device 4-bit binary value is 0010b or 0110b depending sample status of SA pin on power up.

The TS5 device samples the status of the SA pin on power up. The sampled status of the SA pin is used to select one of the two possible unique LID code for the device. The selected LID code either 0010b or 0110b is merged with a 3 bit HID code Table 76, "MR7" [3:1] to establish the 7-bit address code the device. With the default setting in Table 76, "MR7" [3:1] = '111'; if the SA ball is connected to VSS, the device address shall be 0010 111b and if the SA ball is connected to VDDSPD, the device address shall be 0110 111b.

6.1 Serial Address of TS5 Device (cont'd)

Table 2 — 7-bit Address of TS5 Device

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SA	1	0	1	1	1	R/W
TS5 Device Type ID (LID)				Host ID (HID)			Read/W rite

6.2 Switch from I²C Mode to I3C Basic Mode

By default when TS5 first powers on, it operates in I²C mode. The TS5 device shall operate in I²C mode until put into I3C Basic mode via command.

In I²C mode, the controller is allowed to issued only 3 CCCs (DEVCTRL, SETHID, SETAASA). All other CCCs are not supported and the TS5 device may simply ignore it. The Controller must issue DEVCTRL and SETHID CCC first (if required) followed by SETAASA CCC.

The Controller puts the TS5 device in I3C mode by issuing SETAASA CCC.

When SETAASA CCC is registered by the TS5 device, it updates the Table 77, “MR18” [5] to ‘1’.

When SETHID CCC is registered by the TS5 device, it updates the Table 76, “MR7” [3:1].

6.3 Switch from I3C Basic Mode to I²C Mode

The Controller can put the TS5 device back in I²C mode from I3C Basic mode at any time by issuing RSTDAA CCC.

When RSTDAA CCC is registered by the TS5 device, it updates the Table 77, “MR18” [5] to ‘0’.

6.4 I²C Target Protocol

The TS5 device operate on a standard I²C serial interface. Transactions where the TS5 device is the targeted target device begin with the Controller issuing a START condition followed by a 7-bit TS5 device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the TS5 device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK.

The TS5 device accepts 1 byte of address which covers 256 bytes of registers. The TS5 device volatile register space does not require page selection process as all registers are within first 256 bytes.

6.4.1 Write Operation - Data Packet

Table 3 — Write Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	0	X	1	0	HID			W=0	A	
	Address [7:0]								A	
	Data								A	
	...								A	
	Data								A	
NOTE 1 In I ² C mode, Start or Repeat Start operation followed by 7 ^h 7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation including another Repeat Start is considered an illegal operation.										

6.4.2 Read Operation - Data Packet

Table 4 — Read Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr ¹	0	X	1	0	HID			W=0	A	
	Address [7:0]								A	
Sr	0	X	1	0	HID			R=1	A ²	
	Data								A	
	...								A	
	Data								N	
NOTE 1	In I ² C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I ² C mode. Any other operation including another Repeat Start is considered an illegal operation.									
NOTE 2	If target device NACKs during Repeat Start for any reason, the controller may re-try Repeat Start again. The controller can do the Repeat Start as many times it may desire. TS5 may eventually ACK.									

6.4.3 Default Read Address Pointer Mode

During normal operation of the DDR5 DIMM, the controller periodically may poll critical information from the same location. An example may be the TS device's temperature readout. To help improve the efficiency of the I²C bus protocol, the TS5 offers a default read address pointer mode so that whenever the TS5 device sees the STOP operation on its SCL and SDA bus, its read address pointer is always resets to default address. The default read pointer address mode is enabled through register Table 77, "MR18" [4] and default starting address for read operation is selectable through register Table 77, "MR18" [3:2]. This allows controller to read the read command data packet as shown in Table 5. The default read address pointer reduces the packet overhead by 2 bytes. The controller typically enables this mode when the normal operation of the DDR5 DIMM begins.

6.4.3 Default Read Address Pointer Mode (cont'd)

Table 5 — Read Command Data Packet with Default Address Pointer Mode

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	0	X	1	0	HID			R=1	A	
	Data								A	
	...								A	
	Data								N	Sr or P

6.5 I3C Basic Target Protocol

The TS5 device operate on a standard I3C serial interface. Transactions where the TS5 device is the targeted target device begin with the Controller issuing a START condition followed by a 7-bit TS5 device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the TS5 device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 6. The “T” bit carries Parity information from the Controller for each byte.

The Packet Error Code (PEC) function is disabled by default when the TS5 device is put in I3C Basic mode. The controller may optionally enable this function through Table 77, “MR18” [7] or DEVCTRL CCC. If enabled, the PEC is appended at the end of all transactions. If PEC is enabled, the controller must complete the burst length as indicated in CMD field. In other words, the controller must not interrupt the burst length pre-maturely for Write operation.

6.5.1 Write Operation - Data Packet

Table 6 — Write Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	X	1	0	HID			W=0	A ^{1,2,3}	
	Address [7:0]								T	
	Data								T	
	...								T	
	Data								T	
NOTE 1	See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (1st bit of Addr, bit [7]).									
NOTE 2	The TS5 NACKs if there is a parity error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 3	The TS5 does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the controller does not match with its own device code. The TS5 ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 4	Repeat Start or Repeat Start with 7'h7E.									

6.5.1 Write Operation - Data Packet (cont'd)**Table 7 — Write Command Data Packet; PEC Enabled**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	X	1	0	HID			W=0	A ^{1,2,3}	
	Address [7:0]								T	
	CMD			W=0	0000			T		
	Data								T	
	...								T	
	Data								T	
	PEC								T	
NOTE 1	See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (1st bit of Addr, bit [7]).									
NOTE 2	The TS5 NACKs if there is a parity or PEC error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 3	The TS5 does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the controller does not match with its own device code. The TS5 ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 4	Repeat Start or Repeat Start with 7'h7E.									

The controller may optionally allow TS5 device to request IBI. For this case, the transactions to the TS5 device begin with the I3C controller issuing a START condition followed by 7'h7E and then write bit. If TS5 device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If TS5 device has no pending IBI, there is no action taken by TS5. Table 8 and Table 9 show the I3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 9, PEC calculation does not include IBI header byte (7'h7E followed by W=0).

Table 8 — Write Command Data Packet with IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,3}	
Sr	0	X	1	0	HID			W=0	A ^{2,3,4}	
	Address [7:0]								T	
	Data								T	
	...								T	
	Data								T	
NOTE 1	See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (Repeat Start).									
NOTE 2	See Figure 4 to see how the transition occurs from Controller Push Pull Operation to target Open Drain (ACK) and See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (1st bit of Addr, bit [7]).									
NOTE 3	The TS5 NACKs if there is a parity error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 4	The TS5 does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the controller does not match with its own device code. The TS5 ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 5	Repeat Start or Repeat Start with 7'h7E.									

6.5.1 Write Operation - Data Packet (cont'd)

Table 9 — Write Command Data Packet with IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,3}	
Sr	0	X	1	0	HID			W=0	A ^{2,3,4}	
	Address [7:0]								T	
	CMD			W=0	0000			T		
	Data								T	
	...								T	
	Data								T	
	PEC								T	
NOTE 1	See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (Repeat Start).									
NOTE 2	See Figure 4 to see how the transition occurs from Controller Push Pull Operation to target Open Drain (ACK) and See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (1st bit of Addr, bit [7]).									
NOTE 3	The TS5 NACKs if there is a parity or PEC error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 4	The TS5 does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the controller does not match with its own device code. The TS5 ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 5	Repeat Start or Repeat Start with 7'h7E.									

6.5.2 Read Operation - Data Packet

The TS5 device operate on a standard I3C Basic serial interface. Transactions where the TS5 device is the targeted target device begin with the Controller issuing a START condition followed by a 7-bit TS5 device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the TS5 device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 10. The “T” bit carries Parity information from the Controller for each byte prior to Repeat START. After Repeat START, “T” bit carries information from TS5 device to Controller indicating Continuous (‘1’) or Stop (‘0’) whether it is transmitting the last byte or not.

The Packet Error Code (PEC) function is disabled by default when the TS5 device is put in I3C Basic mode. The controller may optionally enable this function through Table 77, “MR18” [7] or DEVCTRL CCC. If enabled, the PEC is appended as shown in Table 10. If PEC is enabled, the controller must complete the burst length as indicated in CMD field. In other words, the controller must not interrupt the burst length pre-maturely for Read operation

6.5.2 Read Operation - Data Packet (cont'd)

Table 10 — Read Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	X	1	0	HID			W=0	A ^{1,2,3}	
	Address [7:0]								T	
Sr	0	X	1	0	HID			R=1	A/N ^{4,5}	
	Data								T=1	
	...								T=1	
	Data								T=1 ^{6,7}	Sr ⁸ or P
NOTE 1	See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (1st bit of Addr, bit [7]).									
NOTE 2	The TS5 NACKs if there is a parity error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 3	The TS5 does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the controller does not match with its own device code. The TS5 ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 4	If target device NACKs during Repeat Start for any reason, the controller may re-try Repeat Start again. The controller can do the Repeat Start as many times it may desire. If target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Controller tries Repeat Start. If there were no parity errors, the TS5 may eventually ACK.									
NOTE 5	See Figure 4 to see how the transition occurs from Controller Push Pull Operation to target Open Drain (ACK).									
NOTE 6	See Figure 5 to see how Controller ends target device operation.									
NOTE 7	When last byte (i.e., MR255) is reached (extreme rare case), the target device sends T = '0'. See Figure 6 to see how target device ends the operation followed by Controller STOP operation.									
NOTE 8	Repeat Start or Repeat Start with 7'h7E.									

6.5.2 Read Operation - Data Packet (cont'd)

Table 11 — Read Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	X	1	0	HID			W=0	A ^{1,2,3}	
	Address [7:0]								T	
	CMD			R=1	0000			T		
	PEC								T	
Sr	0	X	1	0	HID			R=1	A/N ^{4,5}	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 ⁶	
NOTE 1	See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (1st bit of Addr, bit [7]).									
NOTE 2	The TS5 NACKs if there is a parity or PEC error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 3	The TS5 does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the controller does not match with its own device code. The TS5 ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 4	If target device NACKs during Repeat Start for any reason, the controller may re-try Repeat Start again. The controller can do the Repeat Start as many times it may desire. If target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Controller tries Repeat Start. If there were no parity or PEC errors, the TS5 may eventually ACK. The PEC calculation by the target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the target device includes device select of only the last Repeat Start from the Controller when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.									
NOTE 5	See Figure 4 to see how the transition occurs from Controller Push Pull Operation to target Open Drain (ACK).									
NOTE 6	See Figure 6 to see how target device ends the operation followed by Controller STOP operation.									
NOTE 7	Repeat Start or Repeat Start with 7'h7E.									

The controller may optionally allow TS5 device to request IBI. For this case, the transactions to the TS5 device begin with the I3C Basic controller issuing a START condition followed by 7'h7E and then write bit. If TS5 device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If TS5 device has no pending IBI, there is no action taken by TS5. Table 8 and Table 9 show the I3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 9, PEC calculation does not include IBI header byte (7'h7E followed by W=0).

6.5.2 Read Operation - Data Packet (cont'd)

Table 12 — Read Command Data Packet with IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,3}	
Sr	0	X	1	0	HID			W=0	A ^{2,3,4}	
	Address [7:0]								T	
Sr	0	X	1	0	HID			R=1	A/N ^{5,6}	
	Data								T=1	
	...								T=1	
	Data								T=1 ^{7,8}	Sr ⁹ or P
NOTE 1	See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (Repeat Start)									
NOTE 2	See Figure 4 to see how the transition occurs from Controller Push Pull Operation to target Open Drain (ACK) and see Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (1st bit of Addr, bit [7]).									
NOTE 3	The TS5 NACKs if there is a parity error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 4	The TS5 does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the controller does not match with its own device code. The TS5 ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 5	See Figure 4 to see how the transition occurs from Controller Push Pull Operation to target Open Drain (ACK).									
NOTE 6	If target device NACKs during Repeat Start for any reason, the controller may re-try Repeat Start again. The controller can do the Repeat Start as many times it may desire. If target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Controller tries Repeat Start. If there were no parity errors, TS5 may eventually ACK.									
NOTE 7	See Figure 5 to see how Controller ends target device operation.									
NOTE 8	When last byte (i.e., MR255) is reached (extreme rare case), the target device sends T = '0'. See Figure 6 to see how target device ends the operation followed by Controller STOP operation.									
NOTE 9	Repeat Start or Repeat Start with 7'h7E.									

6.5.2 Read Operation - Data Packet (cont'd)

Table 13 — Read Command Data Packet with IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,3}	
Sr	0	X	1	0	HID			W=0	A ^{2,3,4}	
	Address [7:0]								T	
	CMD			R=1	0000				T	
	PEC								T	
Sr	0	X	1	0	HID			R=1	A/N ^{5,6}	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 ⁷	Sr ⁸ or P
NOTE 1	See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (Repeat Start).									
NOTE 2	See Figure 4 to see how the transition occurs from Controller Push Pull Operation to target Open Drain (ACK) and see Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (1st bit of Addr, bit [7]).									
NOTE 3	The TS5 NACKs if there is a parity or PEC error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 4	The TS5 does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the controller does not match with its own device code. The TS5 ignores the entire packet until STOP or next Repeat Start operation.									
NOTE 5	See Figure 4 to see how the transition occurs from Controller Push Pull Operation to target Open Drain (ACK).									
NOTE 6	If target device NACKs during Repeat Start for any reason, the controller may re-try Repeat Start again. The controller can do the Repeat Start as many times it may desire. If target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Controller tries Repeat Start. If there were no parity or PEC errors, the TS5 may eventually ACK. The PEC calculation by the target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the target device includes device select of only the last Repeat Start from the Controller when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.									
NOTE 7	See Figure 6 to see how target device ends the operation followed by Controller STOP operation.									
NOTE 8	Repeat Start or Repeat Start with 7'h7E.									

6.5.3 Default Read Address Pointer Mode

This mode works the same exact way as explained in Section 6.4.3. Table 14 and Table 15 show the read command data packet for PEC function disabled and enabled respectively. When PEC function is enabled, Table 77, “MR18” [1] sets the number of bytes that TS5 device sends out followed by the PEC calculation. If PEC is enabled, the controller must complete the burst length as indicated in Table 77, “MR18” [1] register. In other words, the controller must not interrupt the burst length pre-maturely for default address pointer read operation.

6.5.3 Default Read Address Pointer Mode (cont'd)

Table 14 — Read Command Data Packet with Read Address Pointer Mode; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	X	1	0	HID			R=1	A ¹	
	Data								T=1	
	...								T=1	
	Data								T=1 ^{2,3}	Sr ⁴ or P
NOTE 1	The TS5 NACKs if there is a parity error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 2	See Figure 5 to see how Controller ends target device operation.									
NOTE 3	When last byte (i.e., MR255) is reached (extreme rare case), the target device sends T = '0'. See Figure 6 to see how target device ends the operation followed by Controller STOP operation.									
NOTE 4	Repeat Start or Repeat Start with 7'h7E.									

Table 15 — Read Command Data Packet with Read Address Pointer Mode; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0	X	1	0	HID			R=1	A ¹	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 ²	
NOTE 1	The TS5 NACKs if there is a parity or PEC error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 2	See Figure 6 to see how target device ends the operation followed by STOP operation									
NOTE 3	Repeat Start or Repeat Start with 7'h7E.									

6.5.3 Default Read Address Pointer Mode (cont'd)

Table 16 — Read Command Data Packet with Read Address Pointer and IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,2}	
Sr	0	X	1	0	HID			R=1	A/N ^{2,3}	
	Data								T=1	
	...								T=1	
	Data								T=1 ^{4,5}	Sr ⁶ or P
NOTE 1	See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (Repeat Start).									
NOTE 2	The TS5 NACKs if there is a parity error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 3	See Figure 4 to see how the transition occurs from Controller Push Pull Operation to target Open Drain (ACK).									
NOTE 4	See Figure 5 to see how Controller ends target device operation.									
NOTE 5	When last byte (i.e., MR255) is reached (extreme rare case), the target device sends T = '0'. See Figure 6 to see how target device ends the operation followed by Controller STOP operation.									
NOTE 6	Repeat Start or Repeat Start with 7'h7E.									

Table 17 — Read Command Data Packet with Read Address Pointer and IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A ^{1,2}	
Sr	0	X	1	0	HID			R=1	A/N ^{2,3}	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 ⁴	
NOTE 1	See Figure 2 to see how the transition occurs from target Open Drain (ACK) to Controller Push Pull Operation (Repeat Start).									
NOTE 2	The TS5 NACKs if there is a parity or PEC error in a previous transaction when controller performs consecutive transactions with Repeat Start.									
NOTE 3	See Figure 4 to see how the transition occurs from Controller Push Pull Operation to target Open Drain (ACK).									
NOTE 4	See Figure 6 to see how target device ends the operation followed by STOP operation									
NOTE 5	Repeat Start or Repeat Start with 7'h7E.									

6.5.3 Default Read Address Pointer Mode (cont'd)

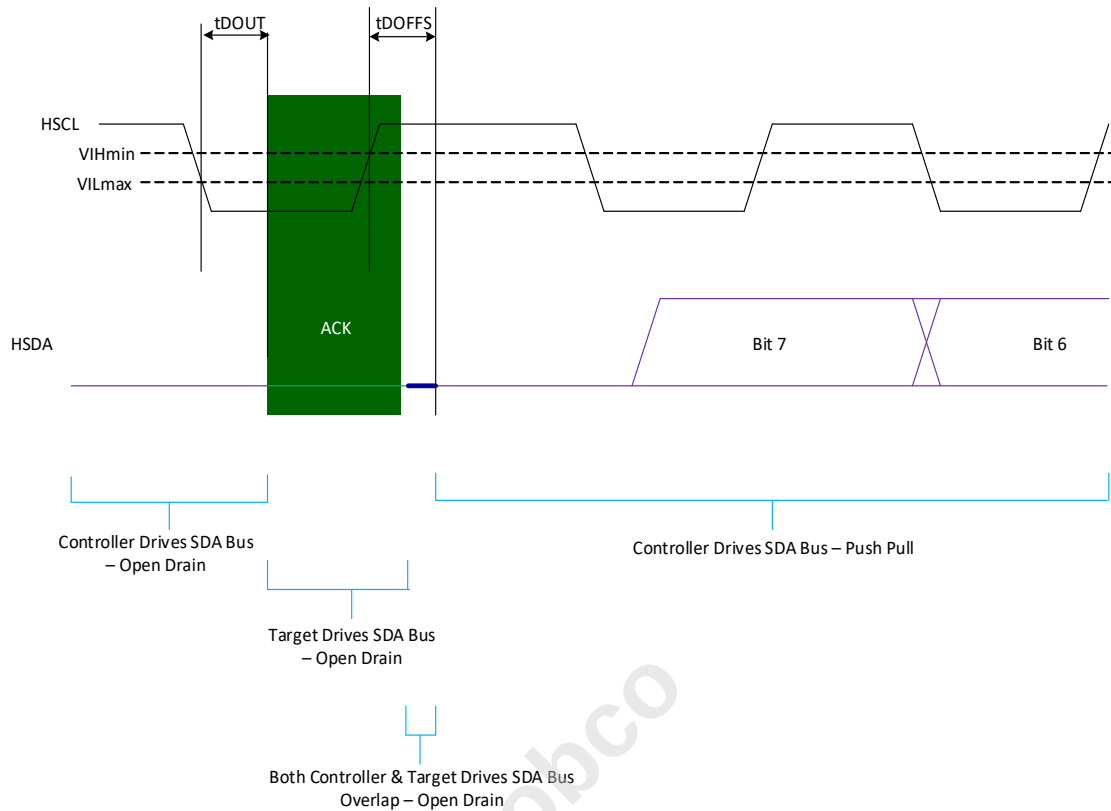


Figure 2 — Target Open Drain to Controller Push Pull Hand Off Operation