

JEDEC STANDARD

DDR4 NVDIMM-P Bus Protocol

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DDR4 NVDIMM-P BUS PROTOCOL

(From JEDEC Board Ballot, JCB-20-26, formulated under the cognizance of the JC-45.6 Subcommittee on Hybrid Modules.)

1. Scope

An NVDIMM-P device is defined as a LRDIMM memory module which provides host controller access to DRAM and/or other memory devices such as persistent memory. In order to enable access to media that may have non-deterministic access latencies, and/or on-board media management activities, which may temporarily delay access to non-volatile memory media, a handshake protocol is required to inform the host controller of availability/unavailability of return data from the DIMM. To mitigate the performance impact of this non-determinism, capabilities to enable out-of-order data transactions and to stack commands for enhanced data bus utilization are also required. A transactional protocol is described herein for NVDIMM-P, which may be used on a DDR interface allowing operation of both standard DRAM modules and NVDIMM-P modules on the same channel.

NVDIMM-P modules follow the DDR4 LRDIMM specification in pinout, electrical topology and behavior except as noted in this specification.

Minimal changes to the host controller can enable these technologies while allowing flexibility to optimize memory system performance. Options to simplify the protocol or implementation (at the expense of performance) are provided.

1.1 Reference Material

This NVDIMM-P protocol spec is a companion to the JEDEC DDR4 DRAM Standard, *JESD79-4B*, as well as the JEDEC DDR4 RCD/DB Standard and JEDEC DDR4 LRDIMM Common Standard.

2. Architecture and Initialization

2.1 NVDIMM-P bus architecture

Figure 1a shows an NVDIMM-P bus architecture example.

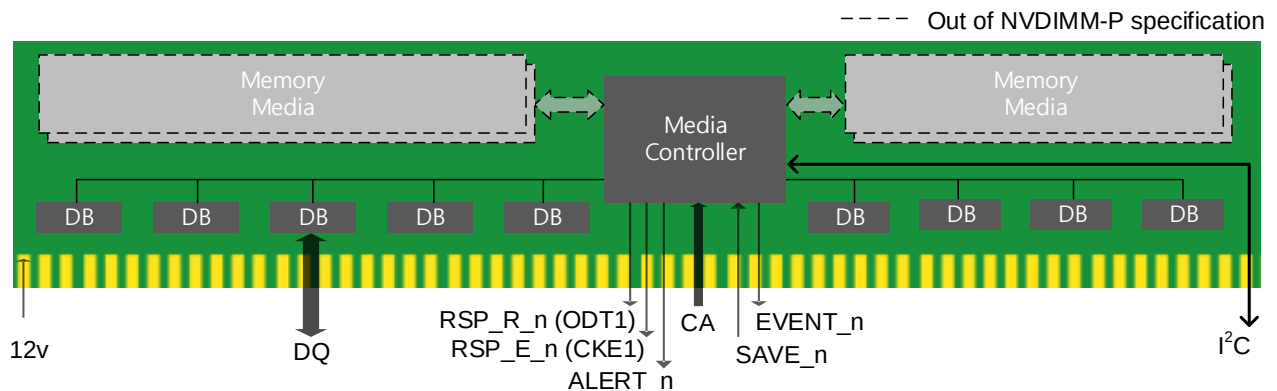


Figure 1a — Example of NVDIMM-P bus architecture

2.1.1 CA and Data bus

The command, address, and data pins of DDR4 NVDIMM-P are identical to DDR4 LRDIMM. Refer to the “JEDEC DDR4 LRDIMM Design Specification”.

2.1.2 Response Signal

Response signals are used to notify the data ready, event or error conditions described below.

- **RSP_R_n:** Response READY signal. Asynchronous, active-LOW, pulse-width modulated signal from NVDIMM-P to host indicating transactional/handshake signals such as when a read data packet is available, or when a status or error condition exists. One signal pin per NVDIMM-P is provided and directly connected to host.
- **RSP_E_n:** Response EXTRA signal. Asynchronous, active-LOW, pulse-width modulated signal from NVDIMM-P to host indicating persistent write completion. One signal pin per NVDIMM-P is provided and directly connected to host.
- **ALERT_n:** Response ERROR signal. Asynchronous, active-LOW, pulse-width modulated signal from NVDIMM-P to host indicating CA parity error and Write Channel error. One signal pin per NVDIMM-P is provided and shared with other SDRAM LRDIMM or NVDIMM in same channel to host.

To make the NVDIMM-P pin-out compatible with DDR4 LRDIMM, response signals are repurposed from existing DDR4 LRDIMM pins. Table 1 shows the pin assignments. Note that the ODT1 is repurposed for RSP_R_n and CKE1 is repurposed for RSP_E_n. Each NVDIMM-P has one (1) RSP_R_n signal and one (1) RSP_E_n signal. The pin assignment of the response signals is described in Table 1, “ - Response Signal Pin Assignment”.

Table 1 - Response Signal Pin Assignment

DDR4 LRDIMM			DDR4 NVDIMM-P		
Name	Pin number	Tx/Rx	Name	Pin number	Tx/Rx
ODT1	91	Rx	RSP_R_n	91	Tx
CKE1	203	Rx	RSP_E_n	203	Tx
ALERT_n	208	Tx	ALERT_n	208	Tx

The electrical characteristics of the response signal, RSP_R_n and RSP_E_n, shall follow the single ended AC & DC output levels and single-ended AC & DC input/output levels for DQ signals, respectively, as defined in the DDR4 SDRAM Specification, JESD79-4B. The electrical characteristics of ALERT_n are identical to DDR4 SDRAM ALERT_n. The response signal shall transmit asynchronously in order to convey read data, status or error message availability, via the use of pulse-width modulation to discern between response conditions. The encoding for the possible responses transmitted on the response signal is described in Table 2.

2.1.2 Response Signal (cont'd)

Table 2 - Response Signal Encoding

Response Signal	Response Pulse Width ^{1,2}	Symbol	Function	Description
RSP_R_n	2	RD_RDY	Read Ready	Read data or Message packet is available in buffers for host retrieval
	4	URGENT	Urgent Error	Urgent error detected on the bus or protocol. Host controller shall poll status immediately to respond to error condition or condition requiring additional action. See 7.1.6
RSP_E_n	2	W_PER	Write Persistency	Data has been written to NVM by flush request. See 4.5
	4	RFU	Reserved	Reserved for future use
ALERT_n	See Table 127	PAR_ERR	CA parity Error	CA parity Error is detected
	See Table 127	WECC_ERR	Write Channel Error	Write Channel error is detected

- NOTE 1 Pulse width is in clock cycles (2UI). The response pulse is active LOW. The maximum response length is 8 UI, equivalent to a DQ burst length of 8. The maximum response pulse width is equivalent to 1.6Gbps @ DDR4-3200.
- NOTE 2 Responses must be separated by a high pulse width of minimum tRSPH.

A RSP_R_n signal from the NVDIMM-P with a logic LOW pulse-width of two (2) clocks (4 UIs) indicates that message or requested data of XREAD is available in the DIMM output buffers.

The RSP_R_n signal with a logic LOW pulse-width of four (4) clocks (8UIs) conveys that an urgent error condition requiring immediate attention exists. A RSP_E_n signal from the NVDIMM-P with a logic LOW pulse-width of two (2) clocks (4UIs) conveys that a group of one or more data bursts has been committed to Non-Volatile Media (NVM).

A minimum tRSPH logic level HIGH time of two (2) clocks (4UIs) must be provided between any signaled responses. An example of pulse-width modulated signals on the RSP_R_n and RSP_E_n pin is described in the following figure.

The NVDIMM-P response signals are non-deterministic and independent. There is no timing correlation between the commands and the responses on each signal.

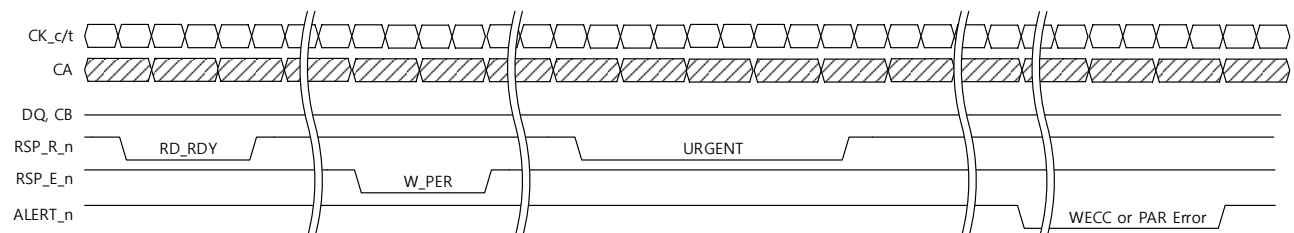


Figure 1b - Response Signaling

2.1.3 Event_n and Save_n

Event_n and Save_n pins are used for communication with the module management controller. See “Module Management Register” Specification for more details.

2.1.4 I2C bus

I2C bus is used to access SPD, MCW(Media controller Control Word) and MMR(Module Management Register). See section 3.2 and “Module Management Register” Specification for more details.

2.2 Data packet format

For data read write operation, NVDIMM-P supports two different data packet formats:

- Option A: 4 user-defined metadata (user) bits and 3 write credit (WC) bits
- Option B: 6 user-defined metadata bits (user) and 1 Credit Threshold (CTH) bit

The data format is determined by the contents of MR2 A[13] bit during the power-up initialization. If MR2 A[13] bit is 0, Format A is used. If MR2 A[13] bit is 1, Format B is used. See Sections 0 for more details.

Option A:

The NVDIMM-P returns packet information for each transaction containing of the following:

- 8 bits Read ID (RID)
- 1 bit data poison
- 4 bits user-defined metadata
- 3 bits Write Credit (WC)
- 48 bits Channel ECC

The transaction data packet format is described in the following tables.

Table 3 - Write data packet format for XWRITE and PWRITE

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Write Data0				Write Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RFU	RFU	RFU	RFU
CB7	POISON	RFU	RFU	RFU	RFU	RFU	RFU	RFU

Table 4 - Read data and message packet format for SEND

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Read Data0				Read Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RID[3]	RID[2]	RID[1]	RID[0]
CB7	POISON	WC[2]	WC[1]	WC[0]	RID[7]	RID[6]	RID[5]	RID[4]

NOTE RID≠FFh indicates read data packet, RID=FFh indicates message packet

Table 5 - Read data packet format for SREAD

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Read Data0				Read Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RFU	RFU	RFU	RFU
CB7	POISON	WC[2]	WC[1]	WC[0]	D_VALID	RFU	RFU	RFU

Option B:

The NVDIMM-P returns packet information for each transaction containing of the following:

- 8 bits Read ID (RID)
- 1 bit data poison
- 6 bits user-defined metadata
- 1 bits CTH(Credit Threshold)
- 48 bits Channel ECC

The transaction data packet format is described in the following tables. ,

Table 6 - Write data packet format for XWRITE and PWRITE

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Write Data0				Write Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RFU	RFU	RFU	RFU
CB7	POISON	RFU	USER	USER	RFU	RFU	RFU	RFU

Table 7 - Read data and message packet format for SEND

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Read Data0				Read Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RID[3]	RID[2]	RID[1]	RID[0]
CB7	POISON	CTH	USER	USER	RID[7]	RID[6]	RID[5]	RID[4]

NOTE: RID≠FFh indicates read data packet, RID=FFh indicates message packet

Table 8 - Read data packet format for SREAD

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Read Data0				Read Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RFU	RFU	RFU	RFU
CB7	POISON	CTH	USER	USER	D_VALID	RFU	RFU	RFU

2.2.1 Read ID

As part of the NVDIMM-P protocol, an explicit RID function is utilized whereby the host controller shall provide an 8-bit transaction Read ID (RID) value. By using the 8 bit RID, the NVDIMM-P supports up to 255 Out-of-Order read transactions. The NVDIMM-P will return the transaction RID along with transaction data as part of the transaction information bus.

2.2.2 Poison and User-defined metadata

Poison and User-defined metadata on writes is stored on NVDIMM-P and returned with corresponding data packet. In normal case, poison bit=1 is used to indicate the poisoned data by the host. Poison on writes is stored and returned as poisoned data on reads.

2.2.3 Data Valid (D_VALID)

This bit indicates the read data validity of a SREAD.

2.2.4 Write Credit (WC) and PWRITE Credit (PWC)

WC and PWC indicate available buffer space in NVDIMM-P at a 64-byte granularity. They are used to limit the number of outstanding XWRITE and PWRITE requests from the host. The total number of credits for XWRITE and PWRITE requests is defined in the message packet, which can be accessed with a READ_STATUS command on initialization. Refer to sections 2.3, “Message packet” and Section 0, “

Available Credit **Synchronization**” for details. The NVDIMM-P device provides write credit feedback to the host as part of the SEND or SREAD response packet using the WC [2:0] (option A) or CTH (option B) fields. The write credit from the NVDIMM-P indicates the number of released write credits (1 write credit represents a 64B write buffer space) since last write credit feedback.

Option A:

The poison bit represents the Poison case and differentiates between XWRITE and PWRITE write credit values as described below.

- Poison bit = 0 WC[2:0] are XWRITE credits, values defined in Table 9
- Poison bit = 1 and WC[2:0] = 000b Poison case, shown in Table 10
- Poison bit = 1 and WC[2:0] ≠ 000b WC[2:0] are PWRITE credits, values defined in Table 10

The poison bit is combined with the three WC[2:0] bits to encode write credits for 0 up to 64 credits. NVDIMM-P always returns the best encoding that is equal to or less than the actual number of credits to be returned.

Table 9 - Write Credit Return

POISION and WC value of SEND or SREAD packet				Returned Write Credit Value
POISON	WC[2]	WC[1]	WC[0]	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	4
0	1	0	0	8
0	1	0	1	16
0	1	1	0	32
0	1	1	1	64

Table 10 - Poison and PWRITE Credit return

POISION and WC value of SEND or SREAD packet				Returned PWRITE Credit or Poison
POISON	WC[2]	WC[1]	WC[0]	
1	0	0	0	Poison
1	0	0	1	1
1	0	1	0	2
1	0	1	1	4
1	1	0	0	8
1	1	0	1	16
1	1	1	0	32
1	1	1	1	64

Since Both WC and PWC are encoded over the same bits, only one of them can be returned with a given read data packet. The media controller should prioritize sending the credits back based on buffer demand for each.

Option B:

The Credit Threshold(CTH) bit represents a programmable write credit threshold value. This value is programmed by the host in mode register location MR2 A[2:0] using the same encoding as the Option A's scheme as shown in Table 9 and Table 10. When a new CTH value is programmed in MR2 A[2:0], the NVDIMM-P does not start using the new CTH value until it receives a READ_STATUS[01] (ADDR[3:2]=01b) command for the total available write buffer space. After the READ_STATUS command is received, the NVDIMM-P will return the three-bit CTH field in the READ_STATUS message packet and the change of incremental credit value will take effect.

If CTH = 0 in the read data or message packet metadata, then no credits are returned to the host. If CTH = 1 then credits based on the programmed value are returned to the host.

Poison bit is combined with CTH bits to return write credits as shown in below. The NVDIMM encodes the poison case with Poison=1 and CTH=0.

Table 11 - Credit Return with CTH

Poison	CTH	Comment
0	0	No Credits returned
0	1	WC returned
1	0	Poison Case
1	1	PWC returned

2.3 Message packet format

Table 12 defines the message packet delivered through the DQ bus. RID=FFh, POISON=0 and valid WC are delivered through CB6 and CB7 with the message packet. For any fields with multiple bits assigned for each DQ, the fields are transmitted from MSB to LSB of the field as the data beat increases from 0 to 7. There are two scenarios that the NVDIMM-P delivers the message packet to the host:

1) Initiated by media controller to deliver an internal event:

The NVDIMM-P generates a message packet and notifies it by asserting RD_RDY when the NVDIMM-P internal event occurs. After receiving a subsequent SEND command, the NVDIMM will transmit the message packet including the event information. The internal events are defined as follows:

- Internal Operation request (IOP)
- Interrupt (INT)
- Uncorrectable media Error (UE) of read request

Error RID return with POISON=1, VALID_ERR=1 and UE=1

2) Requested with a READ_STATUS command:

- A READ_STATUS command is received by the NVDIMM, requesting the NVDIMM-P to generate a message packet with status information. When the request is completed and the message packet is ready, the NVDIMM-P asserts the RD_RDY signal. After receiving a subsequent SEND command, the NVDIMM will transmit the STATUS information in a message packet. The message packet includes the following information. Refer to Section 0, “

Status register Read operation (READ_**STATUS**)” for more details.

- To request the completion of the power-up initialization (RDY_PWR)
When the internal initialization of NVDIMM-P controller is completed, a message packet with RDY_PWR=1 will be generated.
- To request the Available Write and PWRITE Credits
Message packet with Available Write and PWRITE Credits with VALID_WC=1 and VALID_PWC=1 will be generated.
- To request the RESET_RID (RDY_RID)
When all pending RID and output buffers for SEND command are cleared, a message packet with RDY_RID =1 will be generated.

Table 12 - NVDIMM-P Message Packet Format

	Name	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7	
DQ0	ERR_ALERT	VALID_ERR ^[1]	UE	RFU	RFU	RFU	RFU	RFU	RFU	
DQ1	RDY	RDY_PWR ^{[1][2]}	RFU	RFU	RFU	RDY_RID ^[3]	RFU	RFU	RFU	
DQ2	Available WC	VALID_WC ^[1]	User-defined CTH[2:0] ^[4]			Available WC[11:8]				
DQ3		Available WC [7:0]								
DQ4	IOP	VALID_IOP ^[1]	RFU	RFU	RFU		Mode	QoS[1:0]		
DQ5		RFU	IOP Time Shift[1:0]		IOP Time Unit[4:0]					
DQ6	Available PWC	VALID_PWC ^[1]	User-defined CTH[2:0] ^[4]			Available PWC[11:8]				
DQ7		Available PWC [7:0]								
DQ8	Available UNMAP_CNT	VALID_UNMAP ^[1]	RFU	RFU	RFU	Available UNMAP_CNT [11:8]				
DQ9		Available UNMAP_CNT[7:0]								
...	...	...								
DQ18	Interrupt	VALID_INT ^[1]	ADDR_VALID	RFU	RFU	INT_TYPE[3:0]				
DQ19		INT_STATUS[7:0]								
DQ20		INT_ADDR[7:0]								
DQ21		INT_ADDR[15:8]								
DQ22		INT_ADDR[23:16]								
DQ23		INT_ADDR[31:24]								
DQ24		INT_ADDR[39:32]								
...		...								
DQ63		ERID[7:0](Error RID) ^[5]								
CB0~CB5	ECC	ECC					ECC			
CB6	META ^[6]	RFU	RFU	RFU	RFU	1	1	1	1	
CB7		POISON	WC[2] / CTH	WC[1] / RFU	WC[0] / RFU	1	1	1	1	

NOTE 1 VALID_xxx (1-bit): Indicates whether the corresponding information is valid or not. 1: Valid, 0: Invalid. Once the valid corresponding information with VALID_xxx='1' is delivered through message packet, the VALID_xxx is automatically cleared at next message packet if there is no corresponding event.

NOTE 2 RDY_PWR (1-bit): Indicates the media controller ready after the completion of media controller initialization. Normal RDY_PWR value in message packet is '0'. After a READ_STATUS[00] command is received, only one message packet with RDY_PWR=1 is delivered when the initialization is completed.

NOTE 3 RDY_RID (1-bit): Indicates the XREAD/SREAD command ready after the completion of RESET-RID operation. Normal RDY_RID value in message packet is '0'. After a READ_STATUS[11] command is received, only one message packet with RDY_RID =1 is delivered when all prior read-requests and output buffer (for SEND command) are cleared.

NOTE 4 User-defined Programmable Write Credits (3bits): Host can change this value by setting MR2 A[2:0]. Same CTH value is used for WC and PWC.

NOTE 5 POISON, UE and ERID(Error RID) : POISON=1 indicates Uncorrectable media error is detected on the read requested address by XREAD/SREAD. The RID of XREAD/SREAD is reported by ERID bits. Once this event (POISON=1, VALID_ERR=1, UE=1) is delivered through the message packet, the POISON, VALID_ERR and UE bits are automatically cleared. See section 7.1.4 "UE response of " for more details.

NOTE 6 Metadata order follows the order specified in F2RC4x DA[0]

3. Mode control and Status Register

The NVDIMM-P media controller includes both the DDR4 SDRAM Mode Register and DDR4 RCD Function space. Features supported in NVDIMM-P mirror the same DDR4 SDRAM MR and RCD address space. To support NVDIMM-P special functionality, several registers are added within this address space, which are defined in the following table.

Table 13 – NVDIMM-P special function registers

Register Name	Address
IOP mode0 enable/disable	MR1 A[6]
IOP mode1 enable/disable	MR1 A[5]
Interrupt enable/disable	MR1 A[17]
Credit Threshold	MR2 A[2:0]
Meta-data format(A or B)	MR2 A[13]
ECC enable/disable	MR3 A[13]
Advanced FIFO training mode enable/disable	MR6 A[8]
Internal media training start	MR6 A[9]
Training GuardKey enable/disable	MR6 A[13]
Media controller PLL/DLL locking status	MCW F2RC03-DA[0]
Media controller initialization status	MCW F2RC03-DA[1]
Meta-data ordering	MCW F2RC4x-DA[0]
tRRSE mode enable/disable	MCW F2RC4x-DA[1]
All-Zero Fail-Prevention enable/disable	MCW F2RC4x-DA[2]
Programmable READ(SEND) command delay	MCW F3RC00
Programmable WRITE command delay	MCW F3RC01

3.1 Mode Register

MR0

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	RFU	0 = must be programmed to 0 during MRS
A13, A11:9	WR	Write data Recovery time
A8	DLL Reset	0=NO, 1=YES
A7	TM	0=Normal, 1=Test
A12, A6,A5, A4, A2	CAS Latency (CL)	(See Table 15 ¹)
A3	Read Burst Type	0 = Sequential, 1 = Reserved
A1:A0	Burst Length	00 = 8 (Fixed) Abbreviated BL8MRS 01 = Reserved 10 = Reserved 11 = Reserved

NOTE The table only shows the encodings for a given CAS Latency (CL). For actual supported CAS Latency, please refer to speed bin tables for each frequency.

Table 14 - Write data Recovery time (cycles)

A13	A11	A10	A9	Write recovery dealy
0	0	0	0	10
0	0	0	1	12
0	0	1	0	14
0	0	1	1	16
0	1	0	0	18
0	1	0	1	20
0	1	1	0	24
0	1	1	1	22
1	0	0	0	26
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	0

Table 15 - CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25
1	0	0	0	1	26
1	0	0	1	0	27
1	0	0	1	1	28
1	0	1	0	0	29
1	0	1	0	1	30
1	0	1	1	0	31
1	0	1	1	1	32
1	1	0	0	0	Reserved

MR1

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	Interrupt	0 = Disable, 1 = Enable
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff ¹	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable, 1 = Reserved
A10:8	RTT_NOM	000 = RTT_NOM Disable, other = Reserved
A7	Write Leveling Enable	0 = Disable, 1 = Enable
A6	IOP mode 0	0 = Disable, 1 = Enable
A5	IOP mode 1	0 = Disable, 1 = Enable
A4:3	Additive Latency	00 = 0(AL disabled), other = Reserved
A2:1	Output Driver Impedance Control	(See Table 16)
A0	DLL Enable	0 = Disable, 1 = Enable

NOTE Outputs disabled - DQs, DQS_ts, DQS_cs.

Table 16 - Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

MR2

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	RFU	0 = must be programmed to 0 during MRS
A13	Write Credit Update Option	0 = 3 bit 1 = 1 bit
A12	Write CRC	0 = Disable, 1 = Reserved
A11:9	RTT_WR	000 = Dynamic ODT Off, other = Reserved
A8	RFU	0 = must be programmed to 0 during MRS
A7:6	Reserved	0 = must be programmed to 0 during MRS
A5:3	CAS Write Latency (CWL) ^[1]	(See Table 17)
A2:0	Credit Threshold(CTH)	000 = reserved, 001 = 1, 010 = 2, 011 = 4 100 = 8, 101 = 16, 110 = 32, 111 = 64

NOTE: CWL can be updated when MR6 A[13] (training guard key) is enabled.

Table 17 - CAS Write Latency (CWL)

A5	A4	A3	CWL	Speed Grade in MT/s for 1 tCK Write Preamble		Speed Grade in MT/s for 2 tCK Write Preamble	
				1 st Set	2 nd Set	1 st Set	2 nd Set
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	2933/3200	2400	2666	2400
1	1	0	18		2666	2933/3200	2666
1	1	1	20		2933/3200		2933/3200

NOTE The 2 tCK Write Preamble is valid for DDR4-2400/2666/3200 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional CWL is needed.

MR3

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	RFU	0 = must be programmed to 0 during MRS
A13	ECC disable	ECC disable mode in Normal mode 0 = ECC on, 1 : ECC off
A12:11	MPR Read Format	00 = Serial, 01 = Parallel, 10 = Staggered, 11 = Reserved
A10:9	Reserved	0 = must be programmed to 0 during MRS
A8:6	Reserved	0 = must be programmed to 0 during MRS
A5	Temperature sensor readout	0 = Disable, 1 = Reserved
A4	Per DRAM Addressability	0 = Disable, 1 = Reserved
A3	Reserved	0 = must be programmed to 0 during MRS
A2	MPR Operation	0 = Normal mode, 1 = Dataflow from/to MPR ^[1]
A1:0	MPR page Selection	00 = Page0, 10 = Page2, 01 = Page1, 11 = Page3 (See Table 17)

NOTE: In MPR Mode Training, MPR training patterns are accessed through both ECC check bits and DQ bits. MPR data are accessed through both DQ and CB bus.

Table 18 - MPR Data Format with MPR page 0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00=MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01=MPR1	0	0	1	1	0	0	1	1	
	10=MPR2	0	0	0	0	1	1	1	1	
	11=MPR3	0	0	0	0	0	0	0	0	

Table 19 - MPR Data Format with MPR page 2 (MPR Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note	
BA1:BA0	00=MPR0	REVD	REVD	REVD	Temperature Sensor Status		Write CRC Enable	RTT_WR		Read-only	
		-	-	MR2	-	-	MR2	MR2			
		-	-	A11	-	-	A12	A10	A9		
	01=MPR1	REVD	REVD								REVD
		MR6	MR6								MR3
		A6	A5	A4	A3	A2	A1	A0	A3		
	10=MPR2	CAS Latency					CAS Write Latency				
		MR0					MR2				
		A6	A5	A4	A2	A12	A5	A4	A3		
	11=MPR3	RTT_NOM			RTT_PARK			Driver Impedance			
		MR1			MR5			MR1			
A10		A9	A6	A8	A7	A6	A2	A1			

Table 20 - MPR Data Format with MPR page 3 (Vendor use only)¹

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00=MPR0	vendor	vendor	vendor	vendor	vendor	vendor	vendor	vendor	Read/Write
	01=MPR1	vendor	vendor	vendor	vendor	vendor	vendor	vendor	vendor	
	10=MPR2	vendor	vendor	vendor	vendor	vendor	vendor	vendor	vendor	
	11=MPR3	vendor	vendor	vendor	vendor	vendor	vendor	vendor	vendor	

NOTE: MPR page3 is specifically assigned to NVDIMM-P. Actual encoding method is vendor specific.

MR4

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	RFU	0 = must be programmed to 0 during MRS
A13	Reserved	0 = must be programmed to 0 during MRS
A12	Write Preamble	0 = 1nCK, 1 = 2nCK
A11	Read Preamble	0 = 1nCK, 1 = 2nCK
A10	Read Preamble Training Mode	0 = Disable, 1 = Enable
A9	Reserved	0 = must be programmed to 0 during MRS
A8:6	CS to CMD/ADDR Latency Mode	000 = Disable, others = Reserved
A5	Reserved	0 = must be programmed to 0 during MRS
A4	Reserved	0 = must be programmed to 0 during MRS
A3	Reserved	0 = must be programmed to 0 during MRS
A2	Reserved	0 = must be programmed to 0 during MRS
A1	Reserved	0 = must be programmed to 0 during MRS
A0	Clock Stopped Power Down Mode	0 = Disable, 1 = Enable

MR5

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17:13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable, 1 = Reserved
A11	Write DBI	0 = Disable, 1 = Reserved
A10	Data Mask	0 = Disable, 1 = Reserved
A9	Reserved	Reserved
A8:6	RTT_PARK ^[1]	(See Table 21)
A5	ODT Input Buffer during Power Down Mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A4	Reserved	Reserved
A3	Reserved	Reserved
A2:0	Reserved	Reserved

NOTE: RTT_PARK is defined for connections between the data buffer and the media controller.

Table 21 - RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

MR6

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1,BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	RFU	0 = must be programmed to 0 during MRS
A13	Training Guard Key	0 = Disabled,1 = Enabled
A12:10	tDLLK	(See Table 22)
A9	Internal Training Media	0 = NOP(No Operation),1 = Start
A8	Advanced Training FIFO	0 = Disabled,1 = Enabled ²
A7	Reserved	0 = must be programmed to 0 during MRS
A6	Reserved	0 = must be programmed to 0 during MRS
A5:0	Reserved	0 = must be programmed to 0 during MRS

NOTE: MR6 A[8](Advanced FIFO training) can be enabled when MR6 A[13] (training guard key) is enabled.

Table 22 - tDLLK

A12	A11	A10	tDLLKmin(nCK) ¹	Note
0	0	0	597	Data rate ≤ 1333Mbps
0	0	1		1333Mbps < Data rate ≤ 1866Mbps (1600/1866Mbps)
0	1	0	768	1866Mbps < Data rate ≤ 2400Mbps (2133/2400Mbps)
0	1	1	1024	2400Mbps < Data rate ≤ 2666Mbps (2666Mbps)
1	0	0		2666Mbps < Data rate ≤ 3200Mbps (2933/3200Mbps)
1	0	1	RFU	
1	1	0		
1	1	1		

MR7

MR7 is used for the MCW(Media controller Control Word) and BCW(Buffer Control Word).

3.2 Media controller Control Word

The control words are programmed by the host controller using the MRS function with DBG1, DBG0, DBA1, DBA0 = 0111b.

The control word is clocked in when DCS0_n is LOW, DACT_n is HIGH and DA16/RAS_n, DA15/CAS_n, DA14/WE_n are LOW. Both the address of the control word and the settings are transmitted over DA[12:0].

The reset default state of all control words (except vendor specific ones) is '0'. Every time the device is reset, its default state is restored. Stopping the clocks (CK_t=CK_c=LOW) to put the device in low-power mode will not alter the control word settings.

Table 23 - Function Space 0

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F0RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				Reserved	
F0RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				Reserved	
F0RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				Timing and IBT	
F0RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				Reserved	
F0RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				Reserved	
F0RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Reserved	
F0RC06	0	0	0	0	0	0	1	1	0	setting[3:0]				Command Space and Controller Word definition	
F0RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved	
F0RC08	0	0	0	0	0	1	0	0	0	setting[3:0]				Reserved	
F0RC09	0	0	0	0	0	1	0	0	1	setting[3:0]				Power Saving Settings	
F0RC0A	0	0	0	0	0	1	0	1	0	setting[3:0]				NVDIMM Operating Speed	
F0RC0B	0	0	0	0	0	1	0	1	1	setting[3:0]				Operating Voltage VDD and VREF Source	
F0RC0C	0	0	0	0	0	1	1	0	0	setting[3:0]				Training	
F0RC0D	0	0	0	0	0	1	1	0	1	setting[3:0]				DIMM Configuration	
F0RC0E	0	0	0	0	0	1	1	1	0	setting[3:0]				Parity	
F0RC0F	0	0	0	0	0	1	1	1	1	setting[3:0]				Command Latency Adder	
F0RC1x	0	0	0	0	1	setting[7:0]					Internal Vref				
F0RC2x	0	0	0	1	0	setting[7:0]					I2C Bus				
F0RC3x	0	0	0	1	1	setting[7:0]					Fine Granularity NVDIMM Operating Speed				
F0RC4x	0	0	1	0	0	setting[7:0]					CW Source Selection				
F0RC5x	0	0	1	0	1	setting[7:0]					CW Destination Selection				
F0RC6x	0	0	1	1	0	setting[7:0]					CW Data				
F0RC7x	0	0	1	1	1	setting[7:0]					IBT				
F0RC8x	0	1	0	0	0	setting[7:0]					ODT				
F0RC9x	0	1	0	0	1	setting[7:0]					Reserved				
F0RCAx	0	1	0	1	0	setting[7:0]					Reserved				
F0RCBx	0	1	0	1	1	setting[7:0]					IBT and MRS Snoop				
F0RCCx ... F0RCFx	0	1	1	x	x	setting[7:0]					CA Parity Error Log				

NOTE 1 F0RC7x CA Input Bus Termination bits cover the following CA inputs : DA17, DC0, DC1, DC2

NOTE 2 CKE power down mode is enabled

NOTE 3 Context for operation training

NOTE 4 Address mirroring for MRS commands is disabled.

NOTE 5 DODT0 input buffer and IBT ON and passed to QxODT[0] output. DODT1 input buffer and IBT is OFF and QxODT1 output buffer is OFF. If RC8x DA5 is not set to '1', DODT0 is passed to BODT.

Table 24 - Function Space 1

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F1RC00.	0	0	0	0	0	0	0	0	0	setting[3:0]				Data Buffer Interface Driver Characteristics Control Word	
F1RC01	0	0	0	0	0	0	0	0	0	1	setting[3:0]				Reserved
F1RC02	0	0	0	0	0	0	0	0	1	0	setting[3:0]				Reserved
F1RC03	0	0	0	0	0	0	0	0	1	1	setting[3:0]				Reserved
F1RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				Reserved	
F1RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Data Buffer Interface Output Slew Rate	
F1RC06	0	0	0	0	0	0	1	1	0	setting[3:0]				Reserved for future use	
F1RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved for future use	
F1RC08 ... F1RC0F	0	0	0	0	0	1	x	x	x	setting[3:0]				Reserved for future use	
F1RC1x ... F1RC7x	0	x	x	x	x	setting[7:0]									Reserved
F1RC8x	0	x	x	x	x	setting[7:0]									BCOM/BCKE/BODT Output Delay Control
F1RC9x	0	x	x	x	x	setting[7:0]									BCK Output Delay Control
F1RCAx ... F1RCFx	0	x	x	x	x	setting[7:0]									Reserved for future use

Table 25 - Function Space 2

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F2RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				Reserved for future use	
F2RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				Reserved for future use	
F2RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				Reserved for future use	
F2RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				NVDIMM-P controller status	
F2RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				Reserved for future use	
F2RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Reserved for future use	
F2RC06	0	0	0	0	0	0	1	1	0	setting[3:0]				Reserved for future use	
F2RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved for future use	
F2RC08 ... F2RC0F	0	0	0	0	0	1	x	x	x	setting[3:0]				Reserved for future use	
F2RC1x	0	0	0	0	1	setting[7:0]									Reserved for future use
F0RC2x	0	0	0	1	0	setting[7:0]									Reserved for future use
F0RC3x	0	0	0	1	1	setting[7:0]									NVDIMM-P controller status
F2RC4x	0	0	1	0	0	setting[7:0]									Packet and timing option Control
F2RC5x	0	0	1	0	1	setting[7:0]									Correctable Error Interrupt Threshold and Enable
F2RC6x	0	0	1	1	0	setting[7:0]									Error Injection Mode
F2RC7x	0	0	1	1	1	setting[7:0]									Error Address0/Mask0
F2RC8x	0	1	0	0	0	setting[7:0]									Error Address1/Mask1
F2RC9x	0	1	0	0	1	setting[7:0]									Error Address2/Mask2
F2RCAx	0	1	0	1	0	setting[7:0]									Error Address3/Mask3
F2RCBx	0	1	0	1	1	setting[7:0]									Error Address4/Mask4
F2RCCx ... F2RCFx	0	1	1	x	x	setting[7:0]									Urgent Error Log

Table 26 - Function Space 3

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F3RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				Programmable Read Command delay	
F3RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				Programmable Write Command delay	
F3RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				Reserved for future use	
F3RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				Reserved for future use	
F3RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				Reserved for future use	
F3RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Reserved for future use	
F3RC06	0	0	0	0	0	0	1	1	0	setting[3:0]				Reserved for future use	
F3RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved for future use	
F3RC08~F3RC09	0	0	0	0	0	1	0	0	x	setting[3:0]				VrefDQ0~3 Training	
F3RC0A~F3RC0B	0	0	0	0	0	1	0	1	x	setting[3:0]				VrefDQ4~7 Training	
F3RC0C~F3RC0D	0	0	0	0	0	1	1	0	x	setting[3:0]				VrefDQ8~11 Training	
F3RC0E~F3RC0F	0	0	0	0	0	1	1	1	x	setting[3:0]				VrefDQ12~15 Training	
F3RC1x	0	0	0	0	1	setting[7:0]					VrefDQ16~19 Training				
F3RC2x	0	0	0	1	0	setting[7:0]					VrefDQ20~23 Training				
F3RC3x	0	0	0	1	1	setting[7:0]					VrefDQ24~27 Training				
F3RC4x	0	0	1	0	0	setting[7:0]					VrefDQ28~31 Training				
F3RC5x	0	0	1	0	1	setting[7:0]					VrefDQ32~35 Training				
F3RC6x	0	0	1	1	0	setting[7:0]					VrefDQ36~39 Training				
F3RC7x	0	0	1	1	1	setting[7:0]					VrefDQ40~43 Training				
F3RC8x	0	1	0	0	0	setting[7:0]					VrefDQ44~47 Training				
F3RC9x	0	1	0	0	1	setting[7:0]					VrefDQ48~51 Training				
F3RCAx	0	1	0	1	0	setting[7:0]					VrefDQ52~55 Training				
F3RCBx	0	1	0	1	1	setting[7:0]					VrefDQ56~59 Training				
F3RCCx	0	1	1	0	0	setting[7:0]					VrefDQ60~63 Training				
F3RCDx	0	1	1	0	1	setting[7:0]					VrefDQ64~67 Training				
F3RCEx	0	1	1	1	0	setting[7:0]					VrefDQ68~72 Training				
F3RCFx	0	1	1	1	1	setting[7:0]					Reserved for future use				

Table 27 - Function Space 4

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F4RC8x~F4RCEx	0	0	0	0	0	1	x	x	x	setting[3:0]				Event Log	
F4RCFx	0	x	x	x	x	setting[7:0]				Reserved for future use					

Table 28 - Function Space 7

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F7RC00~F7RC0F	0	0	0	0	0	x	x	x	x	setting[3:0]				Reserved for Future use	
F7RC1x	0	0	0	0	1	setting[7:0]								Data code Byte 02 Year Information	
F7RC2x	0	0	0	1	0	setting[7:0]								Data code Byte 12 Work Week Information	
F7RC3x	0	0	0	1	1	setting[7:0]								Data code Byte 22 Reserved	
F7RC4x	0	0	1	0	0	setting[7:0]								Vendor specific unique unit code Byte 02	
F7RC5x	0	0	1	0	1	setting[7:0]								Vendor specific unique unit code Byte 12	
F7RC6x	0	0	1	1	0	setting[7:0]								Vendor specific unique unit code Byte 22	
F7RC7x	0	0	1	1	1	setting[7:0]								Vendor specific unique unit code Byte 32	
F7RC8x	0	1	0	0	0	setting[7:0]								Vendor specific unique unit code Byte 42	
F7RC9x	0	1	0	0	1	setting[7:0]								Vendor specific unique unit code Byte 52	
F7RCAx	0	1	0	1	0	setting[7:0]								Vendor specific unique unit code Byte 62	
F7RCBx	0	1	0	1	1	setting[7:0]								Vendor ID [7:0]3	
F7RCCx	0	1	1	0	0	setting[7:0]								Vendor ID [15:8]3	
F7RCDx	0	1	1	0	1	setting[7:0]								Device ID [7:0]3	
F7RCEx	0	1	1	1	0	setting[7:0]								Device ID [15:8]3	
F7RCFx	0	1	1	1	1	setting[7:0]								Revision ID [7:0]3	

Table 29 - F0RC02: Timing and IBT Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Reserved	Reserved
x	x	x	1		Reserved
x	x	0	x	DPA Input Bus Termination Disable ¹	Enable
x	x	1	x		Disable
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

Table 30 - F0RC06: Command Space Control Word definition

Setting (DA[3:0])				Command No	Command Name	Result
0	0	0	0	CMD0	SoftReset ¹	Resets state of Media controller. Sends reset to DB for 16 * tCK. Self Clear in the next cycle. Does NOT cause QRST_n assertion.
0	0	0	1	CMD1	DB Reset	Sends reset to DB for 16 * tCK. Does NOT reset Media controller.
0	0	1	0	CMD2	Reserved	Reserved
0	0	1	1	CMD3	Reserved	Reserved
0	1	0	0	CMD4	CW Read Operation	Sends selected CW (in CW source selection control word) to MPR page 0
0	1	0	1	CMD5	CW Write Operation	Writes “data” in CW data control word to selected CW (in CW source selection control word)
0	1	1	0	CMD6	Clear Parity Error	Clear ‘CA Parity Error Status’ bit and ‘> 1 Error’ bit and re-enable parity checking (if not already enabled)
0	1	1	1	CMD7	Reserved	Reserved
1	0	0	0	CMD8	Reserved	Reserved
1	0	0	1	CMD9	Soft Media controller Reset ^{1,2,3}	Resets state of Media controller. Self Clear in the next cycle. Does NOT cause QRST_n assertion and does NOT send reset to DB.
1	0	1	0	CMD10	Reserved	Reserved
1	0	1	1	CMD11	Reserved	Reserved for future use
1	1	0	0	CMD12	Reserved	Reserved for future use
1	1	0	1	CMD13	Reserved	Reserved for future use
1	1	1	0	CMD14	Reserved	Reserved for future use
1	1	1	1	CMD15	NOP	No Operation ⁴

NOTE:

1. Requires waiting for tSTAB
2. The DDR4DB01 must not be in MPR Read override mode or BCW Read mode and the DDR4DB01 F[7:0]BC7x control word should be cleared before issuing a Soft Media controller Reset.
3. For during Soft Media controller Reset the DDR4DB01 must be in CKE Power Down Mode
4. This operation was added specifically for hosts that don't support byte writes over the I2C Bus, i.e., that have to write more than one Media-controller Control Word(MCW) at the same time.

Table 31 - F0RC09: Power Saving Settings Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Reserved	Reserved
x	x	x	1		Reserved
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
1	0	x	x	CKE Power Down Mode ¹	CKE power down with IBT ON, QxODT are a function of DODTx. If RC8x DA[7:6] is configured as '00' or '01'. If RC8x DA[76] is configured as either '00' or '01', BODT is a function of DODTn.
1	1	x	x		CKE power down with IBT OFF, QxODT held LOW. If the BODT output is enabled, it is held LOW.
0	x	x	x	CKE Power Down Mode Enable ²	Disabled
1	x	x	x		Enabled

NOTE:

1. The register ignores CKE Power Down mode setting when CKE Power Down is disabled by RC09 DA3.
2. The media controller shall default to CKE Power Down Mode Disabled, upon power-up.

Table 32 - F0RC0A: NVDIMM Operating Speed¹

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	$f \leq 1600 \text{ MT/s}$	DDR4-1600
x	0	0	1	$1600 \text{ MT/s} < f \leq 1866 \text{ MT/s}$	DDR4-1866
x	0	1	0	$1866 \text{ MT/s} < f \leq 2133 \text{ MT/s}$	DDR4-2133
x	0	1	1	$2133 \text{ MT/s} < f \leq 2400 \text{ MT/s}$	DDR4-2400
x	1	0	0	$2400 \text{ MT/s} < f \leq 2666 \text{ MT/s}$	DDR4-2666
x	1	0	1	$2666 \text{ MT/s} < f \leq 2933 \text{ MT/s}$	DDR4-2933
x	1	1	0	$2933 \text{ MT/s} < f \leq 3200 \text{ MT/s}$	DDR4-3200
x	1	1	1	Reserved	Reserved
0	x	x	x	Context for operation training	Default; Context 1 operation
1	x	x	x		Context 2 operation

NOTE: The encoding value is used to inform the register the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a register can run.

Table 33 - F0RC0B: Operating Voltage VDD and VrefCA Source Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Register V _{DD} Operating Voltage ¹	1.2V
x	x	x	1		Reserved
x	0	0	x	QVrefCA and BVrefCA Source	V _{DD} / 2 ¹ connected to QVrefCA and BVrefCA
x	0	1	x		Internally generated Vref connected to QVrefCA ² V _{DD} / 2 ¹ connected to BVrefCA
x	1	0	x		Internally generated Vref connected to BVrefCA ² V _{DD} / 2 ¹ connected to QVrefCA
x	1	1	x		External VrefCA input connected to QVrefCA and BVrefCA
0	x	x	x		Internally generated Vref ²
1	x	x	x	Input Receiver Vref Source	External VrefCA input

NOTE:

1. V_{DD} / 2 is also internally generated, but not by the VrefCA DAC.
2. Value programmed in RC1x. There is only one internal Vref generator. If more than one destination is configured for internally generated Vref, then they will all receive the same Vref level.

Table 34 - F0RC0C: Training Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	Training mode selection	Normal operating mode
x	0	0	1		Clock-to-CA training mode ¹
x	0	1	0		DCS0_n loopback mode ¹
x	0	1	1		Reserved
x	1	0	0		DCKE0_n loopback mode ¹
x	1	0	1		Reserved
x	1	1	0		DODT0_n loopback mode ¹
x	1	1	1		Reserved
0	x	x	x	Reserved for future use	Reserved for future use
1	x	x	x		Reserved for future use

NOTE In these training modes the Media controller 01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals).

Table 35 - F0RC0D: DIMM Configuration Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	Reserved	Reserved
x	x	0	1		Reserved
x	x	1	0		Reserved
x	x	1	1		Reserved
x	0	x	x	DIMM Type	LRDIMM
x	1	x	x		Reserved
0	x	x	x	Address mirroring for MRS commands	Disabled
1	x	x	x		Reserved

Table 36 - F0RC0E: Parity and ALERT Configuration Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Parity Enable	Parity checking disabled ¹
x	x	x	1		Parity checking enabled. Command ² must be delayed ^{3,4}
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
x	0	x	x	ALERT_n Assertion ⁵	ALERT_n stays asserted until 'Clear CA Parity Error' command is sent
x	1	x	x		ALERT_n pulse width according to Table 9
0	x	x	x	ALERT_n Re-enable ⁶	Parity checking remains disabled after ALERT_n pulse
1	x	x	x		Parity checking is re-enabled after ALERT_n pulse

NOTE:

1. Register does not check for parity including control word programming.
2. Command includes A0 .. A17, BA0 .. BA1, BG0 .. BG1, ACT_n, C0 .. C2, CKE0, ODT0, CS0_n .. CS3. It also includes BCOM[3:0], BODT and BCKE if the buffer control bus is enabled.
3. As specified in Table 128
4. At least 1 nCK for $\leq 2400\text{MT/s}$; at least 2 nCK for $> 2400\text{MT/s}$
5. This bit only affects ALERT_n assertion that is a result of a CA parity error. In case of a LOW level on the ERROR_IN_n input, ALERT_n stays asserted as long as ERROR_IN_n remains LOW unless DRST_n is LOW or the device is in clock stopped power down mode.
6. CA Parity Error Status bit in Error Log Register remains set until cleared by sending a Clear CA Parity Error command.