

JEDEC STANDARD

DDR5 Unbuffered Dual Inline Memory Module (UDIMM) Common Standard

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DDR5 UNBUFFERED DUAL INLINE MEMORY MODULE (UDIMM) COMMON STANDARD

From JEDEC Board Ballot JCB-21-55, formulated under the cognizance of the JC-45.3 Subcommittee on Unbuffered DRAM Modules, item number 2265.02B.

1 Scope

This standard defines the electrical and mechanical requirements for 288-pin, 1.1 V (VDD), Unbuffered, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR5 SDRAM UDIMMs). These DDR5 Unbuffered DIMMs (UDIMMs) are intended for use as main memory when installed in Computers.

Reference design examples are included which provide an initial basis for DDR5 UDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC5-4000, PC5-4400, PC5-4800 and beyond PC5-6400 support. All DDR5 UDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

2 Related Standards

- JESD79-5: DDR5 SDRAM Standard
- JESD300-5: SPD5118 Hub and Serial Presence Detect Device Standard
- JESD301-2: PMIC5100 Power Management Integrated Circuit (PMIC) Device Standard
- JESD400-5: DDR5 Serial Presence Detect (SPD) Contents
- JESD401-5: DDR5 DIMM Label
- JESD403-1: JEDEC Module Sideband Bus
- MO-210: Plastic Bottom Grid Array, 0.80 mm Pitch, Rectangular Family Package
- MO-329: 288 pin DDR5 DIMM, 0.85 mm Pitch

3 Product Family Attributes

Table 1 —Product Family Attributes

	x64 (x32 2 channels), x72 ECC (x36 2channels)	
DIMM Dimensions (nominal)	133.35 mm x 31.25 mm	MO-329
Pin Count	288	
DDR5 SDRAMs Supported	16 Gb, 24 Gb, 32 Gb, 64 Gb	MO-210
Capacity	2 GB - 128 GB	
DDR5 SDRAM width	x8, x16	
Serial Presence Detect, Thermal Sensor	1024 byte	JESD300-5
PMIC	PMIC5100	JESD301-2
Voltage Options	5 V (VIN_BULK)	
Interface	1.1 V signaling	

4 Environmental Requirements

288-pin Unbuffered DDR5 SDRAM DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Table 2 — Environmental Parameters (Example)

Symbol	Parameter	Rating	Units	
TOPR	DRAM Operating Temperature	0 to +95	°C	
TSTG	Storage Temperature	-55 to +100	°C	
NOTE 1 Operating temperature applies to the case temperature of all SDRAM components on the module. All other support components on the module must remain within their respective operating temperature ranges when the case temperature of the SDRAMs are at the minimum and maximum values. See JESD402-1 for details. NOTE 2 Storage temperature applies to the case temperature of all components on the module. See JESD402-1 for details. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.				

5 Connector Pinout and Signal Description

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command/Address bus	HSCL	SidebandBus clock
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select	HSDA	SidebandBus data
DQ0_A – DQ31_A, DQ0_B – DQ31_B	DIMM memory data bus	HSA	SidebandBus address
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits	ALERT_n	SDRAM ALERT_n
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set DRAMs to a Known State
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)	VIN_BULK	5 V power input supply to the PMIC for analog circuits
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks	VSS	Power supply return (ground)
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)	PWR_GOOD	Power good indicator
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)	PWR_EN	PMIC Enable
		RFU	Reserved for future use
NOTE 1 DDR5 UDIMM has 2 channels (channel-A and channel-B) of signal bus. The signals with suffix: _A (e.g., DQ0_A) are for channel-A, and the signals with suffix: _B (e.g., DQ0_B) are for channel-B			

5 Connector Pinout and Signal Description (cont'd)

Table 4 — Input/Output Functional Description

Symbol	Type	I/O Level	Function
CK0_A_t, CK0_A_c CK1_A_t, CK1_A_c, CK0_B_t, CK0_B_c CK1_B_t, CK1_B_c	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA12_A, CA0_B - CA12_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus.
CS0_A_n - CS1_A_n CS0_B_n - CS1_B_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DQ0_A - DQ31_A DQ0_B - DQ31_B	Input/ Output	VDDQ	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode Register, then CRC code is added at the end of Data Burst.
CB0_A - CB3_A CB0_B - CB3_B	Input/ Output	VDDQ	DIMM ECC check bits
DQS0_A_t - DQS4_A_t DQS0_A_c - DQS4_A_c DQS0_B_t - DQS4_B_t DQS0_B_c - DQS4_B_c	Input/ Output	VDDQ	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n - DM3_A_n DM0_B_n - DM3_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1.
ALERT_n	Input/ Output	VDD	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	VDDQ	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.

Table 4 — Input/Output Functional Description (cont'd)

Symbol	Type	I/O Level	Function
HSCL	Input	1.0 V	Host SidebandBus bus clock, supplied by the controller.
HSDA	Input / Output	1.0 V	Host SidebandBus data, connected from the controller to Hub or Host bus Target devices.
HSA	Input	2.1 V max	Host SidebandBus bus device ID address pin; input to a Hub or other client device to distinguish between identical devices in the I3C-Basic address range.
RFU			Reserved for Future Use. No on DIMM electrical connection is present.
PWR_GOOD	Input / Output	Open Drain	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceed the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
PWR_EN	Input	3.3 V	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This signal is connected to PMIC's VR_EN pin.
VIN_BULK	Supply	5 V	5 V power input supply to the PMIC for analog circuits.
VSS	Supply		Ground

5.1 DDR5 UDIMM Connector Pin Assignments

Table 5 — DDR5 288 Pin UDIMM Pin Wiring Assignments

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	VIN_BULK	145	VIN_BULK	75	RFU	219	RFU
2	RFU	146	VIN_BULK	KEY			
3	RFU	147	PWR_GOOD	76	RFU	220	RFU
4	HSCL	148	HSA	77	VSS	221	VSS
5	HSDA	149	RFU	78	CK0_B_t	222	CK1_B_t
6	VSS	150	VSS	79	CK0_B_c	223	CK1_B_c
7	RFU	151	PWR_EN	80	VSS	224	VSS
8	VSS	152	RFU	81	RFU	225	RFU
9	DQ0_A	153	VSS	82	CA12_B	226	RFU
10	VSS	154	DQ2_A	83	VSS	227	VSS