

JEDEC STANDARD

DDR5 UDIMM Raw Card Annex A

JESD308-U0-RCA Version 1.0

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DDR5 UDIMM RAW CARD ANNEX A

From JEDEC Board Ballet JCB-22-16, formulated under the cognizance of the JC-45.3 Subcommittee on Unbuffered DRAM Modules, item 2265.13A.

1 Scope

This annex JESD308-U0-RCA, DDR5 Unbuffered Dual Inline Memory Module (UDIMM) Raw Card A Annex defines the design detail of x8, 1 Package Rank DDR5 UDIMM. The common feature of DDR5 UDIMM such as the connector pinout can be found in the JESD308, DDR5 Unbuffered Dual Inline Memory Module (UDIMM) Common Standard.

2 DDR5 Unbuffered DIMM Design File**Table 1 — DDR5 UDIMM Design File**

Raw Card	Applicable Design File	Applicable BOM
A0	PC5-UDIMM_RC_A0_R100_20210721.brd	PC5-UDIMM_RC_A0_R100_20210721_BOM.xlsx
NOTE "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.		

3 Module Configuration**Table 2 — Module Configuration**

SDRAM			DIMM					
Die Density	Organi- zation	Pkg Type	Maximum Capacity	Organi- zation	No. of SDRAM Die on DIMM	No. of Package Ranks	No. of Address Signals Row / Col	MO-329 Variation
16 Gb	2G x 8	SDP	16 GB	2G x 64	8	1	16 / 10	ABxB
24 Gb	3G x 8	SDP	24 GB	3G x 64	8	1	17 / 10	ABxB
32 Gb	4G x8	SDP	32 GB	4G x 64	8	1	17 / 10	ABxB