

JEDEC STANDARD

DDR5 UDIMM Raw Card Annex C

JESD308-U0-RCC Version 1.0

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DDR5 UDIMM RAW CARD ANNEX C

From JEDEC Board Ballet JCB-22-18, formulated under the cognizance of the JC-45.3 Subcommittee on Unbuffered DRAM Modules, item 2265.08A.

1 Scope

This annex JESD308-U0-RCC, “DDR5 Unbuffered Dual Inline Memory Module (UDIMM) Raw Card C Annex” defines the design detail of x16, 1 Package Ranks DDR5 UDIMM. The common feature of DDR5 UDIMM such as the connector pinout can be found in the JESD308, DDR5 Unbuffered Dual Inline Memory Module (UDIMM) Common Standard.

2 DDR5 Small Outline DIMM Design File

Table 1 — DDR5 UDIMM Design File

Raw Card	Applicable Design File	Applicable BOM
C0	PC5-UDIMM_RC_C0_R100_20210720.brd	PC5-UDIMM_RC_C0_R100_20210720_BOM.xlsx
NOTE “Reference” design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.		

3 Module Configuration

Table 2 — Module Configuration

SDRAM			DIMM					
Die Density	Organization	Pkg Type	Maximum Capacity	Organization	No. of SDRAM Die on DIMM	No. of Package Ranks	No. of Address signals Row / Col	MO-329 Variation
16 Gb	1G x 16	SDP	8 GB	1G x 32 x 2	4	1	16 / 10	ABxB
24 Gb	1.5G x 16	SDP	12 GB	1.5G x 32 x 2	4	1	17 / 10	
32 Gb	2G x16	SDP	16 GB	2G x 32 x 2	4	1	17 / 10	