

JEDEC STANDARD

DDR5 UDIMM Raw Card Annex D

JESD308-U4-RCD Version 1.0

JULY 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2022
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2108

JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

This page intentionally left blank

DDR5 UDIMM Raw Card Annex D

Contents

	Page
1 Scope.....	1
2 DDR5 Small Outline DIMM Design File	1
3 Module Configuration.....	1
4 SDRAM Configuration	2
5 Supported Speeds.....	2
6 Design Deviations	2
7 General Layout.....	3
8 Functional Block Diagram	4
9 Sideband Bus Routing.....	6
10 Clock Net Structure.....	7
11 Data Net Structure – DQ, CB, DQS_t, DQS_c.....	8
12 Address and Command Net Structure Routing	9
13 Control Net Structure Routing	10
14 DIMM Impedance Profile.....	11
15 ALERT_n Net Structure Routing.....	12
16 RESET_n Net Structure Routing	13
17 Cross Section Recommendations.....	14

Tables

Table 1 — DDR5 UDIMM Design File.....	1
Table 2 — Module Configuration.....	1
Table 3 — SDRAM Configuration	2
Table 4 — Supported Speeds	2
Table 5 — Design Deviations	2
Table 6 — Trace Lengths for Host and Local Signals	6
Table 7 — Trace Lengths for Clock to SDRAM Load Net Structures	7
Table 8 — Trace Lengths for DQ[31:00]_A, CB[03:00]_A, DQS[04:00]_t_A, DQS[04:00]_c_A, DQ[31:00]_B, CB[03:00]_B, DQS[04:00]_t_B, DQS[04:00]_c_B.....	8
Table 9 — Trace Lengths for Address and Command Net Structures	9
Table 10 — Trace Lengths for Control Net Structures	10

Contents (cont'd)

Table 11 — Voltage Operating Conditions	11
Table 12 — Trace Lengths for ALERT_n Net Structures	12
Table 13 — Trace Lengths for RESET_n Net Structures	13
Table 14 — PCB Fabrication Table	14

Figures

Figure 1 — General Layout	3
Figure 2 — X72 DIMM, Populated as One Package Ranks of x8 DDR5 SDRAMs (Part 1 of 3)	4
Figure 3 — X72 DIMM, Populated as One Package Ranks of x8 DDR5 SDRAMs (Part 2 of 3)	5
Figure 4 — X72 DIMM, Populated as One Package Ranks of x8 DDR5 SDRAMs (Part 3 of 3)	6
Figure 5 — Net Structure Routing for Clock to SDRAM Loads CK00_C_[B:A], CK00_T_[B:A]	7
Figure 6 — Net Structure Routing for DQ, CB, DQS_t, DQS_c	8
Figure 7 — Net Structure Routing for CA[12:00]_[B:A]	9
Figure 8 — Net Structure Routing for CS00_[B:A]	10
Figure 9 — DIMM Impedance Profile	11
Figure 10 — Net Structure Routing for ALERT_n	12
Figure 11 — Net Structure Routing for RESET_n	13

DDR5 UDIMM RAW CARD ANNEX D

From JEDEC Board Ballet JCB-22-19, formulated under the cognizance of the JC-45.3 Subcommittee on Unbuffered DRAM Modules, item 2265.14A.

1 Scope

This annex JESD308-U4-RCD, DDR5 Unbuffered Dual Inline Memory Module with 4-bit ECC (EC4 UDIMM) Raw Card D Annex defines the design detail of x8, 1 Package Rank DDR5 UDIMM with 4-bit ECC. The common feature of DDR5 UDIMM such as the connector pinout can be found in the JESD308, DDR5 Unbuffered Dual Inline Memory Module (UDIMM) Common Standard.

2 DDR5 Small Outline DIMM Design File

Table 1 — DDR5 UDIMM Design File

Raw Card	Applicable Design File	Applicable BOM
D0	PC5-UDIMM_RC_D0_R100_20210721.brd	PC5-UDIMM_RC_D0_R100_20210721_BOM.xlsx
NOTE "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.		

3 Module Configuration

Table 2 — Module Configuration

SDRAM			DIMM					
Die Density	Organization	Pkg Type	Maximum Capacity	Organization	No. of SDRAM Die on DIMM	No. of Package Ranks	No. of Address signals Row / Col	MO-329 Variation
16 Gb	2G x 8	SDP	16 GB	2G x 72	10	1	16 / 10	ABxB
24 Gb	3G x 8	SDP	24 GB	3G x 72	10	1	17 / 10	
32 Gb	4G x 8	SDP	32 GB	4G x 72	10	1	17 / 10	