

JEDEC STANDARD

Compression Attached Memory Module (CAMM2) Common Standard

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COMPRESSION ATTACHED MEMORY MODULE (CAMM2) COMMON STANDARD

From JEDEC Board Ballet JCB-23-56, formulated under the cognizance of the JC-45 committee on DRAM Modules, item 2290.07B.

1 Scope

This standard defines the electrical and mechanical requirements for Double Data Rate, Synchronous DRAM Compression-Attached Memory Modules (DDR5 SDRAM CAMM2s) and Low Power Double Data Rate, Synchronous DRAM Compression-Attached Memory Modules (LPDDR5/5X SDRAM CAMM2s). These DDR5 and LPDDR5/5X CAMM2s are intended for use as main memory when installed in computers, laptops, and other systems.

“CAMM” is general language to describe the module category. CAMM2 is this JEDEC standard version while prior CAMMs have been proprietary.

Reference design examples are included which provide an initial basis for CAMM2 designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC5-6400, and beyond. CAMM2 with LPDDR5 DRAM is expected to start at 6400 MTs and increment upward in cadence with the DRAM speed capabilities. All CAMM2 implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Related specifications:

- JESD79-5: DDR5 SDRAM specification
- JESD209-05A: LPDDR5 SDRAM specification
- JESD300-5: SPD5118 Hub and Serial Presence Detect Device Specification
- JESD301-2: PMIC5100 DDR Power Management Integrated Circuit (PMIC) Device Specification
- JESD301-3: PMIC52x0 LPDDR5/5X Power Management Integrated Circuit (PMIC) Device Specification
- JESD400-5: DDR Serial Presence Detect (SPD) Contents
- JESD406-5: LPDDR Serial Presence Detect (SPD) Contents
- JESD401-5: DDR5 DIMM Label
- JESD401-5: LPDDR5/5X DIMM Label
- JESD403-1: JEDEC Module Sideband Bus
- MO-210: Plastic Bottom Grid Array, 0.80 mm Pitch, Rectangular Family Package
- MO-338: 315-ball, pattern A CAMM2 Package

1 Scope (cont'd)

Table 1 — Product Family Attributes

Module Organization	DDR x64 (x32, 2 subchannels) = Single Channel CAMM2 DDR x72 ECC (x36, 2 subchannels) = Single Channel CAMM2 DDR x128(x32, 4 subchannels) = Dual Channel CAMM2 DDR x144 ECC (x36, 4 subchannels) = Dual Channel CAMM2 LPDDR x128 (x16, 8 subchannels)	
Module Dimensions (nominal)	Various form factors with X = 78 mm, Y = 29.6to 68 mm	MO-357 MO-358
Pin Count and Pitch	Variation AXXX for dual-channel CAMM2: 356 pins on 1.0 x 1.38 mm centers with ground shields interposed between rows Variation BXXX for single-channel CAMM2s: 178 pins on 1.0 x 1.38 mm centers with ground shields interposed between rows Variation CXXX for dual-channel CAMM2s: 644 pins on 1.0 x 1.38 mm centers with no ground shields:	SO-032
DDR5 SDRAMs Supported	16 Gb, 24 Gb, 32 Gb	MO-210
LPDDR5/5X SDRAMs supported	32 Gb (2x16), 64 Gb(4x16), 128 Gb (8x8)	
Capacity	8 GB - 128 GB	
SDRAM width	X8 DDR5, x16 DDR5, x32 LPDDR5/5X	
Serial Presence Detect with Thermal Sensor	1024 byte	JESD300-5
PMIC	PMIC5100 for DDR5 PMIC5200 for LPDDR5/5X	JESD301-2 – DDR5 JESD301-3 for LPDDR5/5X
Input voltage	5V (VIN_BULK)	JESD301-2 – DDR5 JESD301-3 for LPDDR5/5X
Interface	1.1 V signaling for DDR5 0.5 V DQ/DQS/WCK (diff) signaling for LPDDR5/5X 1.05 V Addr/Clock(diff) signaling for LPDDR5/5X	

2 Environmental Requirements

CAMM2s are intended for use in these environments:

- Mobile computing environments that have limited capacity for heat dissipation.
- Standard office environments for desktop and AIO systems that have heating and air conditioning.

Table 2 — Environmental Parameters

Symbol	Parameter	Rating	Units	
TOPR	DDR5 DRAM Operating Temperature	0 to +85 0 to +95	°C	1x Refresh 2x Refresh
TOPR	LPDDR5 DRAM Operating Temperature	0 to +85	°C	Per JESD209-5 Table 400
TSTG	Storage Temperature	-55 to +100	°C	
NOTES: 1. Operating temperature applies to the case temperature of all SDRAM components on the module. All other support components on the module must remain within their respective operating temperature ranges when the case temperature of the SDRAMs is at the minimum and maximum values. See JESD402-1 for details. 2. Storage temperature applies to the case temperature of all components on the module. See JESD402-1 for details. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.				

3 Connector Pinouts and Signal Descriptions

3.1 Power, Ground, and Sideband Signal Descriptions

Table 3 — Power, Ground, and Sideband Signal Descriptions

Signal	Type	I/O Level	Function
ALERT_n	Input/ Output	VDD	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Use of this signal is system dependent. Pull up pin to VDDQ.
HSA	Input	2.1 V max	Host Sideband Bus device ID address pin: input to a Hub or other client device to distinguish between identical devices in the I3C-Basic/I2C address range.
HSCL	Input	1.0 V	Host Sideband Bus clock, supplied by the controller.
HSDA	Input/ Output	1.0 V	Host Sideband Bus data, connected from the controller to Hub or Host bus Target devices.
PWR_EN	Input	1.8 V or 3.3 V	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This signal is connected to PMIC's VR_EN pin. Recommended pullup to 1.8 V. PMIC is 3.3 V tolerant.
PWR_GOOD	Input/ Output	Open Drain	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceed the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.

Table 3 — Power, Ground, and Sideband Signal Descriptions (cont'd)

Signal	Type	I/O Level	Function
RESET_n	Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.
RFU	NA	NA	Reserved for Future Use. No electrical connection is present on CAMM2. Motherboards must pull down these RFU's to assure no unintended effects of floating pins.
RFU DDR6	NA	NA	Reserved for Future Use. These locations are not populated with pins in the current CAMM2 connector but are intentionally spaced at 1 x 1.14 mm such that a future standard could add contacts at these locations.
UNLOCK	Input	1.8 V	If PMIC supports UNLOCK, then when this pin is high upon assertion of VR_EN, the PMIC register bit 0x2F[2] is set high and follows the UNLOCK pin state. When this pin is low upon assertion of VR_EN, then 0x2F[2] is set low and the PMIC enters regulation with registers locked. 220K ohm pulldown to ground on module at PMIC input is required to default to secure state. 22K ohm pull up on motherboards is recommended to indicate support for UNLOCK at VR_EN assertion. Support is optional but highly recommended for new designs that can drive UNLOCK from a secure GPIO source.
VIN_BULK	Supply	4.25 - 5.5 V	5 V (nom) power input supply to the PMIC for analog circuits.
NOTES: Sideband signals may be represented with signal suffix _0 or _1 to indicate channel number. CAMM2 designs must use the sideband signals with _0 suffix. The use of _0 and _1 suffix occurs on motherboard designs that support mechanical stacking of single-channel CAMM2			

3.2 DDR5 Signal Descriptions

Table 4 — DDR5 Signal Descriptions

Signal	Type	I/O Level	Function
CLK[3:0]_t CLK[3:0]_c	Input	VDD	Clock: CLK_t and CLK_c are differential clock inputs. All address and control input signals are sampled when crossing the positive edge of CLK_t and negative edge of CLK_c.
CA[12:0]	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus.
CS[3:0]_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks.
DQ[31:0]	Input/ Output	VDDQ	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst.
CB[3:0]	Input/ Output	VDDQ	DIMM ECC check bits
DQS[4:0]_t DQS[4:0]_c	Input/ Output	VDDQ	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended. (DQS[4] is for ECC)
DMI[3:0]_n	Input	VDDQ	Data Mask Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1.
NOTES: - Subchannel groups are represented with signal prefixes DDR0A_, DDR0B_, DDR1A_, and DDR1B_. All the above signals are duplicated for each subchannel. - Informative: In other documents, CLK naming uses a convention of CLK[1:0]_[1:0][B:A]_t/c for A and B Channels and two Channels [1:0]. The naming conversions are: - DDR0A_CLK0_t = CLK0_0A_t and DDR0A_CLK0_c = CLK0_0A_c - DDR0B_CLK1_t = CLK0_0B_t and DDR0B_CLK1_c = CLK0_0B_c - DDR1A_CLK0_t = CLK1_0A_t and DDR1A_CLK2_c = CLK1_0A_c - DDR1B_CLK1_t = CLK1_0B_t and DDR1B_CLK3_c = CLK1_0B_c			

3.3 DDR5 Single-Channel CAMM2 Connector Pin Assignments

		MOUNTING																							
		HOLE																							
		24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	
A	DDR	GND Shield																							
	A	D0R8_C4[0]	VSS8_C4[1]	VSS8_C4[5]	D0R8_C4[6]	VSS8_C4[7]	VSS8_C4[8]	VSS8_C4[9]	VSS8_C4[10]	VSS8_C4[11]	VSS8_C4[12]	VSS8_C4[13]	VSS8_C4[14]	VSS8_C4[15]	VSS8_C4[16]	VSS8_C4[17]	VSS8_C4[18]	VSS8_C4[19]	VSS8_C4[20]	VSS8_C4[21]	VSS8_C4[22]	VSS8_C4[23]	VSS8_C4[24]		
B	DDR	VSS Shield																							
	B	VSS8_C4[0]	VSS8_C4[1]	VSS8_C4[5]	D0R8_C4[6]	VSS8_C4[7]	VSS8_C4[8]	VSS8_C4[9]	VSS8_C4[10]	VSS8_C4[11]	VSS8_C4[12]	VSS8_C4[13]	VSS8_C4[14]	VSS8_C4[15]	VSS8_C4[16]	VSS8_C4[17]	VSS8_C4[18]	VSS8_C4[19]	VSS8_C4[20]	VSS8_C4[21]	VSS8_C4[22]	VSS8_C4[23]	VSS8_C4[24]		
C	DDR	VSS Shield																							
	C	D0R8_C4[0]	VSS8_C4[1]	VSS8_C4[5]	D0R8_C4[6]	VSS8_C4[7]	VSS8_C4[8]	VSS8_C4[9]	VSS8_C4[10]	VSS8_C4[11]	VSS8_C4[12]	VSS8_C4[13]	VSS8_C4[14]	VSS8_C4[15]	VSS8_C4[16]	VSS8_C4[17]	VSS8_C4[18]	VSS8_C4[19]	VSS8_C4[20]	VSS8_C4[21]	VSS8_C4[22]	VSS8_C4[23]	VSS8_C4[24]		
D	DDR	VSS Shield																							
	D	D0R8_C4[0]	VSS8_C4[1]	VSS8_C4[5]	D0R8_C4[6]	VSS8_C4[7]	VSS8_C4[8]	VSS8_C4[9]	VSS8_C4[10]	VSS8_C4[11]	VSS8_C4[12]	VSS8_C4[13]	VSS8_C4[14]	VSS8_C4[15]	VSS8_C4[16]	VSS8_C4[17]	VSS8_C4[18]	VSS8_C4[19]	VSS8_C4[20]	VSS8_C4[21]	VSS8_C4[22]	VSS8_C4[23]	VSS8_C4[24]		
E	DDR	VSS Shield																							
	E	VSS8_C4[0]	VSS8_C4[1]	VSS8_C4[5]	D0R8_C4[6]	VSS8_C4[7]	VSS8_C4[8]	VSS8_C4[9]	VSS8_C4[10]	VSS8_C4[11]	VSS8_C4[12]	VSS8_C4[13]	VSS8_C4[14]	VSS8_C4[15]	VSS8_C4[16]	VSS8_C4[17]	VSS8_C4[18]	VSS8_C4[19]	VSS8_C4[20]	VSS8_C4[21]	VSS8_C4[22]	VSS8_C4[23]	VSS8_C4[24]		
F	DDR	VSS Shield																							
	F	D0R8_C4[0]	VSS8_C4[1]	VSS8_C4[5]	D0R8_C4[6]	VSS8_C4[7]	VSS8_C4[8]	VSS8_C4[9]	VSS8_C4[10]	VSS8_C4[11]	VSS8_C4[12]	VSS8_C4[13]	VSS8_C4[14]	VSS8_C4[15]	VSS8_C4[16]	VSS8_C4[17]	VSS8_C4[18]	VSS8_C4[19]	VSS8_C4[20]	VSS8_C4[21]	VSS8_C4[22]	VSS8_C4[23]	VSS8_C4[24]		
G	DDR	VSS Shield																							
	G	D0R8_C4[0]	VSS8_C4[1]	VSS8_C4[5]	D0R8_C4[6]	VSS8_C4[7]	VSS8_C4[8]	VSS8_C4[9]	VSS8_C4[10]	VSS8_C4[11]	VSS8_C4[12]	VSS8_C4[13]	VSS8_C4[14]	VSS8_C4[15]	VSS8_C4[16]	VSS8_C4[17]	VSS8_C4[18]	VSS8_C4[19]	VSS8_C4[20]	VSS8_C4[21]	VSS8_C4[22]	VSS8_C4[23]	VSS8_C4[24]		

3.4 DDR5 Single-Channel Pinout Table

Table 5 — DDR5 Single-Channel CAMM2 Connector Pin Wiring Assignments

SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER
ALERT0_n	F46		
DDR0A_CA[0]	D29	DDR0B_CA[0]	D18
DDR0A_CA[1]	A28	DDR0B_CA[1]	A19
DDR0A_CA[10]	A24	DDR0B_CA[10]	A23
DDR0A_CA[11]	B25	DDR0B_CA[11]	B22
DDR0A_CA[12]	C24	DDR0B_CA[12]	C23
DDR0A_CA[2]	C28	DDR0B_CA[2]	C19
DDR0A_CA[3]	E28	DDR0B_CA[3]	E19
DDR0A_CA[4]	B27	DDR0B_CA[4]	B20
DDR0A_CA[5]	A26	DDR0B_CA[5]	A21
DDR0A_CA[6]	C26	DDR0B_CA[6]	C21
DDR0A_CA[7]	D27	DDR0B_CA[7]	D20
DDR0A_CA[8]	E26	DDR0B_CA[8]	E21
DDR0A_CA[9]	D25	DDR0B_CA[9]	D22
DDR0A_CB4[0]	B31	DDR0B_CB4[0]	B16
DDR0A_CB4[1]	D31	DDR0B_CB4[1]	D16
DDR0A_CB4[2]	C32	DDR0B_CB4[2]	C15
DDR0A_CB4[3]	E32	DDR0B_CB4[3]	E15
DDR0A_CLK0_c	G25	DDR0B_CLK0_c	G22
DDR0A_CLK0_t	F25	DDR0B_CLK0_t	F22
DDR0A_CLK1_c	G27	DDR0B_CLK1_c	G20
DDR0A_CLK1_t	F27	DDR0B_CLK1_t	F20
DDR0A_CLK2_c	G31	DDR0B_CLK2_c	G16
DDR0A_CLK2_t	F31	DDR0B_CLK2_t	F16
DDR0A_CLK3_c	G29	DDR0B_CLK3_c	G18
DDR0A_CLK3_t	F29	DDR0B_CLK3_t	F18
DDR0A_CS[0]	B29	DDR0B_CS[0]	B18
DDR0A_CS[1]	E30	DDR0B_CS[1]	E17
DDR0A_CS[2]	C30	DDR0B_CS[2]	C17
DDR0A_CS[3]	A30	DDR0B_CS[3]	A17
DDR0A_DMI0_n	A44	DDR0B_DMI0_n	A13
DDR0A_DMI1_n	A42	DDR0B_DMI1_n	A09
DDR0A_DMI2_n	A38	DDR0B_DMI2_n	A05
DDR0A_DMI3_n	A34	DDR0B_DMI3_n	A03
DDR0A_DQ0[0]	E44	DDR0B_DQ0[0]	B14
DDR0A_DQ0[1]	B45	DDR0B_DQ0[1]	D14
DDR0A_DQ0[2]	A46	DDR0B_DQ0[2]	C13
DDR0A_DQ0[3]	C46	DDR0B_DQ0[3]	B12
DDR0A_DQ0[4]	C44	DDR0B_DQ0[4]	E13
DDR0A_DQ0[5]	D43	DDR0B_DQ0[5]	A15
DDR0A_DQ0[6]	D45	DDR0B_DQ0[6]	A11
DDR0A_DQ0[7]	E46	DDR0B_DQ0[7]	D12
DDR0A_DQ1[0]	E40	DDR0B_DQ1[0]	E09

Table 5 — DDR5 Single-Channel CAMM2 Connector Pin Wiring Assignments (cont'd)

SIGNAL NAME	PIN NUMBER
DDR0A_DQ1[1]	C42
DDR0A_DQ1[2]	D41
DDR0A_DQ1[3]	C40
DDR0A_DQ1[4]	A40
DDR0A_DQ1[5]	B41
DDR0A_DQ1[6]	B43
DDR0A_DQ1[7]	E42
DDR0A_DQ2[0]	B37
DDR0A_DQ2[1]	D39
DDR0A_DQ2[2]	C36
DDR0A_DQ2[3]	D37
DDR0A_DQ2[4]	E36
DDR0A_DQ2[5]	B39
DDR0A_DQ2[6]	E38
DDR0A_DQ2[7]	C38
DDR0A_DQ3[0]	D33
DDR0A_DQ3[1]	D35
DDR0A_DQ3[2]	A32
DDR0A_DQ3[3]	B35
DDR0A_DQ3[4]	C34
DDR0A_DQ3[5]	B33
DDR0A_DQ3[6]	A36
DDR0A_DQ3[7]	E34
DDR0A_DQS0_c	G43
DDR0A_DQS0_t	F43
DDR0A_DQS1_c	G41
DDR0A_DQS1_t	F41
DDR0A_DQS2_c	G37
DDR0A_DQS2_t	F37
DDR0A_DQS3_c	G35
DDR0A_DQS3_t	F35
DDR0A_DQS4_c	G33
DDR0A_DQS4_t	F33

SIGNAL NAME	PIN NUMBER
DDR0B_DQ1[1]	C09
DDR0B_DQ1[2]	B10
DDR0B_DQ1[3]	D10
DDR0B_DQ1[4]	D08
DDR0B_DQ1[5]	B08
DDR0B_DQ1[6]	E11
DDR0B_DQ1[7]	C11
DDR0B_DQ2[0]	D06
DDR0B_DQ2[1]	B06
DDR0B_DQ2[2]	C05
DDR0B_DQ2[3]	E07
DDR0B_DQ2[4]	C07
DDR0B_DQ2[5]	B04
DDR0B_DQ2[6]	E05
DDR0B_DQ2[7]	A07
DDR0B_DQ3[0]	D02
DDR0B_DQ3[1]	C03
DDR0B_DQ3[2]	D04
DDR0B_DQ3[3]	E01
DDR0B_DQ3[4]	B02
DDR0B_DQ3[5]	C01
DDR0B_DQ3[6]	E03
DDR0B_DQ3[7]	A01
DDR0B_DQS0_c	G12
DDR0B_DQS0_t	F12
DDR0B_DQS1_c	G10
DDR0B_DQS1_t	F10
DDR0B_DQS2_c	G06
DDR0B_DQS2_t	F06
DDR0B_DQS3_c	G04
DDR0B_DQS3_t	F04
DDR0B_DQS4_c	G14
DDR0B_DQS4_t	F14
HSA_0	F02
HSCL_0	G45
HSDA_0	F45
PWR_EN_0	G01
PWR_GOOD_0	F01
RESET0_n	G46
UNLOCK_0	G02

Table 5— DDR5 Single-Channel CAMM2 Connector Pin Wiring Assignments (cont'd)

SIGNAL NAME	PIN NUMBER
RFU	F08, F39, G08, G39
VIN_BULK	E23, E24, F23, F24, G23, G24
VSSa	B01, B46, D01, D23, D24, D46, F21, F26, G21, G26
VSSb	A02, A06, A10, A14, A18, A22, A25, A29, A33, A37, A41, A45, B05, B09, B13, B17, B21, B24, B28, B32, B36, B40, B44, C02, C06, C10, C14, C18, C22, C25, C29, C33, C37, C41, C45, D05, D09, D13, D17, D21, D28, D32, D36, D40, D44, E02, E06, E10, E14, E18, E22, E25, E29, E33, E37, E41, E45
VSSc	A04, A08, A12, A16, A20, A27, A31, A35, A39, A43, B03, B07, B11, B15, B19, B23, B26, B30, B34, B38, B42, C04, C08, C12, C16, C20, C27, C31, C35, C39, C43, D03, D07, D11, D15, D19, D26, D30, D34, D38, D42, E04, E08, E12, E16, E20, E27, E31, E35, E39, E43, F03, F05, F07, F09, F11, F13, F15, F17, F19, F28, F30, F32, F34, F36, F38, F40, F42, F44, G03, G05, G07, G09, G11, G13, G15, G17, G19, G28, G30, G32, G34, G36, G38, G40, G42, G44
NOTES: 1. VSSa are ground pins that are populated in this Variation BXXX of the CAMM2 connector. This connector standardization is underway by JEDEC JC-11. 2. VSSb and VSSc are ground pins that are populated in future variations of the CAMM2 Connector. They are intended to improve crosstalk performance of the CAMM2 connector. JEDEC JC-11 defines the ground pin population requirements based on connector performance requirements.	

3.5 DDR5 Dual-Channel CAMM2 Connector Pin Assignments

		MOUNTING		HOLE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23		
A	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
B	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
C	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
D	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
E	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
F	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
G	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
H	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
I	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
J	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
K	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
L	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
M	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
N	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR
P	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR	VSS	DOR

3.6 DDR5 Dual-Channel Pinout Table

Table 6 — DDR5 Dual-Channel CAMM2 Connector Pin Wiring Assignments

SIGNAL NAME	PIN NUMBER
ALERT0_n	N46
ALERT1_n	F46
DDR0A_CA[0]	L29
DDR0A_CA[1]	H28
DDR0A_CA[10]	H24
DDR0A_CA[11]	J25
DDR0A_CA[12]	K24
DDR0A_CA[2]	K28
DDR0A_CA[3]	M28
DDR0A_CA[4]	J27
DDR0A_CA[5]	H26
DDR0A_CA[6]	K26
DDR0A_CA[7]	L27
DDR0A_CA[8]	M26
DDR0A_CA[9]	L25
DDR0A_CB4[0]	J31
DDR0A_CB4[1]	L31
DDR0A_CB4[2]	K32
DDR0A_CB4[3]	M32
DDR0A_CLK0_c	P25
DDR0A_CLK0_t	N25
DDR0A_CLK1_c	P27
DDR0A_CLK1_t	N27
DDR0A_CLK2_c	P31
DDR0A_CLK2_t	N31
DDR0A_CLK3_c	P29
DDR0A_CLK3_t	N29
DDR0A_CS[0]	J29
DDR0A_CS[1]	M30
DDR0A_CS[2]	K30
DDR0A_CS[3]	H30
DDR0A_DMI0_n	H44
DDR0A_DMI1_n	H42
DDR0A_DMI2_n	H38
DDR0A_DMI3_n	H34
DDR0A_DQ0[0]	M44
DDR0A_DQ0[1]	J45

SIGNAL NAME	PIN NUMBER
DDR1A_CA[0]	D29
DDR1A_CA[1]	A28
DDR1A_CA[10]	A24
DDR1A_CA[11]	B25
DDR1A_CA[12]	C24
DDR1A_CA[2]	C28
DDR1A_CA[3]	E28
DDR1A_CA[4]	B27
DDR1A_CA[5]	A26
DDR1A_CA[6]	C26
DDR1A_CA[7]	D27
DDR1A_CA[8]	E26
DDR1A_CA[9]	D25
DDR1A_CB4[0]	B31
DDR1A_CB4[1]	D31
DDR1A_CB4[2]	C32
DDR1A_CB4[3]	E32
DDR1A_CLK0_c	G25
DDR1A_CLK0_t	F25
DDR1A_CLK1_c	G27
DDR1A_CLK1_t	F27
DDR1A_CLK2_c	G31
DDR1A_CLK2_t	F31
DDR1A_CLK3_c	G29
DDR1A_CLK3_t	F29
DDR1A_CS[0]	B29
DDR1A_CS[1]	E30
DDR1A_CS[2]	C30
DDR1A_CS[3]	A30
DDR1A_DMI0_n	A44
DDR1A_DMI1_n	A42
DDR1A_DMI2_n	A38
DDR1A_DMI3_n	A34
DDR1A_DQ0[0]	E44
DDR1A_DQ0[1]	B45
DDR1A_DQ0[2]	A46
DDR1A_DQ0[3]	C46