

JEDEC STANDARD

Low Power Double Data Rate Interface for Non-Volatile Memory (LPDDR4X-NVM) Standard

JESD326-4

November 2024

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Low Power Double Data Rate Interface for Non-Volatile Memory (LPDDR4X-NVM) Standard

(From JEDEC Board Ballot JCB-24-36, formulated under the cognizance of the JC-42.6 subcommittee on Low Power Memories, item number 1887.99).

1 Scope

This standard defines the Low Power Double Data Rate interface for Non-Volatile memory (LPDDR4X-NVM) standard. This standard describes features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant 16 bit single channel LPDDR4X-NVM device. LPDDR4X-NVM density ranges from 128Mb through 32Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2) LPDDR3 (JESD209-3), LPDDR4 (JESD209-4D) and LPDDR4X (JESD209-4-1A).

The LPDDR4X-NVM standard adopts substantial functionality from the LPDDR4 and LPDDR4X specifications to provide an interface to a multi-bank non-volatile memory array. When practical, LPDDR4X-NVM functionality is adopted directly from the LPDDR4/4X specifications. When necessary, existing infrastructure is modified or new infrastructure is created. This revision of the LPDDR4X-NVM specification describes a dual-port memory with a read-only LPDDR4X interface and a read-write capable Serial Peripheral Interface (SPI). Additional functionality includes an interrupt output signal (INT_n) and a device reset input signal (DEVRST_n).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated into the JEDEC Board Ballot JCB-24-36 to prepare the LPDDR4X-NVM standard.

2 Die Configuration, Pad Order, Package Ballout, and Pin Definition

2.1 Die Configuration

The LPDDR4X-NVM specification supports a single channel x16 die configuration.

Figure 1 shows the signals used for the single channel x16 configuration.

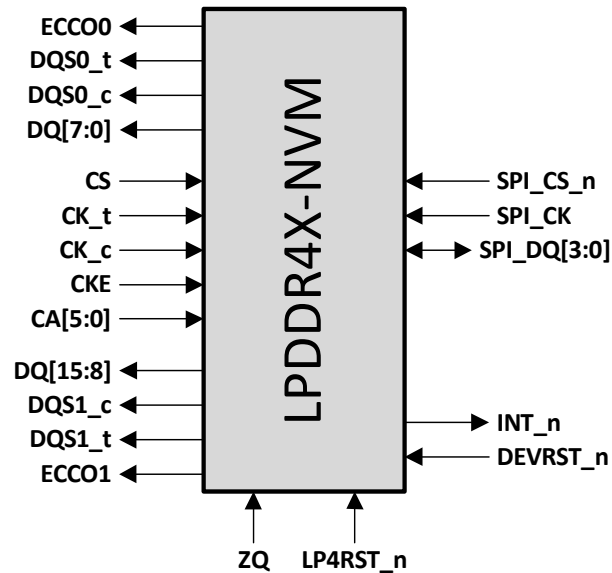


Figure 1 — Single Channel x16 Die

Figure 2 and Figure 3 show simplified block diagrams of the LPDDR4X-NVM device. The standard device is available with the legacy 8-bank LPDDR4 architecture. An optional 8-bank configuration where each bank is partitioned into two sub-banks is also available. The sub-bank architecture allows for READ pipelining between sub-banks within a single bank. The optional architecture uses an upper order row address to specify the target sub-bank. Note that the sub-banks are not specified with a bank address bit but are identified with the highest order (non-bank) row address.

2.1 Die Configuration (cont'd)

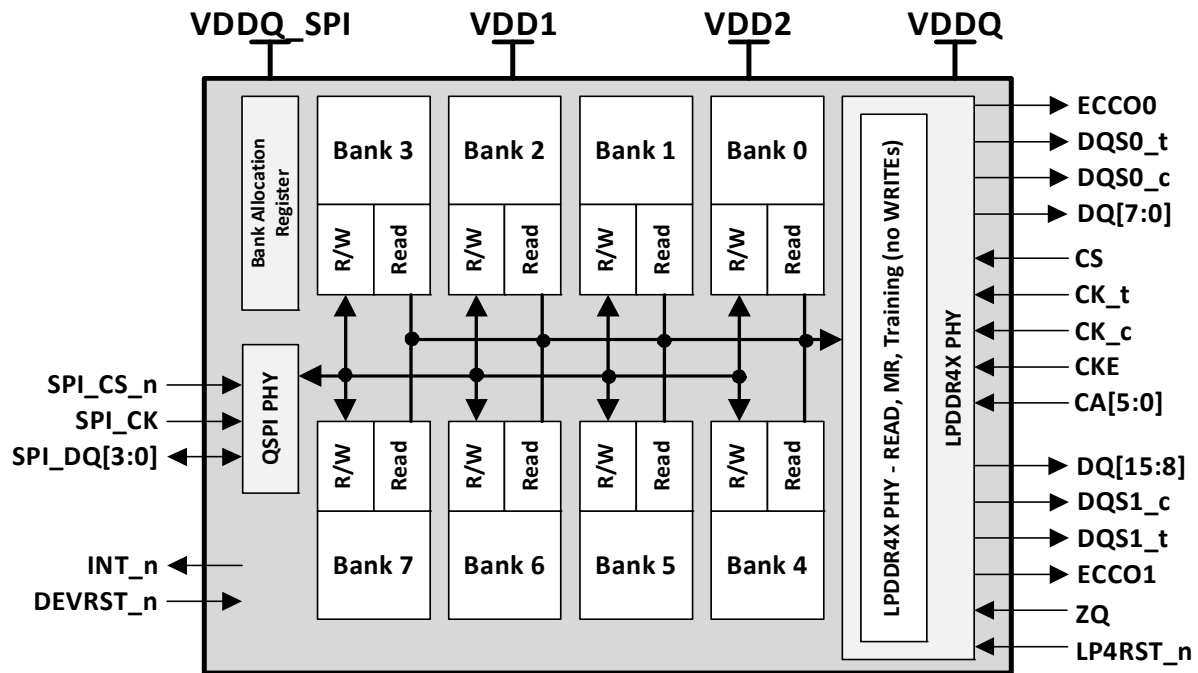


Figure 2 — LPDDR4X-NVM Block Diagram, Standard 8-bank Architecture

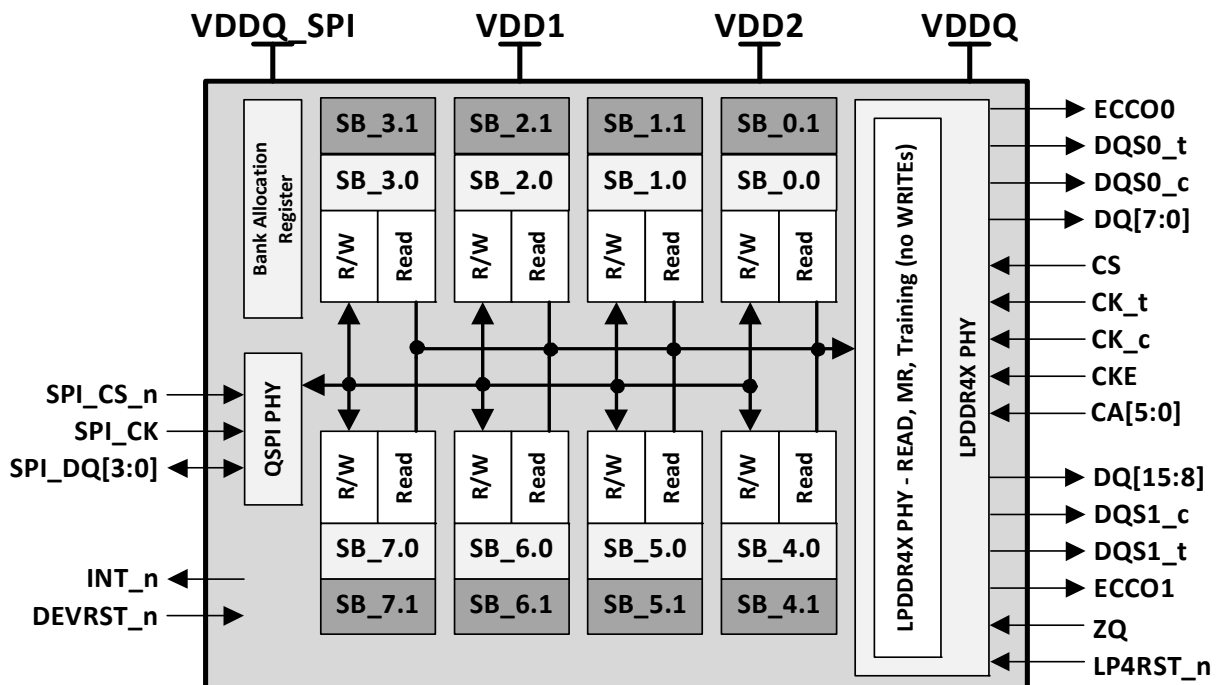
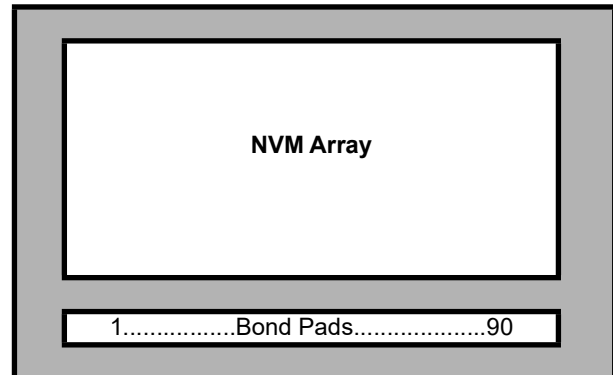


Figure 3 — LPDDR4X-NVM Block Diagram, Optional SubBank (SB) Architecture

2.2 Pad Order

Bottom Left	
1	DIE_NUM
2	DEVRST_n
3	INT_n
4	SPI_DQ3
5	VDDQ_SPI
6	VSS
7	SPI_DQ2
8	SPI_CK
9	SPI_CS_n
10	SPI_DQ1
11	VDDQ_SPI
12	VSS
13	SPI_DQ0
14	VDD2
15	VSS
16	VDD1
17	VDD2
18	VSS
19	VSSQ
20	DQ8
21	VDDQ
22	DQ9
23	VSSQ
24	DQ10
25	VDDQ
26	DQ11
27	VSSQ
28	DQS1_t
29	DQS1_c
30	VDDQ
31	ECCO1
32	VSSQ
33	DQ12
34	VDDQ
35	DQ13
36	VSSQ
37	DQ14
38	VDDQ
39	DQ15
40	VSSQ
41	ZQ
42	VDDQ
43	VDD2
44	LP4RST_n
45	VDD1

46	VSS
47	CA5
48	CA4
49	VDD2
50	CA3
51	CA2
52	VSS
53	CK_c
54	CK_t
55	VDD2
56	CKE
57	CS
58	VSS
59	CA1
60	CA0
61	VDD2
62	VSS
63	VDD1
64	VSSQ
65	DQ7
66	VDDQ
67	DQ6
68	VSSQ
69	DQ5
70	VDDQ
71	DQ4
72	VSSQ
73	ECCO0
74	VDDQ
75	DQS0_c
76	DQS0_t
77	VSSQ
78	DQ3
79	VDDQ
80	DQ2
81	VSSQ
82	DQ1
83	VDDQ
84	DQ0
85	VSSQ
86	VSS
87	VDD2
88	VDD1
89	VSS
90	VDD2
Bottom Right	



NOTE 1 Applications are strongly advised to follow bit/byte assignments. Bit or Byte swapping at the application level requires extensive review of SPI/LPDDR4X bit/byte mapping, MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for memory mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.

2.3 Package Ballout

2.3.1 123 ball 1CHx16 Discrete Package, 0.80 mm x 0.80 mm using MO-216

0.80 mm pitch (X-axis), 0.80 mm pitch (Y-axis), 12 rows.

0.80 mm Pitch												
	1	2	3	4	5	6	7	8	9	10	11	12
A		DNU				NC	NC				DNU	DNU
B	DNU	RFU	VSS	VDD2	ZQ0	NC	NC	ZQ1	VDD2	VSS	RFU	DNU
C	RFU	DQ0	VDDQ	DQ7	VDDQ	NC	NC	VDDQ	DQ15	VDDQ	DQ8	RFU
D	VSS	DQ1	ECCO0	DQ6	VSS	NC	NC	VSS	DQ14	ECCO1	DQ9	VSS
E	VDDQ	VSS	DQS0_t	VSS	VDDQ			VDDQ	VSS	DQS1_t	VSS	VDDQ
F	VSS	DQ2	DQS0_c	DQ5	VSS			VSS	DQ13	DQS1_c	DQ10	VSS
G	VDD1	DQ3	VDDQ	DQ4	VDD2			VDD2	DQ12	VDDQ	DQ11	VDD1
H	VSS	DNU	VSS	VDDQ_S PI	VSS			VSS	VDDQ_S PI	VSS	LP4RST _n	VSS
J	VDD2	CA0	CS1	CS0	VDD2	SPI_DQ0	VSS	VDD2	CA2	CA3	CA4	VDD2
K	VSS	CA1	VSS	CKE0	CKE1	SPI_DQ1	INT_n	CK_t	CK_c	VSS	CA5	VSS
L	VDD2	VSS	VDD2	VSS	SPI_CS_n	SPI_CK	SPI_DQ3	DEVIRST_n	VSS	VDD2	VSS	VDD2
M	DNU	DNU				SPI_DQ2	VSS				DNU	DNU

NOTE 3 Top View, A1 in top left corner.

NOTE 4 Die pad VSS and VSSQ signals are combined to VSS package balls.

2.4 Pin Definition and Description

Table 1 — Pin Definition and Description

Symbol	Type	Description
CK _t , CK _c	Input	Clock: CK _t and CK _c are differential clock inputs for the LPDDR4X interface. All address, command, and control input signals are sampled on the crossing of the positive edge of CK _t and the negative edge of CK _c . AC timings for CA parameters are referenced to CK.
CKE[1:0]	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. CKE[1] connects to the Rank 1 die in a two die package. CKE[0] connects to the Rank 0 die in a two die package and is used as CKE in a single die package.
CS[1:0]	Input	Chip Select: CS is part of the command code. CS[1] is used to indicate Rank 1 in a two die package. CS[0] is used to indicate Rank 0 in a two die package and is used as CS in a single die package.
CA[5:0]	Input	Command/Address Inputs: CA signals provide the Command and Address inputs according to the Command Truth Table.
DQ[15:0]	I/O	Data Input/Output: Bi-direction data bus. Outputs during READ transactions, inputs during CA bus training.
DQS[1:0] _t , DQS[1:0] _c	Output	Data Strobe: DQS _t and DQS _c are differential output clock signals used to strobe data during a READ. The Data Strobe is generated by the memory for a READ and is edge-aligned with Data.
ECCO[1:0]	Output	Error Correction Code Output: The ECC Outputs (per byte lane) can be configured for the following using Mode Register settings: 1. ECC Outputs disabled during read transactions 2. The ECCO signals are used during Read transactions to output ECC information.
ZQ[1,0]	Reference	Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ± 1% resistor. ZQ[1] connects to the Rank 1 die in a two die package. ZQ[0] connects to the Rank 0 die in a two die package and is used as ZQ in a single die package.
VDDQ, VDD1, VDD2, VDDQ_SPI	Supply	Power Supplies: Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	Ground Reference: Power supply ground reference
LP4RST _n	Input	LP4RST_n: When asserted LOW, the LP4RST _n signal resets the LPDDR4X interface. LP4RST _n does not include a weak pull-up.
DEVRST _n	Input	DEVRST_n: The DEVRST _n pin is used to re-initiate the Power-On Reset (POR) process. All volatile registers will be returned to their default state during the reset process. DEVRST _n includes a weak pull-up.
INT _n	Output	INT_n: Open drain output indicates to the host system that an internal event has occurred. INT _n includes a weak (internal) pull-up. The recommended (external) pull-up resistor for the INT _n output is 5K to 10K ohms.
SPI_CS _n	Input	SPI_CS_n: Low enabled chip select for the SPI interface.
SPI_CK _n	Input	SPI_CK_n: The clock signal for the SPI interface.
SPI_DQ[3:0]	I/O	SPI_DQ[3:0]: The SPI data bus supports both the x1 SPI (default) and x4 (QSPI) interfaces.
DIE_NUM	Input	DIE_NUM: This input is compared to an upper-order address bit during SPI transactions when two die are assembled in a single package. On the SPI interface, the Rank 0 device is indicated when the DIE_NUM input is bonded to VSS and the Rank 1 device when DIE_NUM is bonded to VDDQ_SPI.

NOTE 1 Consult manufacturer data sheet for manufacturer specific behavior of stacked die devices.

2.5 ZQ Wiring

Standard LPDDR4X-NVM package ballmaps allocate one ZQ ball per die.

(See Section 4.19.2, 'ZQ External Resistor, Tolerance, and Capacitive Loading' for more information.)

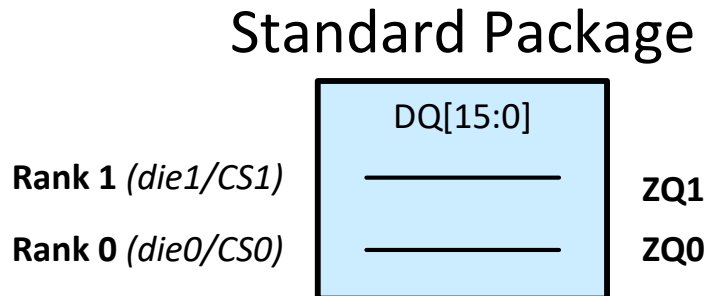


Figure 4 — ZQ Wiring Overview

Below are specific wiring notes for multi-die LPDDR4X-NVM packages.

1. For multi-die packages:
 - ZQ0 is connected to the rank 0 LPDDR4X-NVM device
 - ZQ1 is connected to the rank 1 LPDDR4X-NVM device (if present)

3 Functional Description

LPDDR4X-NVM is a high-speed synchronous nonvolatile memory device. The device is comprised of 8-banks with device densities ranging from 128 Mb to 32 Gb. The devices implement a two-port architecture that includes a Quad IO Serial Peripheral Interface (QSPI) port and a single channel x16 LPDDR4X interface. The LPDDR4X port is read-only and the SPI port supports both read and write operations.

The Serial Peripheral Interface (SPI) port on the LPDDR4X-NVM device performs a number of functions intended to enhance device performance and allow for ease of adoption.

1. Offload the LPDDR4X-NVM interface from performing WRITE operations. Performing Program and Erase operations can occur over the SPI port without diminishing any of the READ bandwidth on the LPDDR interface.
2. Transferring WRITE operations away from the LPDDR interface eliminates the need for time-consuming write training. Eliminating write training shortens the time required until the LPDDR interface is ready for operation.
3. The SPI port allows booting from a legacy boot path. A Quad-SPI boot option is available on many SoC devices.

A 4-bit Quad-SPI (QSPI) port was chosen because of its universal adoption by SoC devices targeting the automotive ecosystem. Performance of the SPI port is a secondary concern because the expectation is that only a small amount of code/data will be accessed during the boot process before high-speed read access is available over the LPDDR interface. A secondary reason for using QSPI is that the interface is well understood and its definition (within this JEDEC specification) can be made unambiguous.

Single-channel LPDDR4X-NVM devices contain the following number of bits:

128 Mb	has 134,217,728 bits
256 Mb	has 268,435,456 bits
512 Mb	has 536,870,912 bits
1 Gb	has 1,073,741,824 bits
2 Gb	has 2,147,483,648 bits
4 Gb	has 4,294,967,296 bits
8 Gb	has 8,589,934,592 bits
16 Gb	has 17,179,869,184 bits
32 Gb	has 34,359,738,368 bits

LPDDR4X-NVM devices use a 2 or 4 clock architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycles, during which command information is transferred on the positive edge of the clock. See command truth table for details.

The LPDDR4X interface uses a double data rate architecture on the DQ pins to achieve high speed operation. A read access on the LPDDR4X interface consists of a single 256 (or 512) bit wide, data transfer from the internal NVM array using 16 (or 32) corresponding 16-bit wide, one half-clock-cycle data transfers at the I/O pins, referred to as the Burst Length (BL). Read accesses from the LPDDR4X-NVM device are burst oriented; accesses start at a selected location and continue for 16 (BL16) or 32 (BL32) address locations in a programmed sequence.

The LPDDR4X-NVM specification describes four different READ sequences:

1. The Legacy READ sequence is available on devices using a high-speed NVM technology and is compatible with the JEDEC LPDDR4X standard. The Legacy READ is described in Section 4.1.1.
2. The Non-Volatile READ sequence minimizes the CA bus footprint for shorter latency NVM technologies. The NVR READ is described in Section 4.1.2.

3 Functional Description (cont'd)

3. The Modified READ sequence is available on devices using a longer latency NVM technology and requires that the host controller comprehend the increased number of row addresses and the smaller row size. The Modified READ is described in Section 4.1.3.
4. The Modified READ with the optional PRE-ACTIVATE command. The PRE-ACTIVATE command is used to support higher densities when using the Modified READ command. The Modified READ using PRE-ACTIVATE is described in section 4.1.4

Manufacturers are expected to support only one of the READ transactions on a device.

Prior to normal operation, the LPDDR4X-NVM device must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

3.1 LPDDR4X-NVM Addressing

Table 2 — LPDDR4X-NVM Addressing x

	Legacy JEDEC READ		Modified JEDEC READ		Non-Volatile READ (NVR)	
	BL16	BL32	BL16	BL32	BL16	BL32
Max Device Density	32Gb	32Gb	1Gb	2Gb	2Gb	4Gb
Max Using Pre-Activate	n.a.		32Gb	32Gb	n.a.	
Configuration	1x 16DQ x 8-bank (single channel)					
Channels (per die)	1					
Number of Banks	8					
Array Pre-Fetch (bits)	256	512	256	512	256	512
Row Size (Bytes)	32	64	32	64	32	64
Number of Rows (1Gb density example)	4,194,304	2,097,152	4,194,304	2,097,152	4,194,304	2,097,152
Bank Address	BA0 - BA2		BA0 - BA2		na	
Row Addresses (wo PRE)	R0 - R23	R0 - R22	R0 - R18	R0 - R18	R0 - R22	R0 - R22
Row Addresses (with PRE)	na		R0 - R23	R0 - R23	na	
Column Addresses	C2 - C3	C2 - C4	C2 - C3	C2 - C4	na	
Burst Starting Address Boundary	64 - bit		64 - bit		256 - bit	512 - bit
NOTE 1	During RD/CAS2 transactions, the lower two column addresses (A0 - A1) are assumed to be “zero” and are not transmitted on the CA bus.					
NOTE 2	For device densities not requiring upper order ROW bits, the respective values in the command cycles must be driven to a valid 1 or 0 level					
NOTE 3	During NVR1/2 transactions, the lower “column” addresses are assumed to be “zero” and are not transmitted on the CA bus.					

3.2 Simplified LPDDR4X-NVM State Diagrams

The LPDDR4X-NVM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specifications.

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For command definitions, see Section 4, Command Definitions and Timing Diagrams.

3.2.1 Bank Allocation Register

The LPDDR4X-NVM device is a dual port memory with banks allocated to either the LPDDR4X port or the SPI port. The 8-banks are allocated according the their respective bits in the Bank Allocation Register (BAR). If a bit in the BAR is 1, the corresponding bank is allocated to the LPDDR4X port. If a bit in the BAR is a 0, the corresponding bank is allocated to the SPI port.

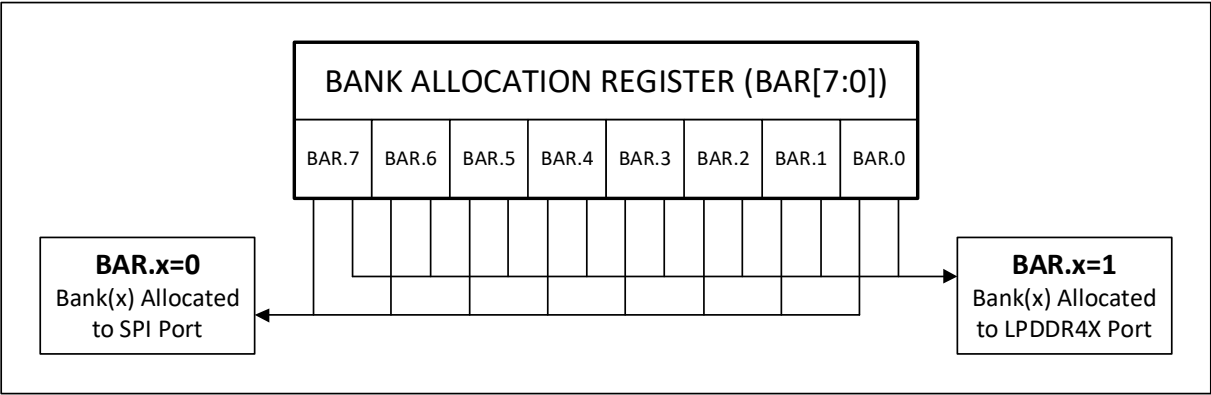


Figure 5 — Bank Allocation Register

3.2.2 LPDDR4X Port State Diagram

The State Diagram for the LPDDR4X Port is described in Figure 6. The diagram narrowly describes the state diagram for the LPDDR4X Port. Only banks that are allocated to the LPDDR4X Port are included in this description. The SPI Port and the banks allocated to the SPI Port are not described in a State Diagram. Note that the LPDDR4X-NVM device introduces an optionally supported READ transaction that use the Non-Volatile Read (NVR) command. The NVR based read lowers the command bus overhead to initiate a read transaction to four clock cycles (NVR1-NVR2) instead of the (Legacy and Modified) JEDEC READ that requires eight clocks (ACT1-ACT2-RD1-CAS2) or the Modified JEDEC READ using PREACTIVATE that uses ten clocks (PRE-ACT1-ACT2-RD1-CAS2).

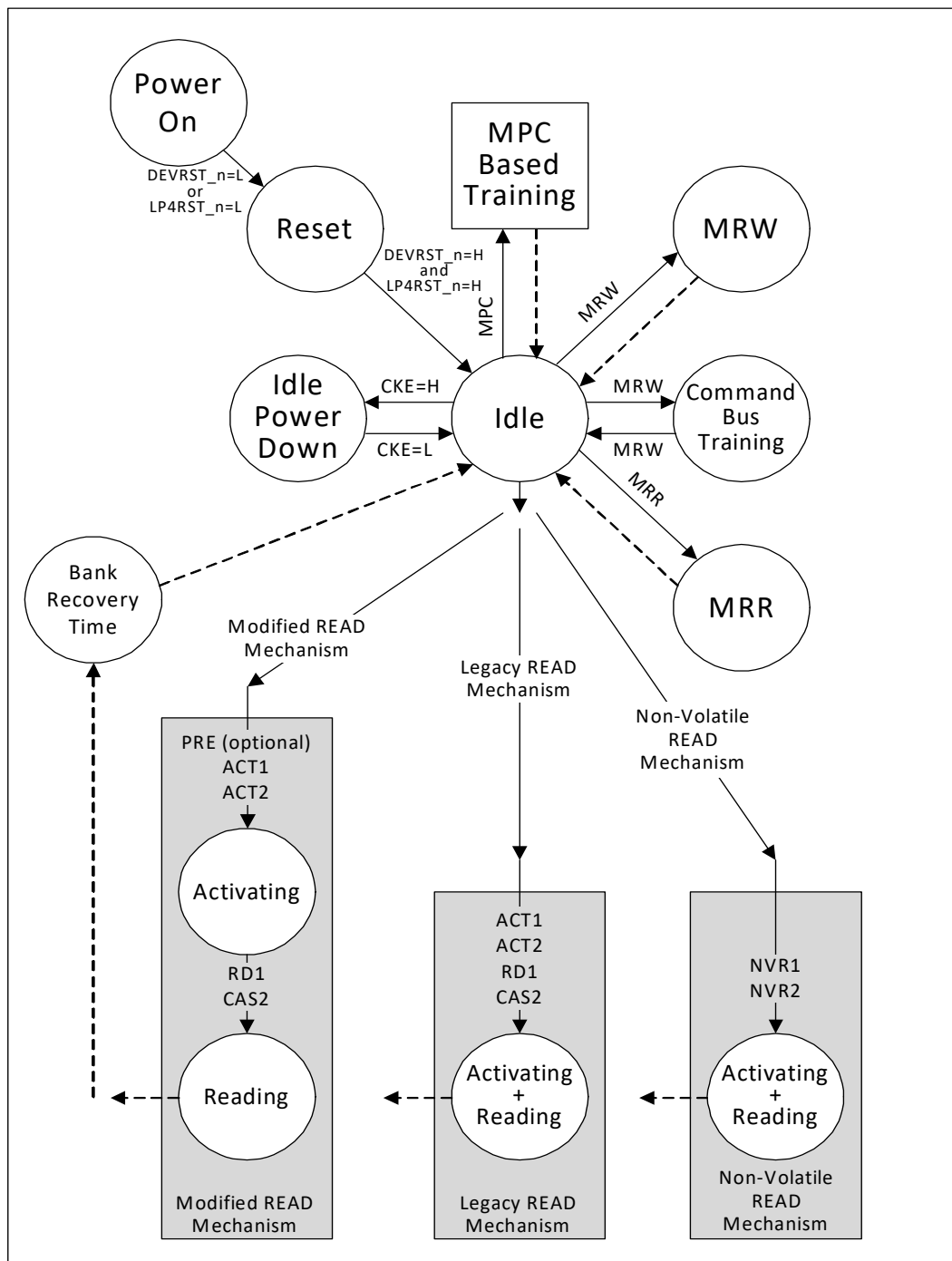
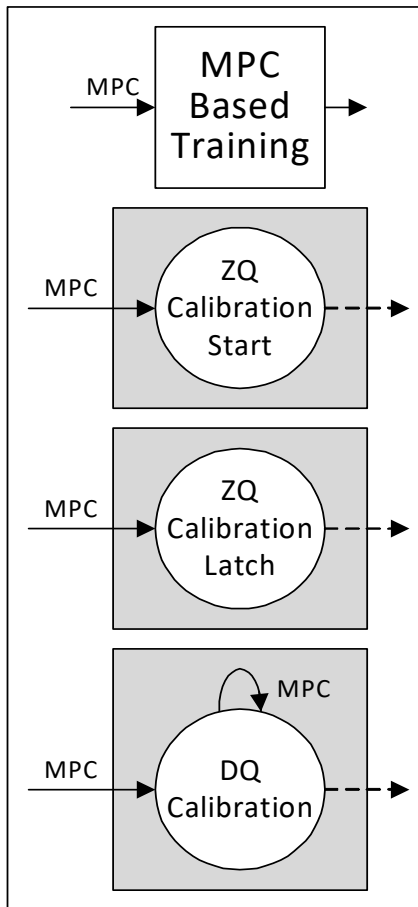


Figure 6 — LPDDR4X-NVM Interface State Diagram

3.2.3 Multi-Purpose Command (MPC) Based Training State Diagram

The LPDDR4X-NVM interface is simpler to train than its LPDDR4X-DRAM counterpart due to its read-only nature. MPC based training is only needed for ZQ calibration and DQ (READ) calibration.



- NOTE 1 In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training.
See Section 4.10 for more information.
- NOTE 2 In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training.
See Section 4.17 for more information.
- NOTE 3 This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
- NOTE 4 The LP4RST_n pin can be asserted from any state, and will cause the LPDDR4X interface to go to the Reset State. Similarly, the DEVRST_n can be asserted from any state, and will cause the entire device to go to the reset state. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on either RESET input.

Figure 7 — LPDDR4X-NVM Interface Training State Diagram

3.3 Power-up, Initialization, and Power-off Procedure

For power-up and reset initialization, in order to allow the LPDDR4X-NVM device to function properly, default values of the following MR settings are defined as shown in Table 3.

Table 3 — MRS Default Settings

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00 _B	FSP-OP/WR[0] is enabled
RL	MR2 OP[2:0]	000 _B	RL = 6
ECCO	MR3 OP[7:6]	00 _B	Read ECC Output is disabled
CA ODT	MR11 OP[6:4]	000 _B	CA ODT is disabled
V _{REFCA} Setting	MR12 OP[6]	1 _B	V _{REFCA} Range[1] enabled
V _{REFCA} Value	MR12 OP[5:0]	011101 _B	Range1: 50.3% of V _{DDQ}

3.3.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4X-NVM device. Unless specified otherwise, these steps are mandatory.

1. While applying power (after Ta), DEVRST_n is recommended to be LOW ($\leq 0.2 \times V_{DD1}$) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while DEVRST_n is held LOW. Power supply voltage ramp requirements are provided in Table 4. V_{DD1} must ramp at the same time or earlier than V_{DDQ_SPI}. V_{DDQ_SPI} must ramp at the same time or earlier than V_{DD2}. and VDD2 must ramp at the same time or earlier than VDDQ.

Table 4 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	V _{DD1} must be greater than V _{DDQ_SPI}
	V _{DDQ_SPI} must be greater than V _{DD2}
	V _{DD2} must be greater than V _{DDQ} - 200 mV
NOTE 1 Ta is the point when any power supply first reaches 300 mV. NOTE 2 Voltage ramp conditions in Table 2 apply between Ta and power-off (controlled or uncontrolled). NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges. NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20 ms. NOTE 5 The voltage difference between any V _{SS} and V _{SSQ} pins must not exceed 100 mV.	

2. Following the completion of the voltage ramp (Tb), DEVRST_n must be maintained LOW. DQ, ECCO, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. CE, CK_t, CK_c, CS_n and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.
3. Beginning at Tb, DEVRST_n must remain LOW for at least tINIT1(Tc), after which DEVRST_n can be deasserted to HIGH(Tc). LP4RST_n must be held LOW from Tb to the end of tINIT2. All other input signals are "Don't Care."

3.3.1 Voltage Ramp and Device Initialization (cont'd)

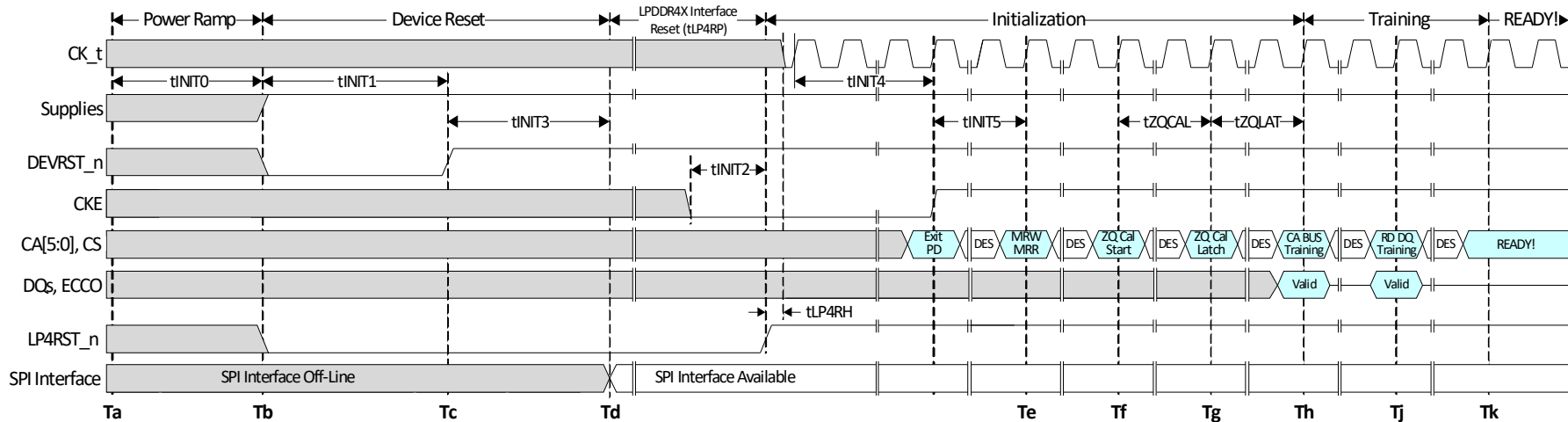


Figure 8 — Power Ramp and Initialization Sequence

4. After DEVRST_n is de-asserted (Tc), wait for at least tINIT3 (Td) before the LPDDR4X-NVM interface reset (LP4RST_n) process initiates. LP4RST_n must remain LOW for at least tLP4RP from Td, after which LP4RST_n can be deasserted to HIGH. At least tINIT2 before LP4RST_n deassertion, CKE is required to be set LOW. Clock (CK_t, CK_c) is required to be started and stabilized for tINIT4 before CKE goes active. CS is required to be maintained at LOW when the controller activates CKE. The SPI interface also becomes available at Td and the host also starts communicating with the SPI port by asserting SPI_CS LOW.
5. After setting CKE high, wait minimum of tINIT5 to issue any Mode Register Read (MRR) or Mode Register Write (MRW) commands (Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.
6. After completing all MRW commands to set the Pull-up, Pull-down and input termination values, the LPDDR-NVR host controller can issue ZQCAL Start command to the memory (Tf). This command is used to calibrate the VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4X-NVM device share one external ZQ resistor, the controller must not overlap the (independent) ZQ calibration sequence of each LPDDR4X-NVM device. The ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and CA ODT to the calibrated values.

3.3.1 Voltage Ramp and Device Initialization (cont'd)

7. After t_{ZQLAT} is satisfied (T_h), the command bus (internal V_{REFCA} , CS, and CA) should be trained for high-speed operation by issuing a MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal V_{REFCA} and align CS/CA with CK for high-speed operation. The LPDDR4X-NVM device will power-up with receivers configured for low-speed operations, and V_{REFCA} set to a default factory setting. Normal device operation at clock speeds higher than t_{CKb} may not be possible until command bus training has been completed.

NOTE The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See Section 4.13 for information on how to enter/exit the Command Bus training mode.

8. After Command Bus Training (CBT) has completed, the Multi-Purpose Command (MPC) Read Calibration command is used (repeatedly at T_j) by the host MCU to calibrate its own V_{refDQ} and also its READ data capture timing.
9. At T_k the LPDDR4X-NVM device is ready for normal operation, and is ready to accept any valid command. Any mode registers that have not previously been set up for normal operation should be written at this time.

Table 5 — Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
t_{INIT0}	-	20	ms	Maximum voltage-ramp time
t_{INIT1}	1	-	μs	Minimum DEV_{RST_n} LOW time after completion of voltage ramp
t_{INIT2}	10	-	ns	Minimum CKE low time before DEV_{RST_n} high
t_{INIT3}	400	-	μs	Time to SPI bus available after DEV_{RST_n} high after power-up
t_{INIT4}	5	-	tCK	Minimum stable clock before first CKE high
t_{INIT5}	2	-	μs	Minimum idle time before first MRW/MRR command
t_{ZQCAL}	1	-	μs	ZQ calibration time
t_{ZQLAT}	Max(30ns, 8tCK)	-	ns	ZQCAL latch quiet time.
t_{CKb}	Note ^{*1,2}	Note ^{*1,2}	ns	Clock cycle time during boot
$t_{ZQRESET}$	Max(50ns, 3tCK)	-	ns	ZQ Calibration Reset Time
t_{LP4RH}	20	-	ns	Reset Hold - $LP4RST_n$ deasserted before CK recognized
t_{LP4RP}	100	-	ns	Interface Reset Pulse Width ($LP4RST_n$)

NOTE 1 Min t_{CKb} guaranteed by LPDDR4X-NVM test is 18 ns.

NOTE 2 The system may boot at a higher frequency than dictated by min t_{CKb} . The higher boot frequency is system dependent.

3.3.2 Device Reset with Stable Power (DEVRST_n)

The following sequence is required for Device Reset after the power reaches a stable state.

1. Assert DEVRST_n below $0.2 \times V_{DDQ_SPI}$ anytime when device reset is needed. DEVRST_n needs to be maintained for minimum tPW_RST. CKE must be pulled LOW at least 10 ns before de-asserting DEVRST_n.
 - All device registers (LPDDR4X and SPI) are loaded with their default values.
 - All embedded operations (erase, program, ...) are terminated
2. Wait for the Stable Power Reset time (tSPR) to expire
3. Perform the LPDDR4X bus initialization sequence starting from the beginning of tINIT4 (See “Power Ramp and Initialization Sequence” on page 14.).

Table 6 — Stable Power Reset Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tPW_RST	200	-	ns	Minimum DEVRST_n low Time for Reset Initialization with stable power
tCKE_DEVRST	10	-	ns	CKE LOW before DEVRST_n high
tSPR	TBD	-	us	Stable Power Reset recovery time for the SPI and LPDDR4X buses after DEVRST_n high

NOTE 1 TBD = To Be Determined (in next specification revision)

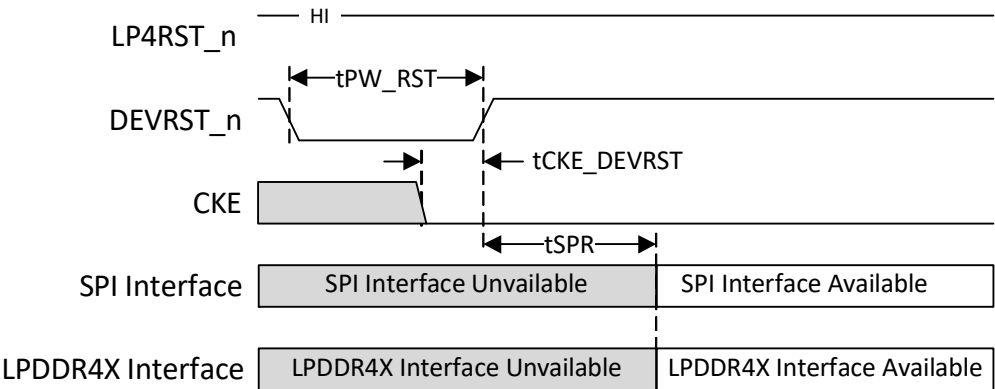


Figure 9 — Stable-Power Device Reset Timing

3.3.3 LPDDR4X Interface Reset with Stable Power (LP4RST_n)

A dedicated LPDDR4X input signal (LP4RST_n) is used to return the LPDDR4X interface to the default state. While the LP4RST_n signal is asserted (LOW), all LPDDR4X inputs are ignored and outputs are placed into the High-Z state. LP4RST_n must remain LOW for at least tLP4RP, after which LP4RST_n can be deasserted to HIGH. At least tINIT2 before LP4RST_n deassertion, CKE is required to be set LOW. All other LPDDR4X input signals are “Don’t Care.” After LP4RST_n is deasserted, wait at least tCKCKEH before activating CKE and after setting CKE HIGH, wait a minimum of tXP to issue commands on the LPDDR4X interface.

Upon completion of an LPDDR4X interface reset, the default values are loaded into the LPDDR4X Mode Registers . The LPDDR4X interface will be ready for new operations after tLP4RH has elapsed.

Note that the LPDDR4X Interface Reset only impacts the LPDDR4X interface, activity in the rest of the device is not interrupted. The LP4RST_n input is ignored during PoR.

3.3.3 LPDDR4X Interface Reset with Stable Power (LP4RST_n) (cont'd)

Table 7 — Mode Registers Set to Defaults After LPDDR4X Interface Reset

Mode Register #	Register Name	Comments
MR1	Bus Configuration 1	Burst Length, Read Preamble, Read Postamble
MR2	Bus Configuration 2	Read Latency
MR3	IO Configuration	Pull-up Cal Point, Pull-down Drive Strength, ECC over ECCO
MR11	ODT Control	CA ODT Strength
MR12	VrefCA Control	VrefCA Setting, VrefCA Range
MR13	Register Control	Frequency Set Point (FSP) Read/Write, Frequency Set Point Operation Mode
MR22	ODT Configuration	CK ODT Enable, CS ODT Enable, CA ODT Enable

Table 8 — LPDDR4X Interface Reset Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT2	10	-	ns	Minimum CKE low time before LPRST_n high
tCKCKEH	max(1.75ns, 3nCK)	-	ns	CK valid before CKE high
tXP	max(7.5ns, 5nCK)	-	ns	Exit Power Down to next valid command
tLP4RP	100	-	ns	Interface Reset Pulse Width (LP4RST_n)
tLP4RH	20	-	ns	LP4RST_n deasserted before CK recognized

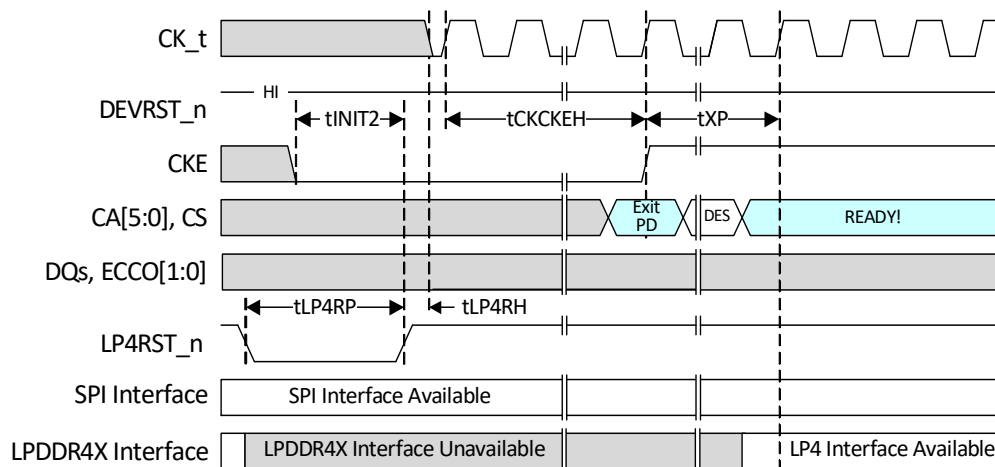


Figure 10 — LPDDR4X Interface Reset Timing

3.3.4 Power-Off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW ($\leq 0.2 \times V_{DD2}$) and all other inputs must be between V_{IL_CKEmin} and V_{IH_CKEmax} . The device outputs remain at High-Z while CKE is held LOW. DQ, ECCO, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. DEVRST_n, CK_t, CK_c, CS and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

Table 9 — Power Supply Conditions

After	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DDQ_SPI}
	V_{DDQ_SPI} must be greater than V_{DD2}
	V_{DD2} must be greater than $V_{DDQ} - 200 \text{ mV}$
NOTE 1 Tx is the point where any power supply drops below the minimum value specified. NOTE 2 Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off. NOTE 3 The voltage difference between any of V_{SS} , V_{SSQ} pins must not exceed 100 mV. NOTE 4 V_{DD1} must be higher than V_{DD2} during Power-Off.	

3.3.5 Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300 mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than $0.5 \text{ V}/\mu\text{s}$ between Tx and Tz.

The maximum Power-Off ramp time is tPOFF.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 10 — Timing Parameters Power Off

Symbol	Value		Unit	Comment
	Min	Max		
tPOFF	-	2	s	Maximum Power-Off ramp time

3.4 Mode Register Definition

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM

Table 11 shows the mode registers for LPDDR4X-NVM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Table 11 — Mode Register Assignment in LPDDR4X-NVM

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	CATR	SCLS	SE mode	RZQI		RFM Support	Latency Mode	Refresh mode
1	RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	
2	WR Lev	WLS	WL			RL		
3	DBI-WR	ECCO-RD	PDDS			PPRP	WR-PST	PU-CAL
4	Temperature Sensor Data							
5	LPDDR4X-NVM Manufacturer ID							
6	Revision ID-1							
7	Revision ID-2							
8	IO Width		Density				Type	
9	Manufacturer Specific Test Register							
10	RFU							ZQ-Reset
11	Reserved	CA ODT			Reserved	DQ ODT		
12	CBT Mode for Byte Mode	VR-CA	V _{REF} CA					
13	FSP-OP	FSP-WR	DMD	RRQ	VRCG	VRO	RPT	CBT
14	RFU	VR(dq)	V _{REF} (DQ)					
15	Lower-Byte Invert Register for DQ Calibration							
16	PASR Bank Mask							
17	PASR Segment Mask							
18	DQS Oscillator Count – LSB							
19	DQS Oscillator Count – MSB							
20	Upper-Byte Invert Register for DQ Calibration							
21	RFU							
22	ODTD for x8 2ch(Byte) mode	ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT			
23	DQS interval timer run time setting							
24	RAAMMT		RAAIMT					RFM
25	PPR Resource							
26	RFU						SCL	
27	RFU							
28	RFU							
29	RFU							
30	Reserved for testing – SDRAM will ignore							
31	Bytemode Vref Selection		RFU					
32	DQ Calibration Pattern “A” (default = 5AH)							
33	RFU							
34	RFU							
35	RFU							
36	RFU							RAADEG
37	RFU							
38	RFU							
39	Reserved for testing – SDRAM will ignore							
40	DQ Calibration Pattern “B” (default = 3CH)							
41-63	RFU							

NOTE 1 The grayed out address/field entries are RESERVED FOR FUTURE USE (RFU) for the LPDDR4X-NVM device but may have been used (or RFU) in LPDDR4 DRAM devices.

NOTE 2 The register fields shown in light green are set up as Frequency Set Point (FSP) register pairs for use during bus training (see Section 4.14).

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (continued)

Table 12 — MR0 Register Information (MA[5:0] = 00_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CATR	RFU		RZQI		RFU		

Table 13 — MR0 Register Functions

Function	Register Type	Operand	Data	Notes
RZQI (Built-in Self-Test for RZQ)	Read Only	OP[4:3]	00 _B : RZQ Self-Test Not Supported 01 _B : ZQ pin may connect to V _{SSQ} or float 10 _B : ZQ-pin may short to V _{DDQ} 11 _B : ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to V _{SSQ} or float, nor short to V _{DDQ})	1,2,3,4
CATR (CA Terminating Rank)		OP[7]	0 _B : CA for this rank is not terminated 1 _B : Manufacturer specific	5

NOTE 1 RZQI MR value, if supported, will be valid after the following sequence:

- MPC ZQCal Start followed by tZQCAL followed by MPC ZQCal Latch followed by tZQLAT.
- RZQI value will be lost after Reset.

NOTE 2 If the ZQ-pin is connected to V_{SSQ} to set default calibration, OP[4:3] shall be set to 01_B. If the ZQ-pin is not connected to V_{SSQ}, either OP[4:3] = 01_B or OP[4:3] = 10_B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 3 In the case of possible assembly error, the LPDDR4X-NVM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.

NOTE 4 If ZQ Self-Test returns OP[4:3] = 11_B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ± 1%).

NOTE 5 CATR functionality is Manufacturer specific. CATR can either indicate the connection status of the ODTCA pad for the die or whether CA for the rank is terminated. Consult the manufacturer device datasheet for details.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 14 — MR1 Register Information (MA[5:0] = 01_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RPST		RFU		RD-PRE	RFU		Burst Length

Table 15 — MR1 Register Functions

Function	Register Type	Operand	Data	Notes
Burst Length	Write Only	OP[1:0]	00 _B : BL=16 Sequential (default) 01 _B : BL=32 Sequential Others: Reserved	1
RD-PRE (RD Preamble Type)		OP[3]	0 _B : RD Preamble = Static (default) 1 _B : RD Preamble = Toggle	2,4,5
RPST (RD Postamble Length)		OP[7]	0 _B : RD Postamble = 0.5*tCK (default) 1 _B : RD Postamble = 1.5*tCK	3,4,5
NOTE 1 On-The-Fly Burst Length functionality is not supported.				
NOTE 2 For Read operations this bit must be set to select between a "toggling" preamble and a "Non-toggling" Preamble. See 4.3, Read Preamble and Postamble, for a drawing of each type of preamble.				
NOTE 3 OP[7] provides an optional READ postamble with an additional rising and falling edge of DQS _t . The optional postamble cycle is provided for the benefit of certain memory controllers.				
NOTE 4 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be read from with an MRR command to this MR address.				
NOTE 5 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.				

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 16 — Burst Sequence for LEGACYJEDEC READ and MODIFIED JEDEC READ (ACT1-ACT2-RD-CAS2)

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
		V	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
		V	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
		V	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
		1	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	0	1	0	0	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1	1	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	1	0	0	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
NOTE 1 C0-C1 are assumed to be '0', and are not transmitted on the command bus.																																						
NOTE 2 The starting burst address is on 64-bit boundaries.																																						

Table 17 — Burst Sequence for Non-Volatile READ (NVR1-NVR2)

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	NA	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

NOTE 1 For BL-16: C0-C3 are assumed to be '0', and are not transmitted on the command bus.
NOTE 2 For BL-16: The starting burst address is on 256-bit boundaries.
NOTE 3 For BL-16: There is no C4.
NOTE 4 For BL-32: C0-C4 are assumed to be '0', and are not transmitted on the command bus.
NOTE 5 For BL-32: The starting burst address is on 512-bit boundaries.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 18 — MR2 Register Information (MA[5:0] = 02_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU					RL		

Table 19 — MR2 Register Functions

Function	Register Type	Operand	Data	Notes
RL (Read latency)	Write Only	OP[2:0]	000 _B : RL=6 (default) 001 _B : RL=12 010 _B : RL=16 011 _B : RL=22 100 _B : RL=28 101 _B : RL=32 110 _B : RL=36 111 _B : RL=40	1,2,3
NOTE 1 See Section 4.7 Read Latencies for detail. NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address. NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.				

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 20 — MR3 Register Information (MA[5:0] = 03_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	ECCO-RD	PDDS			RFU		PU-CAL

Table 21 — MR3 Register Functions

Function	Register Type	Operand	Data	Notes
PU-Cal (Pull-up Calibration Point)	Write Only	OP[0]	0B: VDDQ*0.6 1B: VDDQ*0.5 (default)	1
PDDS (Pull-Down Drive Strength)		OP[5:3]	000B: RFU 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 (default) 111B: Reserved	1,2,3
ECCO-RD (ECC Output Enable)		OP[6]	0B: Disabled (default) 1B: Enabled	2,3,4

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 4 When enabled (OP[6]=1B) ECC information is output on the ECCO signal for the device. See Section 10.7 LPDDR4X-NVM Error Correction Code Output.

Table 22 — MR4 Register Information (MA[5:0] = 04_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Temperature Sensor Data (TSD)							

Table 23 — MR4 Register Functions

Function	Register Type	Operand	Data	Notes
Temperature Sensor Data (TSD)	Read Only	OP[7:0]	Most recent temperature measurement	1,2

NOTE 1 Temperature sensing is initiated over the SPI bus.
NOTE 2 See Section 4.18 for details.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 24 — MR5 Register Information (MA[5:0] = 05_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
LPDDR4X-NVM Manufacturer ID							

Table 25 — MR5 Register Functions

Function	Register Type	Operand	Data	Notes
Manufacturer ID	Read Only	OP[7:0]	See JEP166, Manufacturer ID Codes	

Table 26 — MR6 Register Information (MA[5:0] = 06_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-1							

Table 27 — MR6 Register Functions

Function	Register Type	Operand	Data	Notes
LPDDR4X-NVM Rev ID-1	Read Only	OP[7:0]	xxxx xxxxB: Manufacturer Specific- Rev ID-1	1

NOTE 1 MR6 is manufacturer specific.

Table 28 — MR7 Register Information (MA[5:0] = 07_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-2							

Table 29 — MR7 Register Functions

Function	Register Type	Operand	Data	Notes
LPDDR4X-NVM Rev ID-2	Read Only	OP[7:0]	xxxx xxxxB: Manufacturer Specific- Rev ID-2	1

NOTE 1 MR7 is manufacturer specific.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 30 — MR8 Register Information (MA[5:0] = 08_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
IO Width		Density				Type	

Table 31 — MR8 Register Functions

Function	Register Type	Operand	Data	Notes
Type	Read Only	OP[1:0]	00 _B : 32 byte row size 01 _B : 64 byte row size All Others: Reserved	
Density		OP[5:2]	Density= 1Mb x 2 ⁿ 0000 _B : n=0, Density= 1Mb x 2 ⁰ = 1Mb 0001 _B : n=1, Density= 1Mb x 2 ¹ = 2Mb ... 1111 _B : n=15, Density= 1Mb x 2 ¹⁵ = 32Gb	
IO Width		OP[7:6]	00 _B : x16 (per channel) All Others: Reserved	

Table 32 — MR10 Register Information (MA[5:0] = 0A_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							ZQ-Reset

Table 33 — MR10 Register Functions

Function	Register Type	Operand	Data	Notes
ZQ-Reset	Write Only	OP[0]	0 _B : Normal Operation (Default) 1 _B : ZQ Reset	1,2

NOTE 1 See Table 84, ZQCal Timing Parameters for calibration latency and timing.

NOTE 2 If the ZQ-pin is connected to V_{DDQ} through R_{ZQ}, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to V_{SS}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 34 — MR11 Register Information (MA[5:0] = 0B_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved	CA ODT			Reserved			

Table 35 — MR11 Register Functions

Function	Register Type	Operand	Data	Notes
CA ODT (CA Bus Receiver On-Die-Termination)	Write Only	OP[6:4]	000B: Disable (Default) 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 111B: RFU	1,2,3
NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.				
NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.				
NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.				

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 36 — MR12 Register Information (MA[5:0] = 0C_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR-CA	VREFCA					

Table 37 — MR12 Register Functions

Function	Register Type	Operand	Data	Notes
VREFCA (VREFCA Setting)	Read/ Write	OP[5:0]	000000B: -- Through -- 110010B: See table below (011101B: default) All Others: Reserved	1,2,3, 5,6
VR-CA (VREFCA Range)		OP[6]	0B: VREFCA Range[0] enabled 1B: VREFCA Range[1] enabled (default)	1,2,4, 5,6
NOTE 1 This register controls the V _{REFCA} levels. Refer to Table 38 - VREF Settings for Range[0] and Range[1] for actual voltage of V _{REFCA} .				
NOTE 2 A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See Section 4.9 on MRR Operation.				
NOTE 3 A write to OP[5:0] sets the internal V _{REFCA} level for FSP[0] when MR13 OP[6]=0 _B , or sets the internal VrefCA level for FSP[1] when MR13 OP[6]=1 _B . The time required for V _{REFCA} to reach the set level depends on the step size from the current level to the new level. See Section 4.12 on V _{REFCA} training for more information.				
NOTE 4 A write to OP[6] switches the LPDDR4X-NVM between two internal V _{REFCA} ranges. The range (Range[0] or Range[1]) must be selected when setting the V _{REFCA} register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.				
NOTE 5 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with a MRR command to this address.				
NOTE 6 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.				

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 38 — V_{REFCA} Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of V _{DDQ})				Range[1] Values (% of V _{DDQ})				Notes
V _{REFCA} Settings for MR12	OP[5:0]	000000 _B	15.0%	011010 _B	30.5%	000000 _B	32.9%	011010 _B	48.5%	1,2,3,4
		000001 _B	15.6%	011011 _B	31.1%	000001 _B	33.5%	011011 _B	49.1%	
		000010 _B	16.2%	011100 _B	31.7%	000010 _B	34.1%	011100 _B	49.7%	
		000011 _B	16.8%	011101 _B	32.3%	000011 _B	34.7%	011101 _B default	50.3%	
		000100 _B	17.4%	011110 _B	32.9%	000100 _B	35.3%	011110 _B	50.9	
		000101 _B	18.0%	011111 _B	33.5%	000101 _B	35.9%	011111 _B	51.5%	
		000110 _B	18.6%	100000 _B	34.1%	000110 _B	36.5%	100000 _B	52.1%	
		000111 _B	19.2%	100001 _B	34.7%	000111 _B	37.1%	100001 _B	52.7%	
		001000 _B	19.8%	100010 _B	35.3%	001000 _B	37.7%	100010 _B	53.3%	
		001001 _B	20.4%	100011 _B	35.9%	001001 _B	38.3%	100011 _B	53.9%	
		001010 _B	21.0%	100100 _B	36.5%	001010 _B	38.9%	100100 _B	54.5%	
		001011 _B	21.6%	100101 _B	37.1%	001011 _B	39.5%	100101 _B	55.1%	
		001100 _B	22.2%	100110 _B	37.7%	001100 _B	40.1%	100110 _B	55.7%	
		001101 _B	22.8%	100111 _B	38.3%	001101 _B	40.7%	100111 _B	56.3%	
		001110 _B	23.4%	101000 _B	38.9%	001110 _B	41.3%	101000 _B	56.9%	
		001111 _B	24.0%	101001 _B	39.5%	001111 _B	41.9%	101001 _B	57.5%	
		010000 _B	24.6%	101010 _B	40.1%	010000 _B	42.5%	101010 _B	58.1%	
		010001 _B	25.1%	101011 _B	40.7%	010001 _B	43.1%	101011 _B	58.7%	
		010010 _B	25.7%	101100 _B	41.3%	010010 _B	43.7%	101100 _B	59.3%	
		010011 _B	26.3%	101101 _B	41.9%	010011 _B	44.3%	101101 _B	59.9%	
		010100 _B	26.9%	101110 _B	42.5%	010100 _B	44.9%	101110 _B	60.5%	
		010101 _B	27.5%	101111 _B	43.1%	010101 _B	45.5%	101111 _B	61.1%	
		010110 _B	28.1%	110000 _B	43.7%	010110 _B	46.1%	110000 _B	61.7%	
		010111 _B	28.7%	110001 _B	44.3%	010111 _B	46.7%	110001 _B	62.3%	
		011000 _B	29.3%	110010 _B	44.9%	011000 _B	47.3%	110010 _B	62.9%	
		011001 _B	29.9%	All Others: Reserved		011001 _B	47.9%	All Others: Reserved		
NOTE 1 These values may be used for MR12 OP[5:0] to set the V _{REFCA} levels in the LPDDR4x-NVM.										
NOTE 2 The range may be selected in the MR12 register by setting OP[6] appropriately.										
NOTE 3 The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA are provided to allow for faster switching between terminated and un-terminated operation, or between different high frequency settings which may use different terminations values.										
NOTE 4 Voltage step size is 0.6% (1/167).										

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 39 — MR13 Register Information (MA[5:0] = 0D_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP	FSP-WR	RFU	RFU	VRCG	VRO	RPT	CBT

Table 40 — MR13 Register Functions

Function	Register Type	Operand	Data	Notes
CBT (Command Bus Training)	Write Only	OP[0]	0 _B : Normal Operation (default) 1 _B : Command Bus Training Mode Enabled	1
RPT (Read Preamble Training Mode)		OP[1]	0 _B : Disable (default) 1 _B : Enable	
VRO (V _{REF} Output)		OP[2]	0 _B : Normal operation (default) 1 _B : Output the V _{REF} CA value on DQ bits	2
VRCG (V _{REF} Current Generator)		OP[3]	0 _B : Normal Operation (default) 1 _B : V _{REF} Fast Response (high current) mode	3
FSP-WR (Frequency Set Point Write/Read)		OP[6]	0 _B : Frequency-Set-Point[0] (default) 1 _B : Frequency-Set-Point [1]	4
FSP-OP (Frequency Set Point Operation Mode)		OP[7]	0 _B : Frequency-Set-Point[0] (default) 1 _B : Frequency-Set-Point [1]	5
NOTE 1 A write to set OP[0]=1 causes the LPDDR4X-NVM to enter the Command Bus Training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See Section 4.13 on Command Bus Training for more information.				
NOTE 2 When set, the LPDDR4X-NVM will output the V _{REF} CA voltage on DQ pins. Only the “active” frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal V _{REF} CA levels. The DQ pins used for V _{REF} CA output are manufacturer specific.				
NOTE 3 When OP[3]=1, the V _{REF} CA circuit uses a high-current mode to improve V _{REF} CA settling time.				
NOTE 4 FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as V _{REF} CA Setting, V _{REF} CA Range. For more information, refer to Section 4.14, Frequency Set Point.				
NOTE 5 FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as V _{REF} CA Setting, V _{REF} CA Range. For more information, refer to Section 4.14 Frequency Set Point section.				

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 41 — MR15 Register Information (MA[5:0] = 0F_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower-Byte Invert Register for DQ Calibration							

Table 42 — MR15 Register Functions

Function	Register Type	Operand	Data	Notes
Lower-Byte Invert for DQ Calibration	Write Only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55H	1,2,3
NOTE 1 This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted. NOTE 2 ECCO[0] is not inverted, and always transmits the "true" data contained in MR32/MR40. NOTE 3 No ECC Output function is enacted during DQ Read Calibration, even if ECCO is enabled in MR3-OP[6].				

Table 43 — MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	ECCO[0]	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 44 — MR20 Register Information (MA[5:0] = 14_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Upper-Byte Invert Register for DQ Calibration							

Table 45 — MR20 Register Functions

Function	Register Type	Operand	Data	Notes
Upper-Byte Invert for DQ Calibration	Write Only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55H	1,2,3
NOTE 1 This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted. NOTE 2 ECCO[1] is not inverted, and always transmits the "true" data contained in MR32/MR40. NOTE 3 No ECC Output function is enacted during DQ Read Calibration, even if ECCO is enabled in MR3-OP[6].				

Table 46 — MR20 Invert Register Pin Mapping

PIN	DQ8	DQ9	DQ10	DQ11	ECCO[1]	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7