



Reproduced By GLOBAL
ENGINEERING DOCUMENTS
With The Permission of EIA
Under Royalty Agreement

EIA/JESD35-1

EIA/JEDEC STANDARD

General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics

EIA/JESD35-1

(Addendum No. 1 to EIA/JESD35)

SEPTEMBER 1995

ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT



NOTICE

EIA Engineering Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of EIA from manufacturing or selling products not conforming to such Standards and Publications, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than EIA members, whether the standard is to be used either domestically or internationally.

Standards and Publications are adopted by EIA in accordance with the American National Standards Institute (ANSI) patent policy. By such action, EIA does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the Standard or Publication.

This EIA Standard is considered to have International Standardization implication, but the International Electrotechnical Commission activity has not progressed to the point where a valid comparison between the EIA Standard and the IEC document can be made.

This Standard does not purport to address all safety problems associated with its use or all applicable regulatory requirements. It is the responsibility of the user of this Standard to establish appropriate safety and health practices and to determine the applicability of regulatory limitations before its use.

Published by

©ELECTRONIC INDUSTRIES ASSOCIATION 1995
Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201

PRICE: Please refer to the current
Catalog of EIA, JEDEC, and TIA STANDARDS and ENGINEERING PUBLICATIONS
or call Global Engineering Documents, USA and Canada (1-800-854-7179)
International (303-397-7956)

All rights reserved
Printed in U.S.A.

PLEASE!
DON'T VIOLATE
THE
LAW!

This document is copyrighted by the EIA and may not be reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies through entering into a license agreement. For information, contact:

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112-5704 or call
U.S.A. and Canada 1-800-854-7179, International (303) 397-7956

**GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES
FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS**

CONTENTS

	Page
Foreword	iii
1 Scope	1
2 Introduction	1
3 Sources of error in testing thin oxides	1
3.1 Test equipment	1
3.2 MOS properties	2
3.3 Series resistance	3
3.4 Environment/external factors	6
3.5 Parasitics	7
3.6 Damage	8
4 Electrical model	9
5 Test structure design considerations	10
6 Example test structure	14
7 References	14
Annexes	16
A	16
B	17

ADDENDUM No. 1
EIA/JESD35-1

GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS

FOREWORD

This addendum includes test structure development methodology, criteria, and examples to supplement JESD35. JESD35 describes procedures developed for estimating the overall integrity of thin oxides and as a tool for driving constant improvement in the thin oxide manufacturing process in the MOS integrated circuit manufacturing industry. Two test procedures are included in JESD35: a voltage-ramp (V-Ramp) and a current-ramp (J-Ramp).

The development methodology, criteria, and examples of structures given herein are general in purpose.

It is important to realize that these procedures should not be interpreted as a means of predicting MOS integrated circuit failure rates but rather for quick evaluation control techniques. Thus, no acceptance or rejection criteria are specified in association with these procedures.

The material contained in this publication was formulated under the cognizance of JEDEC JC-14.2 Committee and approved by the Engineering Department Executive Committee (EDEC).

ADDENDUM No. 1
EIA/JESD No. 35-1

GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS

(From Council Ballot JCB-95-01 formulated under the cognizance of JEDEC JC-14.2 on Wafer Level Reliability)

1 Scope

This addendum expands the usefulness of the JEDEC Standard No. 35 (JESD35) by detailing the various sources of measurement error that could affect the test results obtained by the ramped tests described in the JESD35. Each source of error is described and its implications on test structure design is noted. This document can be used as a guide when designing test structures for the qualification and characterization of thin oxide reliability, specifically, by implementing accelerated voltage or current ramp tests.

2 Introduction

The JESD35 describes voltage and current ramp tests for characterizing the integrity of thin dielectrics in MOS microelectronics. Two parameters, the breakdown electric field and the charge density to breakdown, are typically extracted from the test results and used as a measure of dielectric quality. The validity and accuracy of these parameters are dependent on the layout of the thin oxide test structure, test equipment accuracy, and environmental conditions. It is therefore important to understand the various sources of error that can be introduced by the above factors.

This document describes in detail the sources of error that can be encountered by test equipment, MOS properties, series resistance, environment, parasitics, and structure damage when testing thin dielectrics. An electrical model of the thin oxide test structure is provided and recommendations for its design are given.

3 Sources of error in testing thin oxides

3.1 Test equipment

Careful analysis and characterization of test equipment are necessary. Review and verification of the test equipment specifications will aid in program development. Deviations due to equipment can then be understood.