

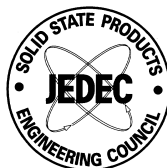
EIA/JEDEC STANDARD

**Standard for Description of
Low-Voltage TTL-Compatible,
5 V-Tolerant CMOS Logic Devices**

EIA/JESD36

JUNE 1996

**ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT**



NOTICE

EIA/JEDEC Standards and Publications contain material that has been prepared, progressively reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA General Counsel.

EIA/JEDEC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such standards shall not in any respect preclude any member or nonmember of JEDEC from manufacturing or selling products not conforming to such standards, nor shall the existence of such standards preclude their voluntary use by those other than EIA members, whether the standard is to be used either domestically or internationally.

EIA/JEDEC Standards and Publications are adopted without regard to whether their adoption may involve patents or articles, materials, or processes. By such action, EIA/JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the EIA/JEDEC Standards or Publications.

The information included in EIA/JEDEC Standards and Publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the EIA/JEDEC organization there are procedures whereby an EIA/JEDEC Standard or Publication may be further processed and ultimately becomes an ANSI/EIA Standard.

Inquiries, comments, and suggestions relative to the content of this EIA/JEDEC Standard or Publication should be addressed to the JEDEC Executive Secretary at EIA Headquarters, 2500 Wilson Boulevard, Arlington, VA 22201.

Published by

© ELECTRONIC INDUSTRIES ASSOCIATION 1997
Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201

“Copyright” does not apply to JEDEC member companies as they are free to duplicate this document in accordance with the latest revision of the JEDEC Publication 21 “Manual of Organization and Procedure”.

Standard for Description of Low Voltage TTL-Compatible, 5 V-Tolerant CMOS Logic Devices

CONTENTS

Section	Page
1 INTERFACE STANDARD	1
1.1 Purpose	1
1.2 Scope	1
2 DEFINITIONS	1
3 STANDARD SPECIFICATIONS	2
3.1 Absolute Maximum Continuous Ratings	2
3.2 Recommended Operating Conditions	2
3.3 dc Specifications	3
4 TEST CIRCUITS AND SWITCHING WAVEFORMS	4
5 REFERENCE TO OTHER APPLICABLE JEDEC STANDARDS AND PUBLICATIONS	8

Standard for Description of Low Voltage TTL-Compatible, 5 V-Tolerant CMOS Logic Devices

(From JEDEC Council Ballot JCB-95-72, formulated under the cognizance of JC-40 Committee on Digital Logic.)

1 INTERFACE STANDARD

1.1 Purpose:

To provide a standard for Low-Voltage 5 V –tolerant CMOS Logic series specifications for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

1.2 Scope:

This standard defines dc interface and switching parameters for a high-speed, low-voltage 5 V-tolerant CMOS digital logic family. This standard covers specifications for CMOS Logic series as defined in Section 2.

2 DEFINITIONS

CMOS Series

Includes devices that utilize CMOS technology.

5 V-tolerant defined within this specification means that leakage current is negligible when inputs, or outputs in the high-impedance state are exposed to voltages exceeding V_{DD} , guaranteed to 5.5 V.

Includes devices whose input logic levels are TTL-compatible.

Compliant with JEDEC standard 8-A.

Prefix

Prefix "74" immediately preceding family name indicate the operating temperature range. 74XXX refers to the Commercial (COM'L) version of devices which are specified over -40°C to 85°C .