

JEDEC STANDARD

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SERIAL PRESENCE DETECT (SPD) for DDR5 SDRAM MODULES

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SERIAL PRESENCE DETECT (SPD) for DDR5 SDRAM MODULES

From JEDEC Board Ballot JCB-23-22, formulated under the cognizance of JC-45, DRAM modules, item 2260-01Q. This standard is broken down into various clauses with their respective revision numbers below.

DDR5 SPD Document Release 1.2
Beta release 0

Base SPD revision 1.2
Soldered down annex revision 1.0
UDIMM annex revision 1.1
RDIMM/LRDIMM annex revision 1.1
MRDIMM annex revision 1.1
DDIMM annex revision 1.0
NVDIMM-N annex revision 0.1
NVDIMM-P annex revision 1.0
CAMM2 annex revision 1.0

1 Introduction / Scope

This publication describes the serial presence detect (SPD) values for all DDR5 memory modules. In this context, “modules” applies to memory modules like traditional Dual In-line Memory Modules (DIMMs) or solder-down motherboard applications. The SPD data provides critical information about all modules on the memory channel and is intended to be use by the system's BIOS in order to properly initialize and optimize the system memory channels. The storage capacity of the SPD non-volatile memory is limited, so a number of techniques are employed to optimize the use of these bytes, including overlays and run length limited coding.

All unused entries will be coded as 0x00. All unused bits in defined bytes will be coded as 0 except where noted.

Timing parameters in the SPD represent the operation of the module including all DRAMs and support devices at the lowest supported supply voltages (see SPD bytes 16 through 18), and are valid from $t_{CKAVGmin}$ to $t_{CKAVGmax}$ (see SPD bytes 20 through 23).

To allow for maximum flexibility as devices evolve, SPD fields described in this publication may support device configuration and timing options that are not included in the JEDEC DDR5 SDRAM data sheet (JESD79-5). Please refer to DRAM supplier data sheets or JESD79-5 to determine the compatibility of components.

2 History

Computer main memory buses have traditionally been defined by the generation of memory attached to the bus, e.g., EDO, SDRAM, DDR1, etc. The bus interface protocol and characteristics have largely been defined by the memory type. Clock frequency, CAS latencies, refresh recovery times and similar parameters defined the timing of signals between memory controller and the memory, and parameters such as number of ranks installed and device widths allowed system software to determine the memory capacity and similar high level characteristics of each module.

Over time, the memory bus has been extended to include additional features for application specific requirements. Registered DIMMs, for example, increased total capacity by buffering the loading of the address bus signals, allowing more DRAM to be installed. Similarly, Load Reduced DIMMs buffered the data bus as well, allowing even more ranks of memory to be supported. As each new extension to the function of the memory bus was introduced, system software combined knowledge of those extensions with information programmed into the non-volatile memory in the SPD to determine how to use and optimize the new features. Using the RDIMM as an example, systems understood that an additional clock of latency needed to be added to the DRAM latency to accommodate propagation delay through the register.

In later generations, the DRAM to host interface is completely virtualized. A memory module may have no DRAM at all, yet may use the DRAM bus to communicate with the host by emulating the DRAM channel interface. These virtual interfaces must appear to the system as one of the base module types, i.e., UDIMM, RDIMM, LRDIMM, or DDIMM. Modules that incorporate at least one non-DRAM media type for the purpose of main memory data storage are called “hybrid”, they act like a DRAM but on the other side of the interface protocol are some other memory type(s).

3 SPD Architecture

The SPD contents architecture must support the many variations of module types while remaining efficient. A system of overlay information selected through the use of “key bytes”, or selectors for the type of information to load has been implemented. The following DDR5 module SPD address map describes where the individual lookup table entries will be held in the serial non-volatile memory.

Consistent with the definition of DDR5 generation SPD devices (SPD5118) which have 16 individual write protection blocks of 64 bytes in length each, the SPD contents are aligned with these blocks as follows:

Table 1 — SPD Contents Alignment with Write Protection Blocks

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	Reserved for future use
3	192~239	0x0C0~0x0EF	Common Module Parameters -- See annex A.0 for details
	240~255	0x0F0~0x0FF	Standard Module Parameters -- See annexes A.x for details
4	256~319	0x100~0x13F	Standard Module Parameters -- See annexes A.x for details
5	320~383	0x140~0x17F	Standard Module Parameters -- See annexes A.x for details
6	384~447	0x180~0x1BF	Standard Module Parameters -- See annexes A.x for details
7	448~509	0x1C0~0x1FD	Reserved for future use
	510~511	0x1FE~0x1FF	CRC for SPD bytes 0~509
8	512~575	0x200~0x23F	Manufacturing information
9	576~639	0x240~0x27F	Manufacturing information
10	640~703	0x280~0x2BF	End User Programmable
11	704~767	0x2C0~0x2FF	End User Programmable
12	768~831	0x300~0x33F	End User Programmable
13	832~895	0x340~0x37F	End User Programmable
14	896~959	0x380~0x3BF	End User Programmable
15	960~1023	0x3C0~0x3FF	End User Programmable

3 SPD Architecture (cont'd)

Operating parameters for the different module types are defined in the following Annexes and will reside in the appropriate address ranges of the SPD address map depending on the module type. Please see Overlay Schema for further details.

Annex A.0: Common SPD Bytes for All Module Types

Annex A.1: Solder down memory applications

Annex A.2: UDIMMs

Annex A.3: RDIMM and LRDIMM

Annex A.4: MRDIMM

Annex A.5: DDIMM

Annex A.6: NVDIMM-N

Annex A.7: NVDIMM-P

Annex A.8: CAMM2

4 Overlay Schema

The following Schemas exemplify the manner in which the base configuration information along with the Annexes are to be overlaid onto the appropriate address spaces in order to provide a complete definition of the module.

4.1 Solder Down Overlay Schema

Key Byte 3 contains any of the following values:

- 0x0B, Solder Down

Table 2 — Solder Down Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.1: Solder Down
4	256~319	0x100~0x13F	Insert Annex A.1: Solder Down
5	320~383	0x140~0x17F	Insert Annex A.1: Solder Down
6	384~447	0x180~0x1BF	Insert Annex A.1: Solder Down
7~15	448~1023	0x180~0x3FF	...

4.2 UDIMM Overlay Schema

Key Byte 2 contains value 0x12 (DDR5)

Key Byte 3 contains any of the following values:

- 0x02, UDIMM
- 0x03, SODIMM

Table 3 — UDIMM Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.2: Unbuffered Memory Module Types
4	256~319	0x100~0x13F	Insert Annex A.2: Unbuffered Memory Module Types
5	320~383	0x140~0x17F	Insert Annex A.2: Unbuffered Memory Module Types
6	384~447	0x180~0x1BF	Insert Annex A.2: Unbuffered Memory Module Types
7~15	448~1023	0x180~0x3FF	...

4.3 RDIMM and LRDIMM Overlay Schema

Key Byte 2 contains value 0x12 (DDR5)

Key Byte 3 contains any of the following values:

- 0x01, RDIMM
- 0x04, LRDIMM

Table 4 — RDIMM and LRDIMM Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.3: Registered and Load Reduced Memory Module Types
4	256~319	0x100~0x13F	Insert Annex A.3: Registered and Load Reduced Memory Module Types
5	320~383	0x140~0x17F	Insert Annex A.3: Registered and Load Reduced Memory Module Types
6	384~447	0x180~0x1BF	Insert Annex A.3: Registered and Load Reduced Memory Module Types
7~15	448~1023	0x180~0x3FF	...

4.4 MRDIMM Overlay Schema

Key Byte 2 contains value 0x12 (DDR5)

Key Byte 3 contains any of the following values:

- 0x07, MRDIMM

Table 5 — MRDIMM Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.4: Multiplexed Rank Memory Module Types
4	256~319	0x100~0x13F	Insert Annex A.4: Multiplexed Rank Memory Module Types
5	320~383	0x140~0x17F	Insert Annex A.4: Multiplexed Rank Memory Module Types
6	384~447	0x180~0x1BF	Insert Annex A.4: Multiplexed Rank Memory Module Types
7~15	448~1023	0x180~0x3FF	...

4.5 DDIMM Overlay Schema

Key Byte 2 contains value 0x12 (DDR5)

Key Byte 3 contains any of the following values:

- 0x07, DDIMM

Table 6 — DDIMM Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.5: Differential Memory Module Types
4	256~319	0x100~0x13F	Insert Annex A.5: Differential Memory Module Types
5	320~383	0x140~0x17F	Insert Annex A.5: Differential Memory Module Types
6	384~447	0x180~0x1BF	Insert Annex A.5: Differential Memory Module Types
7~15	448~1023	0x180~0x3FF	...

4.6 NVDIMM-N Overlay Schema

Key Byte 2 contains value 0x12 (DDR5)

Key Byte 3 contains any of the following values:

- 0x9X, NVDIMM-N Hybrid

where X refers to the base memory architecture

Table 7 — NVDIMM-N Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.6: NVDIMM-N Memory Module Types
4	256~319	0x100~0x13F	Insert Annex A.6: NVDIMM-N Memory Module Types
5	320~383	0x140~0x17F	Insert Annex A.6: NVDIMM-N Memory Module Types
6	384~447	0x180~0x1BF	Insert Annex A.6: NVDIMM-N Memory Module Types
7~15	448~1023	0x180~0x3FF	...

4.7 NVDIMM-P Overlay Schema

Key Byte 2 contains value 0x12 (DDR5)

Key Byte 3 contains any of the following values:

- 0xAX, NVDIMM-P Hybrid
where X refers to the base memory architecture

Table 8 — NVDIMM-P Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.7: NVDIMM-P Memory Module Types
4	256~319	0x100~0x13F	Insert Annex A.7: NVDIMM-P Memory Module Types
5	320~383	0x140~0x17F	Insert Annex A.7: NVDIMM-P Memory Module Types
6	384~447	0x180~0x1BF	Insert Annex A.7: NVDIMM-P Memory Module Types
7~15	448~1023	0x180~0x3FF	...

4.8 CAMM2 Overlay Schema

Key Byte 2 contains value 0x12 (DDR5)

Key Byte 3 contains any of the following values:

- 0x08, CAMM2

Table 9 — CAMM2 Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.8: CAMM2 Memory Module Types
4	256~319	0x100~0x13F	Insert Annex A.8: CAMM2 Memory Module Types
5	320~383	0x140~0x17F	Insert Annex A.8: CAMM2 Memory Module Types
6	384~447	0x180~0x1BF	Insert Annex A.8: CAMM2 Memory Module Types
7~15	448~1023	0x180~0x3FF	...

5 Parsing the SPD

Table 10 — Some Relevant SPD Bytes for Parsing

SPD Byte(s)	Definition
1	SPD revision for the base section of the SPD
2	DRAM interface type presented or emulated
3	Memory module interface type
0~125	Base configuration and DRAM parameters
192	SPD revision for the module specific annex
192~239	Common module parameters
240~445	Module specific parameters
510~511	CRC for bytes 0~509

The system BIOS will acquire information from the SPD in order to properly configure the system's memory controller. It is assumed the BIOS will parse the SPD data in the order listed below.

Step 1: Parse Byte 1 - Verify the SPD contents.

The first step is to verify the validity of the contents of the SPD. Calculate and verify that the 16-bit cyclic redundancy check (CRC) for bytes 0~509 matches the CRC stored in bytes 510~511.

Step 2: Parse Byte 2 - Verify the installed DRAM type is supported.

The first step in parsing the SPD is to verify that the DRAM type installed is supported by looking at DRAM device type byte 2. While it is usually not possible to physically plug in the wrong memory type, for example, a DDR3 module size or key location should prevent insertion into a DDR5 system, there are cases where byte 2 is used to prevent accidental use of an incompatible memory type.

Step 3: Parse Byte 1 - Verify SPD compatibility. See Section 6 - SPD Revision Progression

The SPD revision byte 1 "encoding" nibble may be used to force legacy systems to reject newer modules. This would typically only occur if a critical error were found in SPD encoding that would require a "fix". In this case, as in the case of an unsupported DRAM type, system initialization must be halted immediately.

The SPD revision stored in Byte 1 applies to all information for the module, including base information and module specific information. Each SPD revision exactly defines how many bytes are valid in all other SPD blocks. The number of supported bytes (or bits) may increase from one SPD revision to another within each block as indicated by the "additions" nibble of the SPD revision. For example, an SPD revision 1.3 has more bytes or bits defined than SPD revision 1.2.

This progression of SPD contents is important for the BIOS to DIMM compatibility model. An older system may have a BIOS that only understands SPD revision 1.2 encoding, so if a module is installed that contains revision 1.3 information, the system can accurately interpret all of the historical revision 1.2 information retained in the module that is the subset of the revision 1.3 specification.

5 Parsing the SPD (cont'd)

Similarly, if a module with SPD revision 1.1 information is installed, that same BIOS can interpret all information that was current at the time that SPD 1.1 was defined. Therefore, BIOSes must maintain a knowledge of the active information for each historical SPD revision in order to support older modules.

New in DDR5 SPD contents definition is a separate revision byte for sections of the contents. For example, the revision byte 1 covers only the base configuration information blocks, bytes 0 to 127. There is a separate revision byte for other sections such as the standard module parameters in bytes 192-447. The same scheme of contents and additions nibbles is used in each of these sections to allow forward and backward compatibility. Having separate revision levels in various sections of the SPD contents allows those sections to change independently.

Step 4: Parse Byte 3 - Determine module type and appropriate overlays.

Key byte 3 for module type determines the subsequent use of overlay information. Byte 3 defines the host to module interface style: unbuffered, registered, load reduced, differential, or hybrid. Standard module types are defined in Annexes A.x.

Step 5: Parse Bytes 0~127 - Make base configuration settings to memory interface based on these bytes.

All module types are required to read and interpret this block of data to set up the DRAM type, maximum operating frequency, the number of row, column, bank bits, write recovery time, etc. While these bytes primarily describe the timing of the DRAMs, timing represents the capabilities of the module and it may be necessary to downgrade the timing based on other factors including layout or support components on the module, such as registers.

Step 6: Parse Byte 192 - Module-specific annex SPD revision.

This byte determines the encoding level and additions level of the module specific bytes of the SPD. Separating the base section of the SPD and module specific section prevents unnecessary churn; for example, if the UDIMM annex changes, the SPD for RDIMM/LRDIMM module need not change.

Step 7: Parse Bytes 193~447 - Configure standard module memory interface.

These bytes will be referenced and used by the system as needed based on the Standard module type that was determined after Byte 3 was parsed as indicated in Step 2. Bytes 192~239 are common byte definitions for all module types as defined in Annex A.0. Bytes 240~447 are coded differently for each standard module type as defined in Annex A.x.

6 SPD Revision Progression

SPD Contents sections have a revision code for that section of the specification. This allows each section to evolve over time independently as much as possible. For example a system may need to parse one revision level for the Base Configuration section (bytes 0~127) and a different revision level for the Standard Module Parameters section (bytes 192~447).

Table 11 — Hypothetical SPD Revision Progression Showing Revision Relationships

Section	Bytes	Revision Byte
Base Configuration and SDRAM Parameters	0~127	1
Standard Module Parameters	192~447	192

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

A hypothetical progression is shown to illustrate the relationship between feature updates, typographical error corrections, specification revisions, and dates. In order to reduce the number of module requalifications, policy is to issue SPD releases once per year, typically in June (publication to the JEDEC public site typically takes an additional 3 months from committee approval).

Table 12 — Hypothetical Progression Showing Relationship between Feature Updates, Typo Error Corrections, Spec Revisions, and Dates

Year	Description	Document	Release Date	SPD Byte 1		SPD Byte 192					
				Base	Solder Down	UDIMM	RDIMM/LRDIMM	MRDIMM	DDIMM	NVDIMM-N	NVDIMM-P
0	Initial SPD document release	JESD400-5	June 2021	1.0	1.0	1.0	1.0	N/A	1.0	0.1	0.1
0	Typographical fixes	JESD400-5	September 2021	1.0	1.0	1.0	1.0	N/A	1.0	0.1	0.1
0	Typographical fixes	JESD400-5	December 2021	1.0	1.0	1.0	1.0	N/A	1.0	0.1	0.1
1	Additions to base, RDIMM Add MRDIMM First release NVDIMM-P Pre-production additions to NVDIMM-N	JESD400-5A	June 2022	1.1	1.0	1.0	1.1	1.0	1.0	0.2	1.0
1	Typographical fixes	JESD400-5A	September 2022	1.1	1.0	1.0	1.1	1.0	1.0	0.2	1.0
1	Typographical fixes	JESD400-5A	March 2023	1.1	1.0	1.0	1.1	1.0	1.0	0.2	1.0
2	Additions to base, RDIMM, DDIMM Additions to NVDIMM-P First release NVDIMM-N	JESD400-5B	June 2023	1.2	1.0	1.0	1.2	1.0	1.1	1.0	1.1
3	Additions to base	JESD400-5C	June 2024	1.3	1.0	1.0	1.2	1.0	1.1	1.0	1.1
3	Typographical fixes	JESD400-5C	March 2025	1.3	1.0	1.0	1.2	1.0	1.1	1.0	1.1
4	Additions to base, NVDIMM-N	JESD400-5D	June 2025	1.4	1.0	1.0	1.2	1.0	1.1	1.1	1.1

7 Address Map

Table 13 shows the SPD address map for all DDR5 modules. It describes where the individual lookup table entries will be held in the serial non-volatile memory. Consistent with the definition of DDR5 generation SPD devices which have 16 individual write protection blocks of 64 bytes in length each, the SPD contents are aligned with these blocks as follows:

Table 13 — SPD Address Map for DDR5 Modules

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	Reserved for future use
3	192~239	0x0C0~0x0EF	Common Module Parameters -- See Annex A.0 for details
	240~255	0x0F0~0x0FF	Standard Module Parameters -- See annexes A.x for details
4	256~319	0x100~0x13F	Standard Module Parameters -- See annexes A.x for details
5	320~383	0x140~0x17F	Standard Module Parameters -- See annexes A.x for details
6	384~447	0x180~0x1BF	Standard Module Parameters -- See annexes A.x for details
7	448~509	0x1C0~0x1FD	Reserved for future use
	510~511	0x1FE~0x1FF	CRC for bytes 0~509
8	512~575	0x200~0x23F	Manufacturing Information
9	576~639	0x240~0x27F	Manufacturing Information
10	640~703	0x280~0x2BF	End User Programmable
11	704~767	0x2C0~0x2FF	End User Programmable
12	768~831	0x300~0x33F	End User Programmable
13	832~895	0x340~0x37F	End User Programmable
14	896~959	0x380~0x3BF	End User Programmable
15	960~1023	0x3C0~0x3FF	End User Programmable

After programming the SPD contents, suppliers of JEDEC compliant modules must set the write protect bits for SPD device blocks 0 through 7. See the SPD5118 Device Specification for details on the block protect command protocol.

Beginning with modules supporting JESD400-5 DDR5 SPD Contents Specification Revision 1.1 or higher, write protect must also be asserted after programming on block 8 in addition to write protect on blocks 0 through 7.

Blocks 0~1: Base Configuration and DRAM Parameters

These blocks define the parameters for DDR5 SDRAMs.

Block 2: Reserved for future use

Blocks 3~6: Module Specific Parameters

Bytes 192~447 (0x0C0~0x1BF) parameters in this block are specific to the module type as selected by the contents of SPD Key Byte 3 bits 3~0. Refer to the appropriate annex for detailed byte descriptions.

7 Address Map (cont'd)

Block 7: Reserved for future use

Bytes 448~509 are reserved and must be programmed as 0.

Byte 510 (0x1FE): Cyclical Redundancy Code (CRC) for SPD Bytes 0~509, Least Significant Byte
Byte 511 (0x1FF): Cyclical Redundancy Code (CRC) for SPD Bytes 0~509, Most Significant Byte

This two-byte field contains the calculated CRC for bytes 0~509 (0x000~0x1FD) in the SPD. The following algorithm and data structures (shown in C) are to be followed in calculating and checking the code.

```
int Crc16 (char *ptr, int count)
{
    int crc, i;

    crc = 0;
    while (--count >= 0) {
        crc = crc ^ (int)*ptr++ << 8;
        for (i = 0; i < 8; ++i)
            if (crc & 0x8000)
                crc = crc << 1 ^ 0x1021;
            else
                crc = crc << 1;
    }
    return (crc & 0xFFFF);
}
```

```
char spdBytes[] = { SPD_byte_0, SPD_byte_1, ..., SPD_byte_N-1 };
int data16;
```

```
data16 = Crc16 (spdBytes, sizeof(spdBytes));
SPD_byte_510 = (char) (data16 & 0xFF);
SPD_byte_511 = (char) (data16 >> 8);
```

7 Address Map (cont'd)

Blocks 8~9: Manufacturing Information

Bytes 512~639 (0x200~0x27F). Table 14 details the location of each byte in this block.

Table 14 — Location of Bytes 512~639 in Blocks 8~9

Byte Number		Function Described	Notes
512	0x200	Module Manufacturer's ID Code, First Byte	1
513	0x201	Module Manufacturer's ID Code, Second Byte	1
514	0x202	Module Manufacturing Location	1
515~516	0x203~0x204	Module Manufacturing Date	1
517~520	0x205~0x208	Module Serial Number	1
521~550	0x209~0x226	Module Part Number	1
551	0x227	Module Revision Code	
552	0x228	DRAM Manufacturer's ID Code, First Byte	1
553	0x229	DRAM Manufacturer's ID Code, Second Byte	1
554	0x22A	DRAM Stepping	
555~637	0x22B~0x27D	Module Manufacturer's Specific Data	
NOTE 1 Required byte			

Blocks 10~15: End User Programmable

Bytes 640~1023 (0x280~0x3FF). Bytes in these blocks are reserved for use by end users. Module manufacturers should not assert write protect on blocks 10~15 unless requested to do so by customers.

7.1 ASCII Decode Matrix for SPDs

Table 15 is a subset of the full ASCII standard which is used for coding bytes in the Serial Presence Detect EEPROM that require ASCII characters:

Table 15 — Subset of Full ASCII Standard

First Hex Digit in Pair	Second Hex Digit in Pair														
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E
2	Blank Space								(	)				- Dash	. Period
3	0	1	2	3	4	5	6	7	8	9					
4		A	B	C	D	E	F	G	H	I	J	K	L	M	N
5	P	Q	R	S	T	U	V	W	X	Y	Z				- Underscore
6		a	b	c	d	e	f	g	h	i	j	k	l	m	n
7	p	q	r	s	t	u	v	w	x	y	z				

Examples:

0x20 = Blank Space

0x34 = '4'

0x41 = 'A'

7.1 ASCII Decode Matrix for SPDs (cont'd)

Table 16 — SPD Bytes 521~550

Manufacturer's PN	Coded in ASCII
13M32734BCD-260Y	31334D33323733344243442D323630592020

8 Details of Each Byte

8.1 Blocks 0 and 1: General Configuration Section: Bytes 0~127 (0x000~0x07F)

This clause contains defines parameters that are common to all DDR5 module types with DDR5 SDRAM as the media type, and provides “key bytes” to allow overlay of module specific information. These bytes are defined when Key Byte 2 contains 18 (0x12), DDR5 SDRAM.

Table 17 — Blocks 0 and 1 General Configuration

Byte Number	DDR5 Function Described	Notes
0	0x000	Number of Bytes in SPD Device and Beta Level
1	0x001	SPD Revision for Base Configuration Parameters
2	0x002	Key Byte / Host Bus Command Protocol Type
3	0x003	Key Byte / Module Type
4	0x004	First SDRAM Density and Package
5	0x005	First SDRAM Addressing
6	0x006	First SDRAM I/O Width
7	0x007	First SDRAM Bank Groups and Banks Per Bank Group
8	0x008	Second SDRAM Density and Package
9	0x009	Second SDRAM Addressing
10	0x00A	Second SDRAM I/O Width
11	0x00B	Second SDRAM Bank Groups and Banks Per Bank Group
12	0x00C	SDRAM BL32 and Post Package Repair
13	0x00D	SDRAM Duty Cycle Adjuster and Partial Array Self Refresh
14	0x00E	SDRAM Fault Handling
15	0x00F	Reserved
16	0x010	SDRAM Nominal Voltage, VDD
17	0x011	SDRAM Nominal Voltage, VDDQ
18	0x012	SDRAM Nominal Voltage, VPP
19	0x013	SDRAM Timing
20	0x014	SDRAM Minimum Cycle Time ($t_{CKAVGmin}$), Least Significant Byte
21	0x015	SDRAM Minimum Cycle Time ($t_{CKAVGmin}$), Most Significant Byte
22	0x016	SDRAM Maximum Cycle Time ($t_{CKAVGmax}$), Least Significant Byte

NOTE 1 From DDR5 SDRAM datasheet.

Table 17 — Blocks 0 and 1 General Configuration (cont'd)

Byte Number		DDR5 Function Described	Notes
23	0x017	SDRAM Maximum Cycle Time ($t_{CKAVGmax}$), Most Significant Byte	1
24	0x018	CAS Latencies Supported, First Byte	1
25	0x019	CAS Latencies Supported, Second Byte	1
26	0x01A	CAS Latencies Supported, Third Byte	1
27	0x01B	CAS Latencies Supported, Fourth Byte	1
28	0x01C	CAS Latencies Supported, Fifth Byte	1
29	0x01D	Reserved	1
30	0x01E	SDRAM Read Command to First Data (t_{AA}), Least Significant Byte	1
31	0x01F	SDRAM Read Command to First Data (t_{AA}), Most Significant Byte	1
32	0x020	SDRAM Activate to Read or Write Command Delay (t_{RCD}), Least Significant Byte	1
33	0x021	SDRAM Activate to Read or Write Command Delay (t_{RCD}), Most Significant Byte	1
34	0x022	SDRAM Row Precharge Time (t_{RP}), Least Significant Byte	1
35	0x023	SDRAM Row Precharge Time (t_{RP}), Most Significant Byte	1
36	0x024	SDRAM Activate to Precharge Command Period (t_{RAS}), Least Significant Byte	1
37	0x025	SDRAM Activate to Precharge Command Period (t_{RAS}), Most Significant Byte	1
38	0x026	SDRAM Activate to Activate or Refresh Command Period (t_{RC}), Least Significant Byte	1
39	0x027	SDRAM Activate to Activate or Refresh Command Period (t_{RC}), Most Significant Byte	1
40	0x28	SDRAM Write Recovery Time (t_{WR}), Least Significant Byte	1
41	0x29	SDRAM Write Recovery Time (t_{WR}), Most Significant Byte	1
42	0x2A	SDRAM Normal Refresh Recovery Time (t_{RFC1} , t_{RFC1_slr}), Least Significant Byte	1
43	0x2B	SDRAM Normal Refresh Recovery Time (t_{RFC1} , t_{RFC1_slr}), Most Significant Byte	1
44	0x02C	SDRAM Fine Granularity Refresh Recovery Time (t_{RFC2} , t_{RFC2_slr}), Least Significant Byte	1
45	0x02D	SDRAM Fine Granularity Refresh Recovery Time (t_{RFC2} , t_{RFC2_slr}), Most Significant Byte	1
46	0x02E	SDRAM Same Bank Refresh Recovery Time (t_{RFCsb} , t_{RFCsb_slr}), Least Significant Byte	1
47	0x02F	SDRAM Same Bank Refresh Recovery Time (t_{RFCsb_dlr}), Most Significant Byte	1
48	0x030	SDRAM Normal Refresh Recovery Time, 3DS Different Logical Rank (t_{RFC1_dlr}), Least Significant Byte	1
49	0x031	SDRAM Normal Refresh Recovery Time, 3DS Different Logical Rank (t_{RFC1_dlr}), Most Significant Byte	1
50	0x032	SDRAM Fine Granularity Refresh Recovery Time, 3DS Different Logical Rank (t_{RFC2_dlr}), Least Significant Byte	1
51	0x033	SDRAM Fine Granularity Refresh Recovery Time, 3DS Different Logical Rank (t_{RFC2_dlr}), Most Significant Byte	1
NOTE 1 From DDR5 SDRAM datasheet.			

Table 17 — Blocks 0 and 1 General Configuration (cont'd)

Byte Number		DDR5 Function Described	Notes
52	0x034	SDRAM Same Bank Refresh Recovery Time, 3DS Different Logical Rank (t_{RFCsb_dlr}), Least Significant Byte	1
53	0x035	SDRAM Same Bank Refresh Recovery Time, 3DS Different Logical Rank (t_{RFCsb_dlr}), Most Significant Byte	1
54	0x036	SDRAM Refresh Management, First Byte, First SDRAM	1
55	0x037	SDRAM Refresh Management, Second Byte, First SDRAM	1
56	0x038	SDRAM Refresh Management, First Byte, Second SDRAM	1
57	0x039	SDRAM Refresh Management, Second Byte, Second SDRAM	1
58	0x03A	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM	1
59	0x03B	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM	1
60	0x03C	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM	1
61	0x03D	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM	1
62	0x03E	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM	1
63	0x03F	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM	1
64	0x040	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM	1
65	0x041	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM	1
66	0x042	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM	1
67	0x043	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM	1
68	0x044	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM	1
69	0x045	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM	1
70	0x046	SDRAM Activate to Activate Command Delay for Same Bank Group (t_{RRD_L}), Least Significant Byte	1
71	0x047	SDRAM Activate to Activate Command Delay for Same Bank Group (t_{RRD_L}), Most Significant Byte	1
72	0x048	SDRAM Activate to Activate Command Delay for Same Bank Group (t_{RRD_L}), Lower Clock Limit	1
73	0x049	SDRAM Read to Read Command Delay for Same Bank Group (t_{CCD_L}), Least Significant Byte	1
74	0x04A	SDRAM Read to Read Command Delay for Same Bank Group (t_{CCD_L}), Most Significant Byte	1
75	0x04B	SDRAM Read to Read Command Delay for Same Bank Group (t_{CCD_L}), Lower Clock Limit	1
76	0x04C	SDRAM Write to Write Command Delay for Same Bank Group ($t_{CCD_L_WR}$), Least Significant Byte	1
77	0x04D	SDRAM Write to Write Command Delay for Same Bank Group ($t_{CCD_L_WR}$), Most Significant Byte	1
78	0x04E	SDRAM Write to Write Command Delay for Same Bank Group ($t_{CCD_L_WR}$), Lower Clock Limit	1
79	0x04F	SDRAM Write to Write Command Delay for Same Bank Group, Second Write not RMW ($t_{CCD_L_WR2}$), Least Significant Byte	1
80	0x050	SDRAM Write to Write Command Delay for Same Bank Group, Second Write not RMW ($t_{CCD_L_WR2}$), Most Significant Byte	1
NOTE 1 From DDR5 SDRAM datasheet.			

Table 17 — Blocks 0 and 1 General Configuration (cont'd)

Byte Number		DDR5 Function Described	Notes
81	0x051	SDRAM Write to Write Command Delay for Same Bank Group, Second Write not RMW ($t_{CCD_L_WR2}$), Lower Clock Limit	1
82	0x052	SDRAM Four Activate Window (t_{FAW}), Least Significant Byte	1
83	0x053	SDRAM Four Activate Window (t_{FAW}), Most Significant Byte	1
84	0x054	SDRAM Four Activate Window (t_{FAW}), Lower Clock Limit	1
85	0x055	SDRAM Write to Read Command Delay for Same Bank Group ($t_{CCD_L_WTR}$), Least Significant Byte	1
86	0x056	SDRAM Write to Read Command Delay for Same Bank Group ($t_{CCD_L_WTR}$), Most Significant Byte	1
87	0x057	SDRAM Write to Read Command Delay for Same Bank Group ($t_{CCD_L_WTR}$), Lower Clock Limit	1
88	0x058	SDRAM Write to Read Command Delay for Different Bank Group ($t_{CCD_S_WTR}$), Least Significant Byte	1
89	0x059	SDRAM Write to Read Command Delay for Different Bank Group ($t_{CCD_S_WTR}$), Most Significant Byte	1
90	0x05A	SDRAM Write to Read Command Delay for Different Bank Group, ($t_{CCD_S_WTR}$), Lower Clock Limit	1
91	0x05B	SDRAM Read to Precharge Command Delay (t_{RTP} , t_{RTP_slr}), Least Significant Byte	1
92	0x05C	SDRAM Read to Precharge Command Delay (t_{RTP} , t_{RTP_slr}), Most Significant Byte	1
93	0x05D	SDRAM Read to Precharge Command Delay (t_{RTP} , t_{RTP_slr}), Lower Clock Limit	1
94	0x05E	SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (t_{CCD_M}), Least Significant Byte	1
95	0x05F	SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (t_{CCD_M}), Most Significant Byte	1
96	0x060	SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (t_{CCD_M}), Lower Clock Limit	1
97	0x061	SDRAM Write to Write Command Delay for Different Bank in Same Bank Group ($t_{CCD_M_WR}$), Least Significant Byte	1
98	0x062	SDRAM Write to Write Command Delay for Different Bank in Same Bank Group ($t_{CCD_M_WR}$), Most Significant Byte	1
99	0x063	SDRAM Write to Write Command Delay for Different Bank in Same Bank Group ($t_{CCD_M_WR}$), Lower Clock Limit	1
100	0x064	SDRAM Write to Read Command Delay for Same Bank Group ($t_{CCD_M_WTR}$), Least Significant Byte	1
101	0x065	SDRAM Write to Read Command Delay for Same Bank Group ($t_{CCD_M_WTR}$), Most Significant Byte	1
102	0x066	SDRAM Write to Read Command Delay for Same Bank Group ($t_{CCD_M_WTR}$), Lower Clock Limit	1
103~127	0x067~0x07F	Reserved -- must be coded as 0x00	
NOTE 1 From DDR5 SDRAM datasheet.			

8.1.1 (DDR5): Byte 0 (0x000): Number of Bytes in SPD Device and Beta Level

The least significant nibble of this byte describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data. Bits 6~4 describe the total size of the serial memory used to hold the Serial Presence Detect data. Bits 7,3~0 define the Beta Level of the SPD encoding.

Table 18 — Number of Bytes in SPD Device

Bit 7	Bits 6~4	Bits 3~0
Beta Level 4	SPD Bytes Total	Beta Level 3~0
See bits 3~0	000: Undefined 001: 256 010: 512 011: 1024 (e.g., SPD5118) 100: 2048 (e.g., ESPD5216) All others reserved	Bits 7,3~0: Beta Level Values 0 to 31
NOTE The 5-bit Beta Level field (bit 7 and bits 3~0) is the incremental documentation release level to track changes between major external publications of the SPD Contents specification, typically done once per year. This value shall be reset to 00000 upon each external release and will be visible only to JEDEC members between releases. The Beta Level applies to all sections of the document, including DRAM and module annex sections.		

8.1.2 (DDR5): Byte 1 (0x001): SPD Revision for Base Configuration Parameters

Base SPD revision 1.2, code as 0x12

This byte describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. Software should examine the upper nibble (Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 0x00 or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

Table 19 — SPD Revision for Base Configuration Parameters

Production Status	SPD Revision	Encoding Level				Additions Level				Hex
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Pre-production	Revision 0.0	0	0	0	0	0	0	0	0	00
	Revision 0.1	0	0	0	0	0	0	0	1	01
	...	.	.	.	.	.	.	.	.	.
	Revision 0.9	0	0	0	0	1	0	0	1	09
Production	Revision 1.0	0	0	0	1	0	0	0	0	10
	Revision 1.1	0	0	0	1	0	0	0	1	11
	...	.	.	.	.	.	.	.	.	...
Undefined	Undefined	1	1	1	1	1	1	1	1	FF

8.1.2 (DDR5): Byte 1 (0x001): SPD Revision for Base Configuration Parameters (cont'd)

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

Revisions for each module specific overlay are coded in the same format so that each module type can evolve over time independent of the base configuration parameters section.

The Beta Level (SPD byte 0, bits 7,3~0) may also be used to decode changes made since the last external publication of the SPD Contents.

8.1.3 (DDR5): Byte 2 (0x002): Key Byte / Host Bus Command Protocol Type

This byte is the key byte used by the system BIOS to determine how to interpret all other bytes in the SPD EEPROM. The BIOS must check this byte first to ensure that the EEPROM data is interpreted correctly. This command protocol is often based on the interface parameters for a specific memory device such as a DDR5 SDRAM, however may also be a general media interface protocol such as DDR5 NVDIMM-P. Protocol extensions such as the use of registers or data buffers must be documented in Byte 3, the Module Type byte, and such differences comprehended and accounted for by the system and memory controller. Some non-DRAM solutions called “Hybrid” use an extension of a DRAM bus protocol, such as NVDIMM-N, and use the code for the emulated DRAM protocol in this byte, such as DDR4 SDRAM.

Table 20 — Key Byte / Host Bus Command Protocol Type

Line #	Hex	SDRAM / Module Type Corresponding to Key Byte
0	00	Reserved
1	01	Fast Page Mode
2	02	EDO
3	03	Pipelined Nibble
4	04	SDRAM
5	05	ROM
6	06	DDR SGRAM
7	07	DDR SDRAM
8	08	DDR2 SDRAM
9	09	DDR2 SDRAM FB-DIMM
10	0A	DDR2 SDRAM FB-DIMM PROBE
11	0B	DDR3 SDRAM
12	0C	DDR4 SDRAM
13	0D	Reserved
14	0E	DDR4E SDRAM
15	0F	LPDDR3 SDRAM
16	10	LPDDR4 SDRAM
17	11	LPDDR4X SDRAM
18	12	DDR5 SDRAM
19	13	LPDDR5 SDRAM
20	14	DDR5 NVDIMM-P
21	15	LPDDR5X SDRAM
-	-	-
253	FD	Reserved
254	FE	Reserved
255	FF	Reserved

8.1.4 (DDR5): Byte 3 (0x003): Key Byte / Module Type

This byte is a Key Byte used to index the module specific section of the SPD from bytes 512~639. Byte 3 bits 3~0 identifies the SDRAM memory module type, and bits 7~4 describe hybrid memory extensions.

Some modules may have no base memory, but will have only a secondary memory type. For example, a Flash-only memory module. These are classified as “hybrid” for the purposes of interpreting the SPD. Where base memory parameters apply to this class of hybrid module, these will be documented with those bytes in the base section.

Table 21 — Key Byte / Module Type

Bit 7	Bits 6~4	Bits 3~0
Hybrid	Hybrid Media	Base Module Type
0: Not hybrid (Module is DRAM only) 1: Hybrid module (See bits 6~4 for hybrid type)	000: Not hybrid 001: NVDIMM-N Hybrid 010: NVDIMM-P Hybrid All other codes reserved	0000: Reserved 0001: RDIMM 0010: UDIMM 0011: SODIMM 0100: LRDIMM 0101: CUDIMM 0110: CSODIMM 0111: MRDIMM 1000: CAMM2 1001: Reserved 1010: DDIMM 1011: Solder down 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved
Base Module Type Definitions: Solder down: Direct attachment to memory controller RDIMM: Registered Dual In-Line Memory Module UDIMM: Unbuffered Dual In-Line Memory Module SODIMM: Unbuffered Small Outline Dual In-Line Memory Module CUDIMM: Clocked Unbuffered Dual In-Line Memory Module CSODIMM: Clocked Small Outline Dual In-Line Memory Module LRDIMM: Load Reduced Dual In-Line Memory Module MRDIMM: Multiplexed Rank Dual In-Line Memory Module CAMM2: Compression Attached Memory Module DDIMM: Differential Dual In-Line Memory Module Hybrid Memory Type Definitions: NVDIMM-N: Non-Volatile Dual In-Line Memory Module, Hybrid module with a DDR5 SDRAM interface with one or more non-DRAM components for data storage NVDIMM-P: Non-Volatile Dual In-Line Memory Module, Hybrid module with a DDR5 NVDIMM-P interface with one or more non-DRAM components for data storage		

Examples:

- 0x01: RDIMM, no hybrid memory present
- 0x91: RDIMM, NVDIMM-N hybrid memory present
- 0x94: LRDIMM, NVDIMM-N hybrid memory present
- 0x0B = soldered down memory, no hybrid memory present

8.1.5 (DDR5): Byte 4 (0x004): First SDRAM Density and Package

This byte describes the SDRAM package type, loading as seen by the system, and device density in Gbits. These values come from the DDR5 SDRAM data sheet, JESD79-5. This byte applies to the even rank SDRAMs for asymmetrical memory configurations, or for all SDRAMs for symmetrical configurations.

Table 22 — First SDRAM Density and Package

Bits 7~5	Bits 4~0
Die Per Package	SDRAM Density Per Die
000: 1 die; Monolithic SDRAM 001: 2 die; Dual-die package (DDP) 010: 2 die; 2H 3DS 011: 4 die; 4H 3DS 100: 8 die; 8H 3DS 101: 16 die; 16H 3DS All others reserved	00000: No memory; not defined 00001: 4 Gb 00010: 8 Gb 00011: 12 Gb 00100: 16 Gb 00101: 24 Gb 00110: 32 Gb 00111: 48 Gb 01000: 64 Gb All others reserved

8.1.6 (DDR5): Byte 5 (0x005): First SDRAM Addressing

This byte describes the number SDRAM column and row address bits. These values come from the DDR5 SDRAM data sheet, JESD79-5. This byte applies to the even rank SDRAMs for asymmetrical memory configurations, or for all SDRAMs for symmetrical configurations.

Table 23 — First SDRAM Addressing

Bits 7~5	Bits 4~0
First SDRAM Column Address Bits	First SDRAM Row Address Bits
000: 10 columns 001: 11 columns All others reserved	00000: 16 rows 00001: 17 rows 00010: 18 rows All others reserved

8.1.7 (DDR5): Byte 6 (0x006): First SDRAM I/O Width

This byte describes the number SDRAM I/O bits (DQ) and the number of bank groups. These values come from the DDR5 SDRAM data sheet, JESD79-5. This byte applies to the even rank SDRAMs for asymmetrical memory configurations, or for all SDRAMs for symmetrical configurations.

Table 24 — First SDRAM I/O Width

Bits 7~5	Bits 4~0
SDRAM I/O Width	Reserved
000: x4 001: x8 010: x16 011: x32 All others reserved	Reserved; must be coded as 00000

8.1.8 (DDR5): Byte 7 (0x007): First SDRAM Bank Groups and Banks Per Bank Group

This byte describes the number SDRAM banks per bank group. These values come from the DDR5 SDRAM data sheet, JESD79-5. This byte applies to the even rank SDRAMs for asymmetrical memory configurations, or for all SDRAMs for symmetrical configurations.

Table 25 — First SDRAM Bank Groups and Banks Per Bank Group

Bits 7~5	Bits 4~3	Bits 2~0
First SDRAM Bank Groups	Reserved	First SDRAM Banks Per Bank Group
000: 1 bank group 001: 2 bank groups 010: 4 bank groups 011: 8 bank groups All others reserved	Reserved; must be coded as 00	000: 1 bank per bank group 001: 2 banks per bank group 010: 4 banks per bank group All others reserved

8.1.9 (DDR5): Byte 8 (0x008): Second SDRAM Density and Package

This byte describes the SDRAM package type, loading as seen by the system, and device density in Gbits. These values come from the DDR5 SDRAM data sheet, JESD79-5. This byte applies to the odd rank SDRAMs for asymmetrical memory configurations only.

Table 26 — Second SDRAM Density and Package

Bits 7~5	Bits 4~0
Die Per Package	SDRAM Density Per Die
000: 1 die; Monolithic SDRAM 001: 2 die; Dual-die package (DDP) 010: 2 die; 2H 3DS 011: 4 die; 4H 3DS 100: 8 die; 8H 3DS 101: 16 die; 16H 3DS All others reserved	00000: No memory; not defined 00001: 4 Gb 00010: 8 Gb 00011: 12 Gb 00100: 16 Gb 00101: 24 Gb 00110: 32 Gb 00111: 48 Gb 01000: 64 Gb All others reserved
NOTE This byte is defined only for asymmetrical memory systems; for symmetrical systems this byte must be coded as 0x00.	

8.1.10 (DDR5): Byte 9 (0x009): Second SDRAM Addressing

This byte describes the number SDRAM column and row address bits. These values come from the DDR5 SDRAM data sheet, JESD79-5. This byte describes the number SDRAM bank groups. These values come from the DDR5 SDRAM data sheet, JESD79-5. This byte applies to the odd rank SDRAMs for asymmetrical memory configurations only.

Table 27 — Second SDRAM Addressing

Bits 7~5	Bits 4~0
Second SDRAM Column Address Bits	Second SDRAM Row Address Bits
000: 10 columns 001: 11 columns All others reserved	00000: 16 rows 00001: 17 rows 00010: 18 rows All others reserved
NOTE This byte is defined only for asymmetrical memory systems; for symmetrical systems this byte must be coded as 0x00.	

8.1.11 (DDR5): Byte 10 (0x00A): Secondary SDRAM I/O Width

This byte describes the number SDRAM I/O bits (DQ) and the number of bank groups. These values come from the DDR5 SDRAM data sheet, JESD79-5. This byte applies to the odd rank SDRAMs for asymmetrical memory configurations only.

Table 28 — Second SDRAM I/O Width

Bits 7~5	Bits 4~0
SDRAM I/O Width	Reserved
000: x4 001: x8 010: x16 011: x32 All others reserved	Reserved; must be coded as 00000
NOTE This byte is defined only for asymmetrical memory systems; for symmetrical systems this byte must be coded as 0x00.	

8.1.12 (DDR5): Byte 11 (0x00B): Second SDRAM Bank Groups and Banks Per Bank Group

This byte describes the number SDRAM banks per bank group. These values come from the DDR5 SDRAM data sheet, JESD79-5. This byte applies to the odd rank SDRAMs for asymmetrical memory configurations only.

Table 29 — Second SDRAM Bank Groups and Banks Per Bank Group

Bits 7~5	Bits 4~3	Bits 2~0
Second SDRAM Bank Groups	Reserved	Second SDRAM Banks Per Bank Group
000: 1 bank group 001: 2 bank groups 010: 4 bank groups 011: 8 bank groups All others reserved	Reserved; must be coded as 00	000: 1 bank per bank group 001: 2 banks per bank group 010: 4 banks per bank group All others reserved
NOTE This byte is defined only for asymmetrical memory systems; for symmetrical systems this byte must be coded as 0x00.		

8.1.13 (DDR5): Byte 12 (0x00C): SDRAM BL32 and Post Package Repair

This byte defines support for SDRAM features for burst length 32 (BL32) support and post package repair (PPR). These values come from the DDR5 SDRAM data sheet, JESD79-5.

Table 30 — SDRAM BL32 and Post Package Repair Features

Bit 7	Bit 6	Bit 5	Bit 4
sPPR Granularity	Reserved	sPPR Undo/Lock	BL32
0 = One repair element per bank group 1 = One repair element per bank	Reserved; must be coded as 0	0: sPPR Undo/Lock not supported 1: sPPR Undo/Lock supported	0: Burst length 32 not supported 1: Burst length 32 supported
Bits 3~2		Bit 1	Bit 0
Reserved		MBIST/mPPR	Reserved
Reserved; must be coded as 00		0: MBIST/mPPR not supported 1: MBIST/mPPR supported	Reserved; must be coded as 0
NOTES: MBIST = Memory Built-In Self Test PPR = Post Package Repair hPPR = Hard PPR sPPR = Soft PPR mPPR = MBIST PPR			

8.1.14 (DDR5): Byte 13 (0x00D): SDRAM Duty Cycle Adjuster and Partial Array Self Refresh

This byte describes the options for the DDR5 SDRAM duty cycle adjuster (DCA).

Table 31 — SDRAM Duty Cycle Adjuster

Bits 7~5	Bit 4	Bits 3~2	Bits 1~0
Reserved	PASR	Reserved	DCA Types Supported
Reserved; must be coded as 000	0: PASR not supported 1: PASR supported	Reserved; must be coded as 00	00 = Device does not support DCA 01 = Device supports DCA for single/2-phase internal clock(s) 10 = Device supports DCA for 4-phase internal clock(s) 11 = Reserved
NOTES: PASR = Partial Array Self Refresh DCA = Duty Cycle Adjuster			

8.1.15 (DDR5): Byte 14 (0x00E): SDRAM Fault Handling and Temperature Sense

This byte defines support for SDRAM fault handling features and for wide on-die temperature sensing range (see MR4). These values come from the DDR5 SDRAM data sheet, JESD79-5.

Table 32 — SDRAM Fault Handling Features and Temperature Sense

Bits 7~4			
Reserved; must be coded as 0000			
Bit 3	Bit 2	Bit 1	Bit 0
Wide Temperature Sense	x4 RMW/ECS Writeback Suppression	x4 RMW/ECS Writeback Suppression MR Selector	Bounded Fault
0: Wide temperature sense and reporting not supported 1: Wide temperature sense and reporting supported	0: Writeback suppression not supported 1: Writeback suppression supported	0: Writeback suppression control in MR9 1: Writeback suppression control in MR15	0: Bounded Fault not supported 1: Bounded Fault supported
NOTES: ECS = Error Check Scrub RMW = Read-Modify-Write MR = Mode Register			

8.1.16 (DDR5): Byte 15 (0x00F): Reserved

Reserved; must be coded as 0x00.

8.1.17 (DDR5): Byte 16 (0x010): SDRAM Nominal Voltage, VDD

This byte describes the voltage levels for the SDRAM VDD supply only.

'Operable' is defined as the VDD voltage at which module operation is allowed using the performance values programmed in the SPD.

'Endurant' is defined as the VDD voltage at which the module may be powered without adversely affecting the life expectancy or reliability. Operation is not supported at this voltage.

Table 33 — SDRAM Nominal Voltage, VDD

Nominal	Operable	Endurant
Bits 7~4	Bits 3~2	Bits 1~0
0000: 1.1 V All others reserved	00: 1.1 V All others reserved	00: 1.1 V All others reserved

8.1.18 (DDR5): Byte 17 (0x011): SDRAM Nominal Voltage, VDDQ

This byte describes the voltage levels for the SDRAM VDDQ supply only.

'Operable', 'Endurant': See byte 16.

Table 34 — SDRAM Nominal Voltage, VDDQ

Nominal	Operable	Endurant
Bits 7~4	Bits 3~2	Bits 1~0
0000: 1.1 V All others reserved	00: 1.1 V All others reserved	00: 1.1 V All others reserved

8.1.19 (DDR5): Byte 18 (0x012): SDRAM Nominal Voltage, VPP

This byte describes the voltage levels for the SDRAM VPP supply only.

'Operable', 'Endurant': See byte 16.

Table 35 — SDRAM Nominal Voltage, VPP

Nominal	Operable	Endurant
Bits 7~4	Bits 3~2	Bits 1~0
0000: 1.8 V All others reserved	00: 1.8 V All others reserved	00: 1.8 V All others reserved

8.1.20 (DDR5): Byte 19 (0x013): SDRAM Timing

This byte describes whether the SDRAM uses only standard core timings per JESD79-5, or non-standard timings for markets such as overclocking systems. Core timings refer to tCKmin, tAmin, tRCDmin, and tRPmin. This information assists in determining the most robust algorithm for calculating valid CAS latency settings.

Table 36 — SDRAM Timing

Reserved	Non-Standard Core Timing
Bits 7~1	Bit 0
Reserved; must be coded as 0000000	0 = SDRAM uses standard core timings per JESD79-5 1 = SDRAM supports non-standard core timings