

JEDEC STANDARD

DDR5 DIMM Labels

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DDR5 DIMM LABELS

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DDR5 DIMM Labels

(From JEDEC Board Ballot JCB-21-29, formulated under the cognizance of the JC-45 Committee on DRAM Modules, item 2268.08).

1 Scope

The following labels shall be applied to all DDR5 memory modules to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggg, are to be omitted when not needed.

Hybrid modules appear to the system with a “base module type” compatible interface. For example, an NVDIMM-N may be constructed with an RDIMM-style interface or an LRDIMM-style interface. What specific functions the module provides are described in an “Hybrid Media Type” field (‘n’), essentially a functional overlay on the base module type.

Terminology:

Rank or Package Rank: Collection of SDRAMs on a DIMM sharing a common chip select or copy of a chip select. Chip selects may be sourced by the host controller or by a redriver device such as registering clock driver.

Logical Rank: 3DS stacked DDR5 SDRAMs decode which internal die is selected by decoding chip identifiers (CIDs) in the command. Each package rank, therefore, may contain multiple logical ranks per package rank, increasing module capacity.

Channel: Addresses, clocks, data and associated signals that span the width of the DIMM interface from and to the host controller.

Sub-channel: The data across the width of the DDR5 standard DIMMs is divided into two independent sub-channels, each with half the data width of the full DDR5 channel. For example, an RDIMM with 80 data bits of width is internally divided into two sub-channels of 40 bits each (32 data bits and 8 ECC bits).

Example: DDR5 MRDIMM 2Rx8

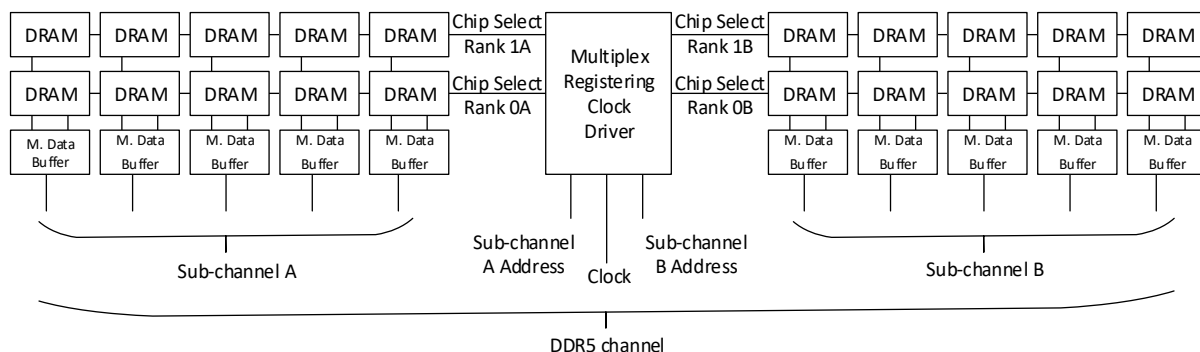


Figure 1 — Example Label

2 DDR5 DIMM Label Format for DRAM-only Module Types Except MRDIMM

DDR5 DIMM labels for DRAM-only memory modules contain four required sections: a module type section, a technical detail section, a serial number section, and a machine-readable section. The first three sections are recommended in order on the label, but the 4th section, machine readable, may be placed anywhere it fits on the label.

2.1 Module Type Section

DDR5 **dimm_type**

Where:

dimm_type = one of:

UDIMM	EC4 UDIMM	SODIMM	EC4 SODIMM
EC4 RDIMM	EC8 RDIMM	EC8 LRDIMM	DDIMM

2.2 Technical Detail Section

gggGB pheeRxff PC5-wwwwaa-mccd-bbss-ttt

Where:

gggGB = Module total capacity, in gigabytes, for primary bus (ECC not counted). **gggTB** for terabytes.
ggg is in natural numbers, e.g., 1GB, 2GB, 4GB, 1TB, etc. (no space between digits and units)

pheeR = Number of package ranks of memory per DIMM and number of logical ranks per package rank.

p =

1 = 1 package rank of SDRAMs per sub-channel
2 = 2 package ranks of SDRAMs per sub-channel
4 = 4 package ranks of SDRAMs per sub-channel

hee =

blank = monolithic DRAM (SDP = single die package)
D2 = Dual die package (DDP)
S2 = Single load SDRAM stack (3DS), 2 logical ranks in each package rank
S4 = Single load SDRAM stack (3DS), 4 logical ranks in each package rank
S8 = Single load SDRAM stack (3DS), 8 logical ranks in each package rank
S16 = Single load SDRAM stack (3DS), 16 logical ranks in each package rank

R = rank(s)

xff = Device organization (data bit width) of SDRAMs used on this assembly

x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization

www = SDRAM maximum data rate in Mb/s/data pin

3200
3600
4000

2.2 Technical Detail Section (cont'd)

4400
4800
5200
5600
6000
6400
6800
7200
7600
8000
8400
8800

aa = SDRAM speed grade

aa = Speed grade, i.e., AN, B, BN, C

sobco

2.2 Technical Detail Section (cont'd)

Table 1 — Examples of DDR5 Monolithic or DDP Components

DDR5 Monolithic Components			
SDRAM Speed Grade	CAS Latency	tRCD in nCK	tRP in nCK
3200AN	24	24	24
3200B	26	26	26
3200BN	26	26	26
3200C	28	28	28
3600AN	26	26	26
3600B	30	30	30
3600BN	30	30	30
3600C	32	32	32
4000AN	28	28	28
4000B	32	32	32
4000BN	32	32	32
4000C	36	35	35
4400AN	32	32	32
4400B	36	36	36
4400BN	36	36	36
4400C	40	39	39
4800AN	34	34	34
4800B	40	39	39
4800BN	40	40	40
4800C	42	42	42
5200AN	38	38	38
5200B	42	42	42
5200BN	42	42	42
5200C	46	46	46
5600AN	40	40	40
5600B	46	45	45
5600BN	46	46	46
5600C	50	49	49
6000AN	42	42	42
6000B	48	48	48
6000BN	48	48	48
6000C	54	53	53
6400AN	46	46	46
6400B	52	52	52
6400BN	52	52	52
6400C	56	56	56
6800AN	48	48	48
6800B	56	55	55
6800BN	56	56	56
6800C	60	60	60
7200AN	52	52	52
7200B	58	58	58
7200BN	58	58	58
7200C	64	63	63

2.2 Technical Detail Section (cont'd)

Table 2 — Examples of DDR5 3DS Stacked Components

DDR5 3DS Stacked Components			
SDRAM Speed Grade	CAS Latency	tRCD in nCK	tRP in nCK
3200AN 3DS	26	24	24
3200B 3DS	30	26	26
3200BN 3DS	30	26	26
3200C 3DS	32	28	28
3600AN 3DS	30	26	26
3600B 3DS	34	30	30
3600BN 3DS	34	30	30
3600C 3DS	36	32	32
4000AN 3DS	32	28	28
4000B 3DS	38	32	32
4000BN 3DS	38	32	32
4000C 3DS	40	35	35
4400AN 3DS	36	32	32
4400B 3DS	42	36	36
4400BN 3DS	42	36	36
4400C 3DS	44	39	39
4800AN 3DS	34	34	34
4800B 3DS	46	39	39
4800BN 3DS	46	40	40
4800C 3DS	48	42	42
5200AN 3DS	42	38	38
5200B 3DS	50	42	42
5200BN 3DS	50	42	42
5200C 3DS	52	46	46
5600AN 3DS	46	40	40
5600B 3DS	52	45	45
5600BN 3DS	52	46	46
5600C 3DS	56	49	49
6000AN 3DS	48	42	42
6000B 3DS	56	48	48
6000BN 3DS	56	48	48
6000C 3DS	60	53	53
6400AN 3DS	52	46	46
6400B 3DS	60	52	52
6400BN 3DS	60	52	52
6400C 3DS	64	56	56
6800AN 3DS	56	48	48
6800B 3DS	64	55	55
6800BN 3DS	64	56	56
6800C 3DS	68	60	60
7200AN 3DS	58	52	52
7200B 3DS	68	58	58
7200BN 3DS	68	58	58
7200C 3DS	72	63	63

