

JEDEC STANDARD

JEDEC Module Sideband Bus (SidebandBus)

JESD403-1B

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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JEDEC MODULE SIDEBAND BUS (SIDEBANDBUS)

From JEDEC Board Ballot JCB-22-29, formulated under the cognizance of the JC-45 Committee on DRAM Modules, item 2260.56A.

1 Scope

This standard defines the assumptions for the system management bus for next generation memory solutions; covering the interface protocol, use of hub devices, and voltages appropriate to these usages.

2 Terminology

This standard has been updated to utilize terms with preferred social and cultural connotations.

Table 1 — Terminology

Term	Definition
CCC	Common command code.
Controller	A SidebandBus Controller device controls information flow on the I3C Basic bus. It drives the bus clock and coordinates data flow. It provides pull-up voltages on the Host bus data lines.
HID	Host identifier. This 3-bit field uniquely selects one out of up to eight Hub devices on the Host bus. It defines the three least significant bits of the Hub's I3C Basic device address.
Host	SidebandBus/I3C Basic bus Controller.
Host bus	I3C Basic bus between the Controller and Hubs or other I3C Target devices not isolated behind a Hub.
HSA	Host SidebandBus bus device ID address pin; input to a Hub or other Target device to distinguish between identical devices in the I3C Basic address range.
HSCL	Host SidebandBus bus clock, supplied by the Controller.
HSDA	Host SidebandBus data, connected from the Controller to Hubs or Host bus Target devices.
Hub	A SidebandBus Hub is a device that isolates loads on the I3C Basic bus, increasing the number of supported devices on a bus. It provides pull-up voltages on the local bus data lines.
I3C Basic	Serial bus specification defined in coordination with MIPI used as a basis for SidebandBus.
LID	Local identifier. This 4-bit device type identifier uniquely defines one of up to 15 devices on a local bus. It defines the four most significant digits of the local bus device's I3C Basic address.
Local bus	I3C Basic bus between a Hub and Target devices isolated by the Hub from the Host bus.
LSA	Local bus SidebandBus device ID address pin to distinguish between identical devices in the I3C Basic address range.
LSCL	Local SidebandBus clock, driven by the Hub to local bus Target devices.
LSDA	Local SidebandBus data, connected from the Hub to local bus Target devices.
Controller	Replacement for "Master" per the latest Terminology update
PEC	Packet error code.
PMIC	Power management integrated circuit; i.e., voltage regulator.
SA	SidebandBus device ID address pin, generically (Host or Local bus).
SCL	SidebandBus clock, generically (Host or Local bus).
SDA	SidebandBus data, generically (Host or Local bus).
SidebandBus	System management bus for next generation memory solutions, based on I3C Basic.
Target	Replacement for "Slave" per the latest Terminology update
SPD	Serial Presence Detect Hub device.
Target device	A SidebandBus Target device receives input from a Controller device or as pass-through on a Local bus from a Hub device.

3 Protocol

The JEDEC Module Sideband Bus (SidebandBus) architecture is compliant to and compatible with MIPI I3C Basic, a two-wire interface based on SDA (data) and SCL (clock) that is backward compatible with I²C.

Extensions to I3C Basic include the definition of load-isolation hub devices to increase the number of supported devices and provide explicit identification of the physical location of such devices (e.g., slot identification). The specific reference documents are:

- MIPI Alliance Specification for I3C BasicSM Version 1.0 – 19 July 2018
- MIPI I3C BasicSM Target Reset Version 1.0 – 13 December 2018

This clause documents the additional details and conformance waivers to I3C Basic specification to enable the SidebandBus usage. In most cases, I3C Basic and SidebandBus are used interchangeably; differences between them are noted. For detailed operation of modes, please refer to I3C SDR mode in MIPI-I3C Specification above.

3.1 Pins

3.1.1 Serial Clock (SCL)

This pin/signal is used to strobe data in and out of the device. This signal driven is by the bus Controller using a push-pull driver to achieve higher data rates in I3C-SDR mode. It is also possible to use an open-drain driver in the bus Controller, provided that the board has a pull-up resistor connected between SCL and the I/O power supply.

3.1.2 Serial Data (SDA)

This bi-directional pin/signal is used to transfer data in or out of the device. It can operate in open drain mode or push-pull mode. A pull up resistor may be connected from Serial Data (SDA) to I/O power supply with on-die terminations on the Controller which could, optionally, be turned off in push-pull mode. If on-chip termination on the Controller is missing, a pull-up resistor must be present on the board.

3.2 I2C Mode

At power on, SidebandBus devices operate in I²C mode at up to 1 MHz (FM+ / Fast Mode Plus). This is an open drain I/O mode where the pull-up to VDDIO is supplied by the host bus Controller for the Host bus, and the Hub device for the Local bus. On either Host or Local bus, pull-up may be supplied by external pull-up resistors as well, however, operation is limited to I²C mode only in a configuration with external pull-ups.

- In-band interrupts are **not** supported in I2C Mode.
- SidebandBus does **not** support clock stretching in I2C Mode.
- Packet error codes (PECs) are **not** supported in I2C mode.
- Multi-Controller capability is **not** supported.
- SidebandBus devices must support bus RESET via a timed low pulse on the SCL line.
- Compliant to I3C Specification, all devices shall be able to handle (ACK and process the mandatory CCCs listed in Sec 4.5.2, and ACK/NACK other CCCs based on specific device requirements) broadcast CCCs when in I2C Mode. Host / Controller shall ensure functional dependency on CCCs are followed – for e.g., SETHID must be sent before SETAASA. Direct CCCs shall be NACK-ed, until the dynamic address is assigned with SETAASA CCC.

3.3 Bus Reset Schemes

SidebandBus devices shall support the SCL pulled-low timeout reset scheme.

3.3.1 Timed RESET

Bus timeout via a timeout pulse on SCL is required in both I²C and I3C Basic mode. Availability of this function is documented in the DEVCAPS CCC.

To prevent a malfunctioning device from locking up the SidebandBus, a bus protocol RESET mechanism is defined. It uses a timeout mechanism on HSCL as shown in Figure 1. All devices (including a Hub, if present, and all Target devices behind the Hub) on an I²C or I3C bus are RESET simultaneously. Bus reset operation works same way regardless of whether device is operating in I²C or I3C Basic Bus mode.

To guarantee the device resets I²C bus or I3C bus, the SCL clock input LOW time shall be greater than or equal to $t_{\text{TIMEOUT}}(\text{Max})$. The device does not reset the I2C bus or I3C bus if the HSCL clock input LOW time is less than $t_{\text{TIMEOUT}}(\text{Min})$.

If the SCL clock input LOW time is between $t_{\text{TIMEOUT}}(\text{Min})$ and $t_{\text{TIMEOUT}}(\text{Max})$, the device may or may not reset the I²C bus or I3C Basic bus. Refer to Figure 1 for details.

When a SidebandBus Reset is detected, SidebandBus compliant devices shall do the following.

- Reset the interface to power on reset state and any pending command or transaction is cleared.
- All internal register values including error and interrupt status bits are preserved, except for PEC_ERR (PEC Error) and PROT_ERR (Protocol/Parity Error) fields reported in GET_STATUS CCC which shall be cleared to 'b0. Exact register location / offset for these fields are device specific.
- The device resets to the I²C mode of operation [power on state – PEC disabled, IBI disabled, Parity Enabled, HID set to 'b111]. HUB devices shall not reset (but retain) HID, since they do not re-sample the HSA pin.
- Device floats SDA pin such that it gets pulled High by the external pull-up.

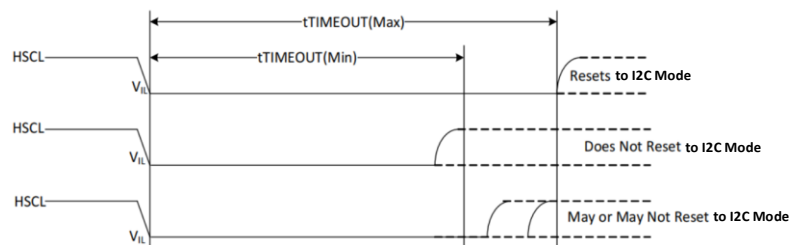


Figure 1 — I2C or I3C Basic Timed RESET

3.3.1.1 Impact of Timed RESET on I3C Devices

Pure MIPI-I3C Specification compliant Target devices that have no notion of timed-reset will ignore the timed-reset sustained SCL low condition, and not treat or report it as an error. An explanatory note on the above is available in the MIPI-I3C FAQ.

3.3.2 Pattern RESET

Pattern reset, also known as MIPI I3C Target Reset, will not be supported on JESD403-1 bus.

3.4 Bus Initialization Sequence

Figure 2 indicates the usage of SETHID and SETAASA for mode change including the effects of reset.

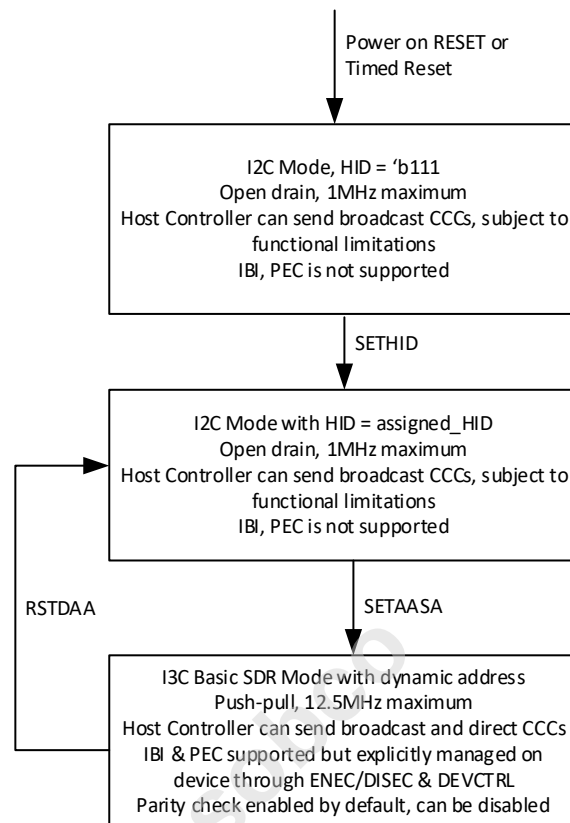


Figure 2 — State / Mode Transition Diagram

The recommended method to check if a dynamic address is assigned and the device is in I3C Basic mode is to issue a direct GET CCC like GETSTATUS. Direct CCCs shall only be ACK-ed once the dynamic address is assigned.

3.5 I3C Basic Mode

SidebandBus devices are put into I3C Basic single data rate (SDR) mode using the SETAASA common command code, which is preceded by a broadcast 7'h7E.

- Controller SCL clock stalling is supported.
- Secondary Controller support is not required.
- SDR mode only; no HDR modes supported.
- No mixing of device protocols. All devices will be in I²C Mode OR I3C Basic Mode.
- Address arbitration optimization is not supported; (after a START, the first address byte is always in open-drain)
- Hot Join is not supported.
- Timing Control Support is not supported.

3.5.1 Address Assignment and Enumeration

SidebandBus uses a specific and structured addressing scheme as described below to identify DIMMs (memory modules) and devices on the DIMMs. Hence, I3C Basic's ENTDA and PID based address enumeration scheme is not mandated.

3.5.1.1 Static Address

The 7-bit Static Address for each connected device on the bus is determined by the 4-bit Local Device address (LID, also known as Device Type Identifier, DTI) and the 3-bit Host Device address (HID). The HID bits are used to indicate the DIMM_ID on which the device resides and can range from 'b000 to 'b111, and default to 'b111, except the hub, which determines the HID from its own implementation specific mechanism like precision resistors.

I2C Bus and I3C Bus address:

- Target Address[6:3] = LID / DTI. The assigned DTI/LID values for known device types are documented in Section 4.2 Device Map of this standard.
- Target Address[2:0] = HID, also known as DIMM_ID

The Static Address is used for performing transactions on the bus when the device is in I2C mode.

3.5.1.2 Broadcast Address

The Sideband Bus standard uses 0x7E as the broadcast address, based on MIPI I3C Specification.

3.5.1.3 Address Enumeration and HID Assignment Through the HUB

The power on default value of the HID portion of the Static Address is 'b111. The Hub SPD detects the HID/DIMM_ID using the precision resistor and assists in the assignment of HID, also called DIMM_ID, using two modes.

3.5.1.3.1 HID Modification Scheme

In this mode, which is the power on default, the Hub SPD replaces the LSB 3-bits (HID) of the Target address for the addressed DIMM, except broadcast address of 0x7E, on **each** transaction to 'b111, as documented in Clause 5. Note that all devices power up with a default value of 'b111 for HID.

PEC is **not** supported in this mode.

This mode is in effect until a SETHID CCC is received. Once the Hub detects a SETHID CCC, the Hub shall no longer do the HID bit flipping, and shall transparently pass the incoming 7 bit Target address as is to the local bus. Note that a SETAASA can only be issued following SETHID.

3.5.1.3.2 HID Propagation with SETHID

The Host Controller shall issue a broadcast SETHID CCC to propagate and assign the HID on **all** connected devices, across Hubs. The Hub SPD replaces the 3 bits of the SETHID CCC's payload with its detected HID, known to it through mechanisms like precision resistor.

The devices receiving the SETHID CCC shall use the HID bits in the payload to update the LSB 3 bits of the Target address internally. Once this is done, the device shall only respond to the updated static address with received/assigned HID. A timed reset sets HID back to 'b111.

3.5.1.3.2 HID Propagation with SETHID (cont'd)

The SETHID CCC is documented in Section 3.5.2.7 Set HID Command (SETHID) Operation of this standard.

This assigned HID remains valid until a bus reset (SCL-timeout based reset) is detected or power cycle occurs. On any of these events the devices and the Hub SPD shall transition to the HID Modification Scheme.

3.5.1.3.3 HID Transparent Scheme

Once a SETHID CCC is successfully effectuated across the bus, the Hub SPD shall no longer perform the HID bit flipping and shall transparently pass the incoming 7 bit Target address as is to the local bus.

PEC can be optionally supported in this mode.

3.5.1.4 Dynamic Address

On reception of a SETAASA Command, the current static address is converted/deemed to be the dynamic address as well, and the device is in I3C Basic SDR mode of operation.

Note that SETAASA is a broadcast command, and the host issues just one SETAASA command to move the entire bus into I3C Basic SDR mode, with dynamic address assigned.

A dynamic address can be reset using the RSTDAA command or a bus reset (SCL low-timeout based) or a power-cycle. When the dynamic address is reset, the device shall keep its assigned HID and return to I2C open-drain mode. Note that the assigned HID is only reset to 'b111 on a timed-reset or a power-cycle.

3.5.1.5 Support for ENTDA and 48-bit Provisional ID

SidebandBus compliance does not need ENTDA and PID to be supported mandatorily, since the addressing scheme is based on the LID and HID concept as described above. Host bus Controllers on the SidebandBus should be aware of the bus topology and device types through alternate means like enumeration tables and should use SETAASA for dynamic address assignment and mode transition to I3C Basic SDR mode. If ENTDA is not supported, SidebandBus devices shall NACK them, as with any other unsupported CCCs.

However, note that supporting ENTDA and PID on SidebandBus devices enable these devices to be used with generic I3C Controllers that may want to use ENTDA and/or SETNEWD to re-assign addresses.

A JESD403-1 compliant Target device supporting ENTDA that intends to be on the Local bus (behind the Hub), must follow the following rules. Please refer to Clause 3.9 on Interoperability considerations.

- a. Must support ENTDA **instead** of SETAASA.
- b. These Target devices shall update the Instance_ID field of the 48 bit provisional ID with the HID value received in SETHID CCC.
- c. DCR.Device_ID should be "1101 <DTI>". These Device ID values are reserved in MIPI DCR registry for JESD403-1 SidebandBus Standard.

Generic Target devices supporting ENTDA can seamlessly co-exist with SidebandBus devices that do not support ENTDA or PID, provided they can support the full dynamic address range. Refer to the enumeration sequence in Section 3.9 on Interoperability considerations.

3.5.1.5 HID Propagation with SETHID (cont'd)

The choice of SETAASA for enumeration is driven by the overall bus discovery and enumeration time with a fully loaded JESD403-1 bus with about 40 devices. It is recommended that all standard Sideband bus devices follow the SETAASA approach to enable bus enumeration with just 2 broadcast commands – SETHID and SETAASA.

3.5.2 Common Command Codes (CCCs)

The I3C Basic specification lists large number of Common Command Codes (CCC). Common command codes that are mandatory for Sideband Bus devices are listed in Table 2. All rules for CCCs documented in I3C Basic Specification are applicable and devices shall ignore all unsupported CCCs.

Note that some devices may have restrictions in cascading different transactions.

CCC is an I3C concept by definition, and shall always conform to I3C SDR timings, irrespective of whether the device has switched from I2C mode or not.

Prior to dynamic address assignment (SETAASA/P), the Target Device(s) may drive the ACK/NACK past the Open Drain SCL rising but before the next SCL falling transition, as a longer overlap in Open Drain is harmless. Immediately after the Open Drain ACK (upon the next SCL falling edge), the bus should transition to push pull mode (though still at 1Mhz) as described in the MIPI I3C Basic Specification V1.0, Section 5.1.2.3 “Handoff from Address ACK to SDR Controller Write Data” and Figure 32 “I3C Data Transfer – ACK by Target”.

For additional details on how to handle an the ACK transition, please refer to the MIPI I3C Basic Specification V1.0, Section 5.1.2.3.1 “Transition from Address ACK to SDR Controller Write Data”

A host shall issue a STOP in the following conditions

- Immediately following an ENEC, DISEC, SETAASA, RSTDAA and SETHID CCCs.
- After a CCC operation, before any private device specific Write or Read transactions, and vice versa.
- After any direct CCC, before a broadcast CCC.

A host may use Repeat Start

- Between direct CCC and any other direct CCC
- Between any broadcast CCC and any other broadcast CCC
- Between any private Write or Read operation to any other private Write or Read mode operation.

3.5.2 Common Command Codes (CCCs) (cont'd)

Table 2 — Required CCCs

CCC	Mode	Code	Description	Notes
SETBUSCON	Broadcast	0x0C	Set Bus Context to JEDEC (128 decimal) for generic devices. This is optional for DDR5 components, but mandatory for generic devices that desire to sit on JESD403-1 bus.	
ENEC	Broadcast	0x00	Enable event interrupts	
	Direct	0x80		
DISEC	Broadcast	0x01	Disable event interrupts	
	Direct	0x81		
RSTDAA	Broadcast	0x06	Put the device in I2C Mode (Reset dynamic address assignment)	2
SETAASA	Broadcast	0x29	Put the device in I3C Mode (Set all addresses to static address)	
SETHID	Broadcast	0x61	Hub updates 3-bit HID field, updates “T” bit with updated parity calculation for all devices behind hub and stops 3-bit HID translation	1
DEVCTRL	Broadcast	0x62	Configure hub and all devices behind hub	1
Reserved	Broadcast	0x63	Reserved	1
Reserved	Broadcast	0x64	Reserved	1
GETSTATUS	Direct Get	0x90	Get device status	
DEVCAPS	Direct	0xE0	Get device capabilities	1
Reserved	Direct	0xE1	Reserved	1
Reserved	Direct	0xE2	Reserved	1
Reserved	Direct	0xE3	Reserved	1
NOTE 1 JEDEC Specific command				
NOTE 2 Direct RSTDAA is not supported since mix bus configuration is not supported. This direct CCC is deprecated in MIPI I3C v1.1 Specification				

The following Common command codes are not required to be supported for baseline JESD403-1 Compliance but may **optionally** be supported to claim full compliance to MIPI I3C Specification and enable devices to be used on any generic I3C bus.

- ENTAS[0~3]
- ENTDA
- SETMWL
- SETMRL
- SETNEWDA
- GETPID, GETBCR, GETDCR
- Any other CCC not specifically stated as supported in the MIPI I3C Basic Specification is not required

All Sideband Bus Target devices shall ignore any unsupported directed CCCs and ignore unsupported / unimplemented broadcast CCCs, in compliance with MIPI I3C Basic Specification. All broadcast CCCs subject to functional usage restrictions, can be issued by Controller / Host in I2C mode, as well, but direct GET/SET CCCs can only be issued in I3C mode (after dynamic address assignment is done).

Please refer to the I3C Basic Version 1.0 Specification document for details on the encoding and usage of all MIPI standard I3C commands.

The following sub-clauses define the restrictions / customizations for Sideband Bus devices relative to Standard I3C CCCs. For all details of the specific CCCs, please refer to MIPI I3C Specification v1.0.

3.5.2.1 PEC Support for CCCs

If PEC is enabled, all CCCs will have an additional PEC byte, as the last byte of CCC, preceding a STOP or RESTART. If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

SETAASA and SETHID CCCs do not support PEC. PEC needs to be enabled explicitly on devices using the DEVCTRL CCC.

Note that when CCCs are cascaded with restarts, errors from previous transactions (before RESTART) may cause the current transaction to be NACKed.

3.5.2.2 Enable/Disable Events Command (ENEC/DISEC) Operation

The only event type mandatorily supported by SidebandBus devices for ENEC/DISEC Command are **Target Interrupt Requests**. All other event types are not required and ignored. After receiving an ENEC, devices shall be able to initiate IBI transactions either with a START on the bus (initiated by Controller) or when the bus is IDLE for a duration of t_{AVAL} or more.

The host shall end ENEC and DISEC CCC with a STOP, and these CCCs shall be effective on the device on this STOP. It should be noted that while the host can issue a DISEC broadcast when in I2C mode (prior to dynamic address assignment), an ENEC is recommended to be send only after devices are in I3C mode.

Generic devices desirous of complying to JESD403-1 Standard and be used on JEDEC Module Sideband bus must support SETBUSCONTEXT CCC with 128 (JEDEC) as the defining byte. Such devices would have ENHJ/DISHJ and ENCR/DISCR fields valid in this CCC, and the bus Controller/host shall use these fields to disable Hot Join and Controller Request.

Table 3 — ENEC/DISEC CCC (Broadcast, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x00 (ENEC) / 0x01 (DISEC)								T	
	0	0	0	0	ENHJ / DISHJ *	0	ENCR / DISCR *	ENINT / DISINT	T	P
Note (*) SidebandBus devices ignore HJ (Hot Join) and CR (Control Request) bits.										

3.5.2.2 Enable/Disable Events Command (ENEC/DISEC) Operation (cont'd)

Table 4 — ENEC/DISEC CCC (Broadcast, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x00 (ENEC) / 0x01 (DISEC)								T	
	0	0	0	0	ENHJ / DISHJ *	0	ENCR / DISCR *	ENINT / DISINT	T	
	PEC								T	
NOTE	(*) SidebandBus devices ignore HJ (Hot Join) and CR (Control Request) bits.									

Table 5 — ENEC/DISEC CCC (Direct, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x80 (Direct ENEC) or 0x81 (Direct DISEC)								T	
Sr	DTI				Assigned_HID			W = 0	A	
	0	0	0	0	ENHJ / DISHJ *	0	ENCR / DISCR *	ENINT / DISINT	T	P
NOTE (*) SidebandBus devices ignore HJ (Hot Join) and CR (Control Request) bits.										

Table 6 — ENEC/DISEC CCC (Direct, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x80 (Direct ENEC) or 0x81 (Direct DISEC)								T	
	PEC(8)								T	
Sr	DTI				Assigned_HID			W = 0	A	
	0	0	0	0	ENHJ/ * DISHJ	0	ENCR/* DISCR	ENINT/ DISINT	T	
	PEC(8)								T	
NOTE	(*) SidebandBus devices ignore HJ (Hot Join) and CR (Control Request) bits.									