

JEDEC STANDARD

LPDDR5/5X Serial Presence Detect (SPD) Contents

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CAMM annex	1.0

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Serial Presence Detect (SPD) for LPDDR5/5X SDRAM Modules

(From JEDEC Board Ballot JCB-24-33, formulated under the cognizance of the JC-45 committee on DRAM Modules, item number 2268.09B).

LPDDR5/5X SPD, Document Release 1.0

Base SPD, Revision 1.0

Soldered Down Annex, Revision 1.0

CAMM2 Annex, Revision 1.0

1 Introduction / Scope

This standard describes the serial presence detect (SPD) values for all LPDDR5/5X memory modules. In this context, “modules” applies to memory modules like traditional Dual In-line Memory Modules (DIMMs) or solder-down motherboard applications. The SPD data provides critical information about all modules on the memory channel and is intended to be use by the system's BIOS in order to properly initialize and optimize the system memory channels. The storage capacity of the SPD non-volatile memory is limited, so a number of techniques are employed to optimize the use of these bytes, including overlays and run length limited coding.

All unused entries will be coded as 0x00. All unused bits in defined bytes will be coded as 0 except where noted.

Timing parameters in the SPD represent the operation of the module including all DRAMs and are valid from $t_{CKAVGmin}$ to $t_{CKAVGmax}$ (see SPD bytes 18, 19, 124, and 125).

To allow for maximum flexibility as devices evolve, SPD fields described in this document may support device configuration and timing options that are not included in the JEDEC LPDDR5/5X SDRAM standard (JESD209-5). Please refer to DRAM supplier data sheets or JESD209-5 to determine the compatibility of components.

2 History

Computer main memory buses have traditionally been defined by the generation of memory attached to the bus, e.g., EDO, SDRAM, DDR1, etc. The bus interface protocol and characteristics have largely been defined by the memory type. Clock frequency, CAS latencies, refresh recovery times and similar parameters defined the timing of signals between memory controller and the memory, and parameters such as number of ranks installed and device widths allowed system software to determine the memory capacity and similar high level characteristics of each module.

Over time, the memory bus has been extended to include additional features for application specific requirements. Registered DIMMs, for example, increased total capacity by buffering the loading of the address bus signals, allowing more DRAM to be installed. Similarly, Load Reduced DIMMs buffered the data bus as well, allowing even more ranks of memory to be supported.

As each new extension to the function of the memory bus was introduced, system software combined knowledge of those extensions with information programmed into the non-volatile memory in the SPD to determine how to use and optimize the new features. Using the RDIMM as an example, systems understood that an additional clock of latency needed to be added to the DRAM latency to accommodate propagation delay through the register.

3 SPD Architecture

The SPD contents architecture must support the many variations of module types while remaining efficient. A system of overlay information selected through the use of “key bytes”, or selectors for the type of information to load has been implemented. The following LPDDR5/5X module SPD address map describes where the individual lookup table entries will be held in the serial non-volatile memory.

Consistent with the definition of LPDDR5/5X generation SPD devices (SPD5118) which have 16 individual write protection blocks of 64 bytes in length each, the SPD contents are aligned with these blocks as follows:

Table 1 — LPDDR5/5X Module SPD Address Map

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration, DRAM, and Module Parameters
1	64~127	0x040~0x07F	Base Configuration, DRAM, and Module Parameters
2	128~191	0x080~0x0BF	Reserved for future use
3	192~239	0x0C0~0x0EF	Common Module Parameters -- See annex A.0 for details
	240~255	0x0F0~0x0FF	Standard Module Parameters -- See annexes A.x for details
4	256~319	0x100~0x13F	Standard Module Parameters -- See annexes A.x for details
5	320~383	0x140~0x17F	Standard Module Parameters -- See annexes A.x for details
6	384~447	0x180~0x1BF	Standard Module Parameters -- See annexes A.x for details
7	448~509	0x1C0~0x1FD	Reserved for future use
	510~511	0x1FE~0x1FF	CRC for SPD bytes 0~509
8	512~575	0x200~0x23F	Manufacturing information
9	576~639	0x240~0x27F	Manufacturing information
10	640~703	0x280~0x2BF	End User Programmable
11	704~767	0x2C0~0x2FF	End User Programmable
12	768~831	0x300~0x33F	End User Programmable
13	832~895	0x340~0x37F	End User Programmable
14	896~959	0x380~0x3BF	End User Programmable
15	960~1023	0x3C0~0x3FF	End User Programmable

Operating parameters for the different module types are defined in the following Annexes and will reside in the appropriate address ranges of the SPD address map depending on the module type. Please see Overlay Schema for further details.

- Annex A.0: Common SPD Bytes for All Module Types
- Annex A.1: Solder down memory applications
- Annex A.2 through A.7: Reserved
- Annex A.8: CAMM2

4 Overlay Schema

The following Schema exemplify the manner in which the base configuration information along with the Annexes are to be overlaid onto the appropriate address spaces in order to provide a complete definition of the module.

4.1 Solder Down Overlay Schema

Key Byte 3 contains any of the following values:

- 0x0B, Solder Down

Table 2 — Solder Down Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.1: Solder Down
4	256~319	0x100~0x13F	Insert Annex A.1: Solder Down
5	320~383	0x140~0x17F	Insert Annex A.1: Solder Down
6	384~447	0x180~0x1BF	Insert Annex A.1: Solder Down
7~15	448~1023	0x1C0~0x3FF	...

4.2 CAMM2 Overlay Schema

Key Byte 2 contains value 0x13 (LPDDR5) or 0x15 (LPDDR5X)

Key Byte 3 contains any of the following values:

- 0x08, CAMM2

Table 3 — CAMM2 Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration, DRAM, and Module Parameters
1	64~127	0x040~0x07F	Base Configuration, DRAM, and Module Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.8: CAMM2 Memory Module Types
4	256~319	0x100~0x13F	Insert Annex A.8: CAMM2 Memory Module Types
5	320~383	0x140~0x17F	Insert Annex A.8: CAMM2 Memory Module Types
6	384~447	0x180~0x1BF	Insert Annex A.8: CAMM2 Memory Module Types
7~15	448~1023	0x1C0~0x3FF	...

5 Parsing the SPD

Table 4 — Some Relevant SPD Bytes for Parsing

SPD Byte(s)	Definition
1	SPD revision for the base section of the SPD
2	DRAM interface type presented or emulated
3	Memory module interface type
0~125	Base configuration, DRAM, and Module parameters
192	SPD revision for the module specific annex
192~239	Common module parameters
240~445	Module specific parameters
510~511	CRC for bytes 0~509

The system BIOS will acquire information from the SPD in order to properly configure the system's memory controller. It is assumed the BIOS will parse the SPD data in the order listed below.

Step 1: Parse Byte 1 - Verify the SPD contents.

The first step is to verify the validity of the contents of the SPD. Calculate and verify that the 16-bit cyclic redundancy check (CRC) for bytes 0~509 matches the CRC stored in bytes 510~511.

Step 2: Parse Byte 2 - Verify the installed DRAM type is supported.

The first step in parsing the SPD is to verify that the DRAM type installed is supported by looking at DRAM device type byte 2. While it is usually not possible to physically plug in the wrong memory type, for example a DDR3 module size or key location should prevent insertion into a DDR5 system, there are cases where byte 2 is used to prevent accidental use of an incompatible memory type.

Step 3: Parse Byte 1 - Verify SPD compatibility. See Section 6 - SPD Revision Progression

The SPD revision byte 1 “encoding” nibble may be used to force legacy systems to reject newer modules. This would typically only occur if a critical error were found in SPD encoding that would require a “fix”. In this case, as in the case of an unsupported DRAM type, system initialization must be halted immediately.

The SPD revision stored in Byte 1 applies to all information for the module, including base information and module specific information. Each SPD revision exactly defines how many bytes are valid in all other SPD blocks. The number of supported bytes (or bits) may increase from one SPD revision to another within each block as indicated by the “additions” nibble of the SPD revision. For example, an SPD revision 1.3 has more bytes or bits defined than SPD revision 1.2.

This progression of SPD contents is important for the BIOS to DIMM compatibility model. An older system may have a BIOS that only understands SPD revision 1.2 encoding, so if a module is installed that contains revision 1.3 information, the system can accurately interpret all of the historical revision 1.2 information retained in the module that is the subset of the revision 1.3 specification. Similarly, if a module with SPD revision 1.1 information is installed, that same BIOS can interpret all information that was current at the time that SPD 1.1 was defined. Therefore, BIOSes must maintain a knowledge of the active information for each historical SPD revision in order to support older modules.

5 Parsing the SPD (cont'd)

New in the LPDDR5/5X SPD contents definition is a separate revision byte for sections of the contents. For example, the revision byte 1 covers only the base configuration information blocks, bytes 0 to 127. There is a separate revision byte for other sections such as the standard module parameters in bytes 192-447. The same scheme of contents and additions nibbles is used in each of these sections to allow forward and backward compatibility. Having separate revision levels in various sections of the SPD contents allows those sections to change independently.

Step 4: Parse Byte 3 - Determine module type and appropriate overlays.

Key byte 3 for module type determines the subsequent use of overlay information. Byte 3 defines the host to module interface style: unbuffered, registered, load reduced, differential, or hybrid. Standard module types are defined in Annexes A.x.

Step 5: Parse Bytes 0~127 - Make base configuration settings to memory interface based on these bytes.

All module types are required to read and interpret this block of data to set up the DRAM type, maximum operating frequency, the number of row, column, bank bits, write recovery time, etc. While these bytes primarily describe the timing of the DRAMs, timing represents the capabilities of the module and it may be necessary to downgrade the timing based on other factors including layout or support components on the module, such as registers.

Step 6: Parse Byte 192 - Module-specific annex SPD revision.

This byte determines the encoding level and additions level of the module specific bytes of the SPD. Separating the base section of the SPD and module specific section prevents unnecessary churn; for example, if the CAMM annex changes, the SPD for soldered down need not change.

Step 7: Parse Bytes 193~447 - Configure standard module memory interface.

These bytes will be referenced and used by the system as needed based on the Standard module type that was determined after Byte 3 was parsed as indicated in Step 2. Bytes 192~239 are common byte definitions for all module types as defined in Annex A.0. Bytes 240~447 are coded differently for each standard module type as defined in Annex A.x.

6 SPD Revision Progression

SPD Contents sections have a revision code for that section of the specification. This allows each section to evolve over time independently as much as possible. For example a system may need to parse one revision level for the Base Configuration section (bytes 0~127) and a different revision level for the Standard Module Parameters section (bytes 192~447).

Hypothetical SPD Revision Progression Showing Revision Relationships		
Section	Bytes	Revision Byte
Base Configuration, SDRAM, and Module Parameters	0~127	1
Standard Module Parameters	192~447	192

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

A hypothetical progression is shown to illustrate the relationship between feature updates, typographical error corrections, specification revisions, and dates. In order to reduce the number of module requalifications, policy is to issue SPD releases once per year, typically in June (publication to the JEDEC public site typically takes an additional 3 months from committee approval).

Table 5 — Hypothetical SPD Revision Progression

Year	Description	Document	Release Date	SPD Byte 1	SPD Byte 192	
				Base	Soldered Down	CAMM2
0	Initial SPD document release	JESD406-5	June 2024	1.0	1.0	1.0
0	Typographical fixes	JESD406-5	September 2024	1.0	1.0	1.0
0	Typographical fixes	JESD406-5	December 2024	1.0	1.0	1.0
1	Additions to base, CAMM2	JESD406-5A	June 2025	1.1	1.0	1.1
1	Typographical fixes	JESD406-5A	September 2025	1.1	1.0	1.1
1	Typographical fixes	JESD406-5A	March 2026	1.1	1.0	1.1
2	Additions to base, Soldered Down	JESD406-5B	June 2026	1.2	1.1	1.1
3	Additions to base	JESD406-5C	June 2026	1.3	1.1	1.1
3	Typographical fixes	JESD406-5C	March 2027	1.3	1.1	1.1

7 Address Map

Table 6 is the SPD address map for all LPDDR5/5X modules. It describes where the individual lookup table entries will be held in the serial non-volatile memory. Consistent with the definition of LPDDR5/5X generation SPD devices which have 16 individual write protection blocks of 64 bytes in length each, the SPD contents are aligned with these blocks as follows:

Table 6 — SPD Address Map for all LPDDR5/5X Modules

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration, DRAM, and Module Parameters
1	64~127	0x040~0x07F	Base Configuration, DRAM, and Module Parameters
2	128~191	0x080~0x0BF	Reserved for future use
3	192~239	0x0C0~0x0EF	Common Module Parameters -- See Annex A.0 for details
	240~255	0x0F0~0x0FF	Standard Module Parameters -- See annexes A.x for details
4	256~319	0x100~0x13F	Standard Module Parameters -- See annexes A.x for details
5	320~383	0x140~0x17F	Standard Module Parameters -- See annexes A.x for details
6	384~447	0x180~0x1BF	Standard Module Parameters -- See annexes A.x for details
7	448~509	0x1C0~0x1FD	Reserved for future use
	510~511	0x1FE~0x1FF	CRC for bytes 0~509
8	512~575	0x200~0x23F	Manufacturing Information
9	576~639	0x240~0x27F	Manufacturing Information
10	640~703	0x280~0x2BF	End User Programmable
11	704~767	0x2C0~0x2FF	End User Programmable
12	768~831	0x300~0x33F	End User Programmable
13	832~895	0x340~0x37F	End User Programmable
14	896~959	0x380~0x3BF	End User Programmable
15	960~1023	0x3C0~0x3FF	End User Programmable

After programming the SPD contents, suppliers of JEDEC compliant modules must set the write protect bits for SPD device blocks 0 through 8. See the SPD5118 Device Specification for details on the block protect command protocol.

Blocks 0~1: Base Configuration, DRAM, and Module Parameters

These blocks define the parameters for LPDDR5/5X SDRAMs and limited parameters for the modules. Limited module information is being retained in blocks 0~1 to reduce enable greater firmware reuse for systems utilizing LPDDR3 and LPDDR4 SPD standard byte definitions prior to the creation of this LPDDR5/5X standard.

Block 2: Reserved for Future Use

Blocks 3~6: Module Specific Parameters

Bytes 192~447 (0x0C0~0x1BF). Parameters in this block are specific to the module type as selected by the contents of SPD Key Byte 3 bits 3~0. Refer to the appropriate annex for detailed byte descriptions.

7 Address Map (cont'd)

Block 7: Reserved for future use

Bytes 448~509 are reserved and must be programmed as 0.

Byte 510 (0x1FE): Cyclical Redundancy Code (CRC) for SPD Bytes 0~509, Least Significant Byte

Byte 511 (0x1FF): Cyclical Redundancy Code (CRC) for SPD Bytes 0~509, Most Significant Byte

This two-byte field contains the calculated CRC for bytes 0~509 (0x000~0x1FD) in the SPD. The following algorithm and data structures (shown in C) are to be followed in calculating and checking the code.

```
int Crc16 (char *ptr, int count)
{
    int crc, i;

    crc = 0;
    while (--count >= 0) {
        crc = crc ^ (int)*ptr++ << 8;
        for (i = 0; i < 8; ++i)
            if (crc & 0x8000)
                crc = crc << 1 ^ 0x1021;
            else
                crc = crc << 1;
    }
    return (crc & 0xFFFF);
}

char spdBytes[] = { SPD_byte_0, SPD_byte_1, ..., SPD_byte_N-1 };
int data16;

data16 = Crc16 (spdBytes, sizeof(spdBytes));
SPD_byte_510 = (char) (data16 & 0xFF);
SPD_byte_511 = (char) (data16 >> 8);
```

Blocks 8~9: Manufacturing Information

Bytes 512~639 (0x200~0x27F). The following table details the location of each byte in this block.

Byte Number		Function Described	Notes
512	0x200	Module Manufacturer's ID Code, First Byte	1
513	0x201	Module Manufacturer's ID Code, Second Byte	1
514	0x202	Module Manufacturing Location	1
515~516	0x203~0x204	Module Manufacturing Date	1
517~520	0x205~0x208	Module Serial Number	1
521~550	0x209~0x226	Module Part Number	1
551	0x227	Module Revision Code	
552	0x228	DRAM Manufacturer's ID Code, First Byte	1
553	0x229	DRAM Manufacturer's ID Code, Second Byte	1
554	0x22A	DRAM Stepping	
555~639	0x22B~0x27F	Module Manufacturer's Specific Data	
NOTE 1 Required byte			

Blocks 10~15: End User Programmable

Bytes 640~1023 (0x280~0x3FF). Bytes in these blocks are reserved for use by end users. Module manufacturers should not assert write protect on blocks 10~15 unless requested to do so by customers.

ASCII Decode Matrix for SPDs

Table 7 is a subset of the full ASCII standard which is used for coding bytes in the Serial Presence Detect EEPROM that require ASCII characters:

Table 7 — ASCII Decode Matrix for SPDs

First Hex Digit in Pair	Second Hex Digit in Pair															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	Blank Space								(	)				- Dash	.	Period
3	0	1	2	3	4	5	6	7	8	9						
4		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z					- Under-score
6		a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z					

Examples:

0x20 = Blank Space

0x34 = '4'

0x41 = 'A'

SPD Bytes 521~550	
Manufacturer's PN	Coded in ASCII
13M32734BCD-260Y	31334D333237333344243442D323630592020

8 Details of Each Byte

8.1 Blocks 0 and 1: General Configuration Section: Bytes 0~127 (0x000~0x07F)

This section defines parameters common to all modules with LPDDR5 or LPDDR5X SDRAM as the media type and provides “key bytes” to allow overlay of module specific information. These bytes are defined when Key Byte 2 contains 19 (0x13) for LPDDR5 SDRAM or 21 (0x15) for LPDDR5X SDRAM.

Table 8 — General Configuration Section: Bytes 0~127 (0x000~0x07F)

Byte Number		LPDDR5/5X Function Defined	Notes
0	0x000	Number of Bytes in SPD Device and Beta Level	
1	0x001	SPD Revision for Base Configuration Parameters	
2	0x002	Key Byte / Host Bus Command Protocol Type	
3	0x003	Key Byte / Module Type	
4	0x004	SDRAM Density and Banks	1
5	0x005	SDRAM Addressing	1
6	0x006	SDRAM Package Type	1
7	0x007	Reserved - Must be coded as 0x00	
8	0x008	Reserved - Must be coded as 0x00	
9	0x009	Optional SDRAM Features	1
10	0x00A	Reserved - Must be coded as 0x00	
11	0x00B	Reserved - Must be coded as 0x00	
12	0x00C	Module Organization	1
13	0x00D	Bus Width	
14	0x00E	Reserved - Must be coded as 0x00	
15	0x00F	Reserved - Must be coded as 0x00	
16	0x010	Signal Loading	1
17	0x011	Timebases	
18	0x012	Minimum Cycle Time ($t_{CKAVGmin}$), MTB	1
19	0x013	Maximum Cycle Time ($t_{CKAVGmax}$), MTB	1
20	0x014	Reserved - Must be coded as 0x00	
21	0x015	Reserved - Must be coded as 0x00	
22	0x016	Reserved - Must be coded as 0x00	
23	0x017	Reserved - Must be coded as 0x00	
24	0x018	Minimum CAS Latency Time (t_{AAmin}), MTB	1
25	0x019	Reserved - Must be coded as 0x00	1
26	0x01A	Minimum RAS to CAS Delay Time (t_{RCDmin}), MTB	1
27	0x01B	All Banks Minimum Row Precharge Delay Time ($t_{RPabmin}$), MTB	1
28	0x01C	Per Bank Minimum Row Precharge Delay Time ($t_{RPpbmin}$), MTB	1
29	0x01D	All Banks Minimum Refresh Recovery Delay Time ($t_{RFCabmin}$), MTB, LSB	1