JEDEC STANDARD

Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements

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TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENTS

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Foreword

The measurement of the junction-to-ambient ($R_{\theta JA}$) thermal characteristics of an integrated circuit (IC) has historically been carried out using a number of test fixturing methods. The most prominent method is the soldering of the packaged devices to a printed circuit board (PCB). The characteristics of the test PCBs can have a dramatic (>60%) impact on the measured $R_{\theta JA}$. Due to this wide variability, it is desirable to have an industry-wide standard for the design of PCB test boards to minimize discrepancies in measured values between companies.

To obtain consistent measurements of $R_{\theta JA}$ from one company to the next, the test PCB geometry and trace layout must be completely specified for each package geometry tested. Such a complete specification would limit the flexibility of user companies who would like to design test boards for their individual needs. Thus, one characteristic of a test board specification is to allow some variability of PCB test board design while minimizing measurement variability.

This specification is intended for use with the thermal measurements and modeling specifications grouped under JEDEC EIA/JESD 51, [1]. Specifically, the electrical test procedures described in JEDEC EIA/JESD 51-1, “Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device),” [2], and 51-2, “Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air), [3], and 51-6, “Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air), [4].

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