

JEDEC STANDARD

Guidelines for Reporting and Using Electronic Package Thermal Information

JESD51-12.01

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Guidelines for Reporting and Using Electronic Package Thermal Information

(From JEDEC Board Ballot, JCB-05-68, formulated under the cognizance of the JC-15.1 Subcommittee on Thermal Characterization.)

1 Scope

This document provides guidelines for both reporting and using electronic package thermal information generated using JEDEC JESD51 standards. By addressing these two areas, this document can be used as the common basis for discussion between electronic package thermal information suppliers and users.

The first goal is for the electronic package thermal information to be reported consistently by different suppliers. Suppliers may choose to summarize the results or present a subset of the results, but the complete test information should be available on request. The complete information to be reported is documented in the various JESD51 standards, but key elements are consolidated in this guideline for easy reference by both suppliers and users.

The second goal is for end users to be able to properly understand, interpret and use the data reported. The purpose of the JESD51 standards is to compare the thermal performance of various packages under standardized test conditions. While standardized thermal test information cannot apply directly to the many specific applications, the standardized results can help compare the relative thermal performance of different packages. A more meaningful comparison is possible if the test conditions are understood along with the factors affecting package thermal performance. Brief discussions of key topics are included in this guideline.

2 Normative references

The following standards contain provisions that, through reference in this text, constitute provisions of this guideline. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on these standards are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

- [1] JESD51, *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Devices)*. This is the overview document for this series of specifications.
- [2] JESD51-1, *Integrated Circuit Thermal Measurement Method - Electrical Test Method*
- [3] JESD51-2, *Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- [4] JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- [5] JESD51-4, *Thermal Test Chip Guideline (Wire Bond Type Chip)*
- [6] JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

2 Normative references (cont'd)

- [7] JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)*
- [8] JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- [9] JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board*
- [10] JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*
- [11] JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*
- [12] JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*
- [13] JESD15-3, *Two-Resistor Compact Thermal Model Standard*
- [14] JESD15-4, *DELPHI Compact Thermal Model Guideline*

3 Terms, Definitions, symbols, and abbreviations

Standard JESD51 [1] is an overview document that introduces the electronic package thermal resistance concept. Most definitions and symbols are included in JESD51-1 [2], Annex A. JESD51-2 [3], Annex A includes definitions for the junction-to-top and top-to-air thermal characterization parameters. The junction-to-board thermal characterization parameter is introduced in JESD51-6 [7] and the junction-to-board thermal resistance test method is in JESD51-8 [9].

4 Reporting electronic package thermal results

The JEDEC JESD51 family of standards defines the methodology necessary for making meaningful thermal measurements on packages containing single chip semiconductor devices. Different aspects of the methodology are defined in separate detailed standards. To measure one component thermal value the supplier follows one standard from each of the categories in Table 1.

The JEDEC Theta-JCx standard is under development. While Theta-JC measurements have been common for years (for example, Mil Std 883C Method 1012.1), it is very difficult to define a measurement method which provides accurate and repeatable results covering a wide range of package designs, sizes, and power dissipation. The nomenclature used in this document is consistent with the standard being developed. For the 2R model discussed in 5.2.4, the method by which Theta-JC_{top} was determined must be reported.

4 Reporting electronic package thermal results (cont'd)

Table 1 — JESD51 Thermal measurement standards by category

ENVIRONMENT ¹	CHIP	BOARD ⁴	MEASUREMENT METHOD
- Natural Convection (Still Air), one cubic foot enclosure, θ_{JA}, Ψ_{JT} [3]² - Forced Convection (Moving Air), wind tunnel, θ_{JMA}, Ψ_{JT}, Ψ_{JB} [7] - Junction-to-Board, θ_{JB} [9] - Junction-to-Case, θ_{JCx}³	- Thermal Test Chip – Wire Bond Type [5] - Thermal Test Chip – Flip Chip Type (not yet available; refer to [5] for applicable information) - Active Die or Thermal Test Die [2]	- Low Effective Thermal Conductivity (1s board), Leaded Surface Mount Packages [4,6⁵] - High Effective Thermal Conductivity (2s2p board), Leaded Surface Mount Packages [8,6⁴] - Area Array Surface Mount Packages (1s and 2s2p boards) [10] - Through-Hole Perimeter Leaded Packages (1s and 2s2p boards) [11] - Through-Hole Area Array Leaded Packages (1s and 2s2p boards) [12]	Static Mode or Dynamic Mode; Active Die or Thermal Test Die [2]

NOTE 1 In some cases the environment standards identify which test board cross-section (see note 3) is to be used when measuring a particular thermal value.

- θ_{JA} – the board used must be indicated [3]
- θ_{JMA} – 1s board, unless indicated otherwise [7]
- θ_{JB} – 2s2p board [9]; Ψ_{JB} is also normally measured on the 2s2p board [7]

A 1s board may not be practical for high lead count components. More discussion of the boards is included in 5.3.2.

NOTE 2 Ψ_{JB} was not included in the natural convection standard [3]; it had not yet been defined. It may be added in the future. Ψ_{JB} can be measured in the natural convection environment, but it is normally measured on a 2s2p board, and in the forced convection environment, including the zero forced convection condition [7].

NOTE 3 The JEDEC θ_{JCx} standard is under development. While θ_{JC} measurements have been common for years (for example, Mil Std 883C Method 1012.1), it is very difficult to define a measurement method which provides accurate and repeatable results covering a wide range of package designs, sizes, and power dissipation. The nomenclature used in this document (see 5.2.2) is consistent with the standard being developed. For the 2R model discussed in 5.2.4, the method by which θ_{JCtop} was determined must be reported

NOTE 4 Two test board cross-sections are defined in the JESD51 standards.

- The first cross-section is referred to as the low effective thermal conductivity or 1s board. The 1s refers to the one signal layer on the component side of the board, so the board is sometimes referred to as a single layer board. Limited signals are permitted on the opposite side actually making it a 2s or two layer board. The key point is that this board does not have power planes (0p). The signal layer traces are 0.070 mm (2 oz/ft²) finished copper thickness.
- The second cross-section is referred to as the high effective thermal conductivity or 2s2p board. It has significantly more copper. The 2s refers to the signal layers on both outside surfaces of the board and the 2p refers to two power planes in the board (voltage and ground). The board is sometimes referred to as a four layer board. The signal layer traces are 0.070 mm (2 oz/ft²) finished copper thickness and the power planes are 0.035 mm (1 oz/ft²) finished copper thickness.
- For packages with ball pitch ≤ 0.5 mm the traces are reduced to 0.050 mm (1.5 oz/ft²) finished copper thickness for both boards. [10]
- Test boards designed according to JEDEC JESD51 standards are referred to as JEDEC JESD51 boards or JESD51 boards. JEDEC does not make thermal test boards available.

NOTE 5 Reference [6] extends board standards [4] and [8] for packages with direct thermal attach mechanisms such as deep down-set exposed pad packages or thermally tabbed packages.

4 Reporting electronic package thermal results (cont'd)

Following a selected set of these standards allows the supplier to report the thermal information included in the Environment column. Each of the standards also has a table at the end that tells the component supplier what test condition information is to be reported for that aspect of the test. The following statement is from the JESD51 Overview, Clause 5:

"Thermal data are not meaningful unless all pertinent test condition information is provided with the actual thermal data ... (The) documents for each of the measurement areas...state the thermal information necessary for a complete description of the data."

Table 2 thru Table 11 of this document identify some of the key elements from the standards that affect the thermal results.

Suppliers may choose to summarize the results or present a subset of the results, but the complete test information should be available on request. Suppliers may deviate from the JEDEC standards and still provide valuable data. Such deviations are to be identified.

When reporting information from tests run according to the JESD51 standards, suppliers are encouraged to indicate this in their reports and datasheets, together with any deviations. An example is given here.

"This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org. Deviations from the JESD51 standards are noted on page xx."

5 Using standardized thermal results

5.1 General problems using standardized thermal results

Several factors affect the thermal performance of a device in a user's application. These include power dissipation in the component; airflow velocity, direction and turbulence level; power in adjacent components; two-sided vs. one-sided active component mounting; printed circuit board (PCB) orientation; and adjacent boards and their power dissipation.

Ways in which the JESD51 test condition may not match a specific application include

- Die size
- Printed circuit board size
- Amount of copper on the application boards vs. the JESD51 2s2p board
- Copper trace thickness – JESD51 0.070 mm (2 oz/ft²) copper vs. application 0.018 mm (1/2 oz/ft²) copper, for example
- Trace widths – JESD51 widths may be larger than trace widths in the application, for example
- Environment – JESD51 natural convection one cubic foot enclosure vs. a cell phone, for example
- Single heat source vs. multiple heat sources in the application

5 Using standardized thermal results (cont'd)

5.1 General problems using standardized thermal results (cont'd)

For specific applications, component and system level thermal engineers should be consulted. It may be necessary to test or model specific applications. This may require special thermal test vehicles involving application-specific boards and thermal test die.

Numerical modeling of the thermal performance of a component in a JESD51 standardized test can be used as a basis for modeling of the component in a specific application. To accomplish this, detailed package geometry and material information is required from the component supplier. Alternatively, the supplier may provide compact models that can be incorporated in numerical models (see 5.2.4).

This testing and modeling of a component user's specific applications is the user's responsibility, but the work may be performed by component suppliers or consultants.

5.2 JESD51 standardized thermal values

The thermal resistances and thermal characterization parameters that are generated using JESD51 standards are described here together with their typical uses. All have the units of $^{\circ}\text{C}/\text{W}$.

Reported results are generally average values. Standard deviation or range information may be available in some cases, or on request.

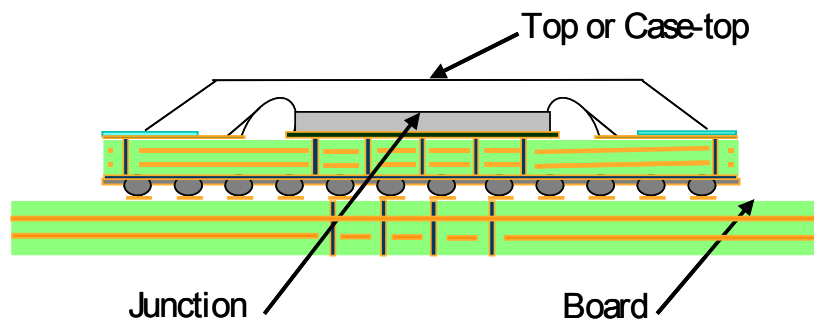


Figure 1 — Typical temperature location designations

Temperature measurement locations used to determine the thermal values are shown in Figure 1. The junction designation represents the location of the temperature sensitive device in the die used for the measurements [2]. User application dies may have an additional temperature rise from this representative junction to a hot-spot junction. The top, or case-top, and board designations are discussed in 5.2.2 and 5.2.3.