

JEDEC STANDARD

Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)

JESD51-2A

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INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR)

Foreword

This document is in the JESD51 series of specifications that specify the methods to determine and report the thermal performance of integrated circuit packages. The specification was formulated under the cognizance of the JC-15.1 Committee on Thermal Characterization Techniques for Electronic Packages and Interconnects.

Introduction

The purpose of this document is to outline the environmental conditions necessary to ensure accuracy and repeatability for a standard junction-to-ambient (θ_{JA}) thermal resistance measurement in natural convection. Without the standardized control of the environment, the test results from different vendors or from different packages will not be consistent and cannot be used to judge relative performance. The intent of θ_{JA} measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

NOTE: “Still air” (in the title) signifies natural convection in an enclosure as opposed to a natural convection measurement made in a wind tunnel with the blower off.

INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR)

(From JEDEC Board Ballot JCB-07-111, formulated under the cognizance of the JC-15.1 Committee on Thermal Characterization Techniques for Electronic Packages and Interconnects.

1 Scope

The environmental conditions described in this document will apply only to natural convection, θ_{JA} , measurements for packages mounted on standard test boards. The board will be placed in a horizontal (package up) position in an enclosure that prevents extraneous air currents and allows only natural convection generated by the package under test.

2 Normative reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

- [1] JESD51, *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Devices)*. This is the overview document for this series of specifications.
- [2] JESD51-1, *Integrated Circuit Thermal Measurement Method - Electrical Test Method*
- [3] JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- [4] JESD51-4, *Thermal Test Chip Guideline (Wire Bond Type Chip)*
- [5] JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*
- [6] JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)*
- [7] JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- [8] JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board*
- [9] JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*
- [10] JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*
- [11] JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*
- [12] JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*
- [13] JESD30D, *Descriptive Designation System for Semiconductor-device Packages*