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EIA/JEDEC STANDARD

**Standard for Description of
54/74ABTXXX and 74BCXXX
TTL-Compatibility BiCMOS Logic
Devices**

EIA/JESD54

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**ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT**



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**Standard for Description of
54/74ABTXXX and 74BCXXX
TTL-Compatible BiCMOS Logic Devices**

(From JEDEC Council ballot JCB-95-67, formulated under the cognizance of JC-40 Committee on Standardization of Digital Logic.)

CONTENTS

Section	Page
1 PURPOSE AND SCOPE	1
1.1 Purpose	1
1.2 Scope	1
2 DEFINITIONS	1
3 STANDARD SPECIFICATIONS	2
3.1 Absolute Maximum Continuous Ratings	2
3.2 Recommended Operating Conditions	2
3.3 ABT DC Specifications	3
3.4 BC DC Specifications	4
4 TEST CIRCUITS AND SWITCHING WAVEFORMS	5
5 SUPPLY CURRENT TEST PROCEDURES	12
6 ABT SWITCHING SPEED STANDARDS	13
6.1 Index of Device Types	13
6.2 Switching Speed Tables	14
7 BC SWITCHING SPEED STANDARDS	29
7.1 Index of Device Types	29
7.2 Switching Speed Tables	30

1 PURPOSE AND SCOPE

1.1 Purpose:

To provide a standard of BiCMOS Logic series specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

1.2 Scope:

This standard covers specifications for BiCMOS Logic series as defined in Section 2.

2 DEFINITIONS

BiCMOS Series

Includes devices combining bipolar and silicon-gate complementary metal-oxide-semiconductor (CMOS) field effect devices in a single-chip integrated circuit.

ABTXXXXXX Series

Includes devices whose input logic levels are TTL compatible, whose outputs are specified at TTL levels.

BCXXX Series

Includes devices whose input logic levels are TTL compatible, whose outputs are specified at TTL levels and the output sink current is specified at either 24mA or 48mA.

Prefixes

Prefixes "54" or "74" immediately preceding "ABT" or "BC" indicate the operating temperature range. For example, 54ABTXXXXXX refers to the Military (MIL) version of devices which are specified over the temperature range of -55°C to 125°C . 74BCXXX or 74ABTXXXXXX refers to the Commercial (COM'L) version of devices which are specified over the temperature range of -40°C to 85°C .

3 STANDARD SPECIFICATIONS

3.1 Absolute Maximum Continuous Ratings (Notes 1 and 2):

Supply Voltage, V_{CC}	−0.5 V to 7 V
dc input voltage, V_I (Note 3)	−0.5 V to V_{CC}
dc output voltage, V_O	−0.5 V to 5.5 V
dc input clamp current, I_{IK} ($V_I < 0$)	−18 mA
dc output clamp current, I_{OK} ($V_O < 0$)	−30 mA
dc current into any output in the low state, I_{OL} (Note 4)	$2 \times I_{OL(rated)}$
dc current into any output in the high state, I_{OH} (Note 5)	$2 \times I_{OH(rated)}$
Storage temperature range	−65°C to 150°C

Note 1: Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Note 2: Under transient conditions these ratings may be exceeded as defined elsewhere in this specification.

Note 3: The dc input voltage rating may be exceeded if the dc input clamp current ratings are observed.

Note 4: Not to exceed 70 mA.

Note 5: Not to exceed −35 mA.

3.2 Recommended Operating Conditions:

Symbol	Parameter		MIN	NOM	MAX	Unit
V _{CC}	Supply voltage		4.5	5	5.5	V
V _I	Input Voltage		0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	V
T _A	Operating free-air temperature	74 Series	−40	25	85	°C
		54 Series	−55	25	125	°C
ΔI/Δv	Input transition rise or fall rate (Note 1)		0		5	ns/V

Note 1: As measured between 0.8 V and 2 V.

3.3 ABT dc Specifications:

Symbol	Parameter	Test Conditions	54/74 Series		Unit
			MIN	MAX	
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN},$ $I_I = -18 \text{ mA}$		-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN},$ $V_I = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3 \text{ mA}$	2.4	V
			$I_{OH} = -12 \text{ mA}$	2	V
			$I_{OH} = -24 \text{ mA}, (\text{Note } 5)$	2	V
			$I_{OH} = -32 \text{ mA}, (\text{Notes } 4,5)$	2	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN},$ $V_I = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 12 \text{ mA}$	0.8	V
			$I_{OL} = 48 \text{ mA}, (\text{Note } 5)$	0.55	V
			$I_{OL} = 64 \text{ mA}, (\text{Notes } 4,5)$	0.55	V
I_I	Input current	$V_{CC} = \text{MAX},$ $V_I = V_{CC}$	except I/O ports	0.1	mA
			I/O ports	1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX},$ $V_I = 2.7 \text{ V}$		10	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX},$ $V_I = 0.5 \text{ V}$		-10	μA
I_{OZH}	Off-state output current (Note 1)	$V_{CC} = \text{MAX},$ $V_O = 2.7 \text{ V}$	except I/O ports	50	μA
			I/O ports	60	μA
I_{OZL}	Off-state output current (Note 1)	$V_{CC} = \text{MAX},$ $V_O = 0.5 \text{ V}$	except I/O ports	-50	μA
			I/O ports	-60	μA
I_{OS}	Output short-circuit current (Note 2)	$V_{CC} = \text{MAX},$ $V_O = 0$	-50		mA
I_{CCZ}	Static supply current, outputs high-impedance	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or } \text{GND}$		(Note 3)	μA
I_{CCH}	Static supply current, outputs high	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or } \text{GND}$		(Note 3)	μA
I_{CCL}	Static supply current outputs low	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or } \text{GND}$		(Note 3)	mA
ΔI_{CC}	Static supply current per input at TTL levels	$V_I = V_{CC} - 2.1 \text{ V or } V_I = 0.5 \text{ V},$ $V_{CC} = \text{MIN to MAX}$		2.5	mA

Note 1: For I/O pins, I_{OZH} and I_{OZL} include the input leakage current.

Note 2: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Note 3: Refer to manufacturer's datasheets.

Note 4: Not applicable to 54 series products.

Note 5: Not applicable to series resistor parts.

3.4 BC dc Specifications:

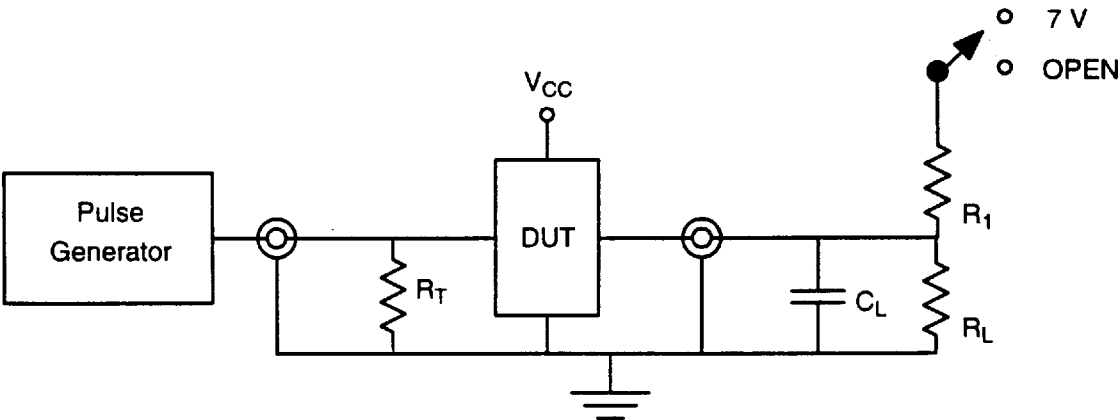
Symbol	Parameter	Test Conditions	74 Series		Unit
			MIN	MAX	
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN},$ $I_I = -18 \text{ mA}$		-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN},$ $V_I = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3 \text{ mA}$	2.4	V
			$I_{OH} = -15 \text{ mA}$	2	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN},$ $V_I = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 24 \text{ mA}$	0.55	V
			$I_{OL} = 48 \text{ mA}$	(Note 3)	V
I_I	Input current	$V_{CC} = \text{MAX},$ $V_I = V_{CC}$	except I/O ports	1	μA
			I/O ports	1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX},$ $V_I = 2.7 \text{ V}$	except I/O ports	1	μA
			I/O ports	50	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX},$ $V_I = 0.5 \text{ V}$	except I/O ports	-1	μA
			I/O ports	-50	μA
I_{OZH}	Off-state output current (Note 1)	$V_{CC} = \text{MAX},$ $V_O = 2.7 \text{ V}$		50	μA
I_{OZL}	Off-state output current (Note 2)	$V_{CC} = \text{MAX},$ $V_O = 0.5 \text{ V}$		-50	μA
I_{OS}	Output short-circuit current (Note 2)	$V_{CC} = \text{MAX},$ $V_O = 0$	-60		mA
I_{CCZ}	Static supply current, outputs high-impedance	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or GND}$		50	μA
I_{CCH}	Static supply current, outputs high	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or GND}$		50	μA
I_{CCL}	Static supply current outputs low	$V_{CC} = \text{MAX},$ $V_I = V_{CC} \text{ or GND}$		(Note 3)	mA
ΔI_{CC}	Static supply current per input at TTL levels	$V_I = V_{CC} - 2.1 \text{ V or } V_I = 0.5 \text{ V},$ $V_{CC} = \text{MIN to MAX}$		1.5	mA

Note 1: For I/O pins, I_{OZH} and I_{OZL} include the input leakage current.

Note 2: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Note 3: Refer to manufacturer's datasheets.

4 TEST CIRCUITS AND SWITCHING WAVEFORMS



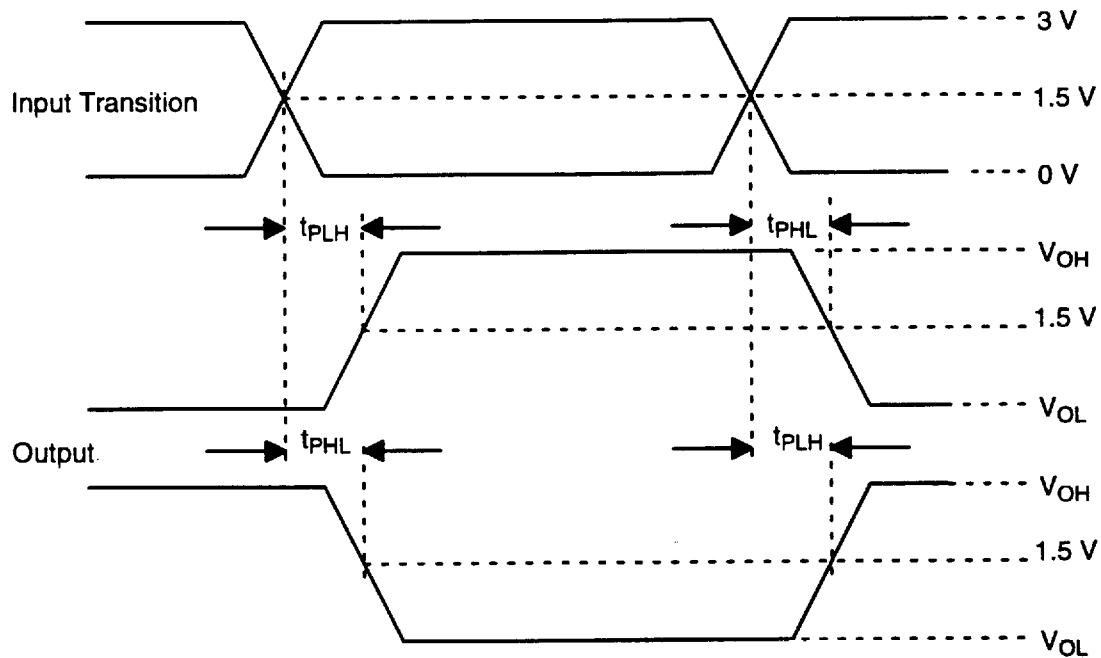
Test	Switch
t_{PLH} (except open-collector outputs)	Open
t_{PLH} (open-collector outputs)	7 V
t_{PHL} (except open-collector outputs)	Open
t_{PHL} (open-collector outputs)	7 V
t_{PZH}	Open
t_{PZL}	7 V
t_{PHZ}	Open
t_{PLZ}	7 V

C_L = 50 pF or equivalent (includes jig and probe capacitance)

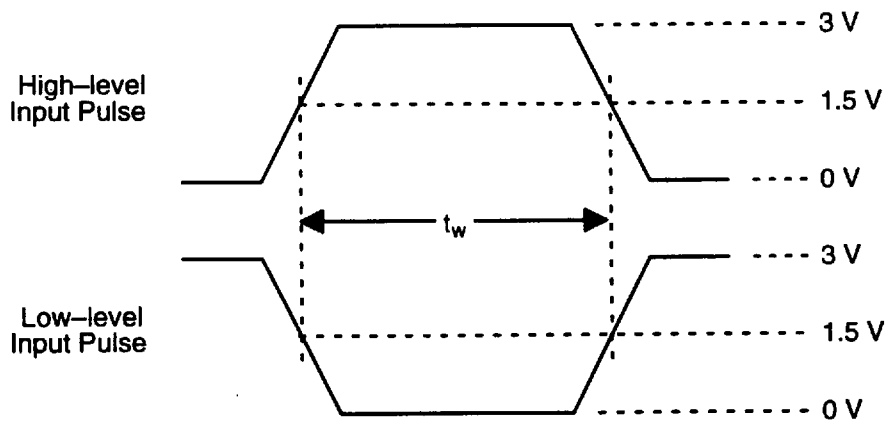
$R_L = R_1$ = 500 Ω or equivalent

R_T = Z_{OUT} of pulse generator (typically 50 Ω)

PROPAGATION DELAY MEASUREMENTS



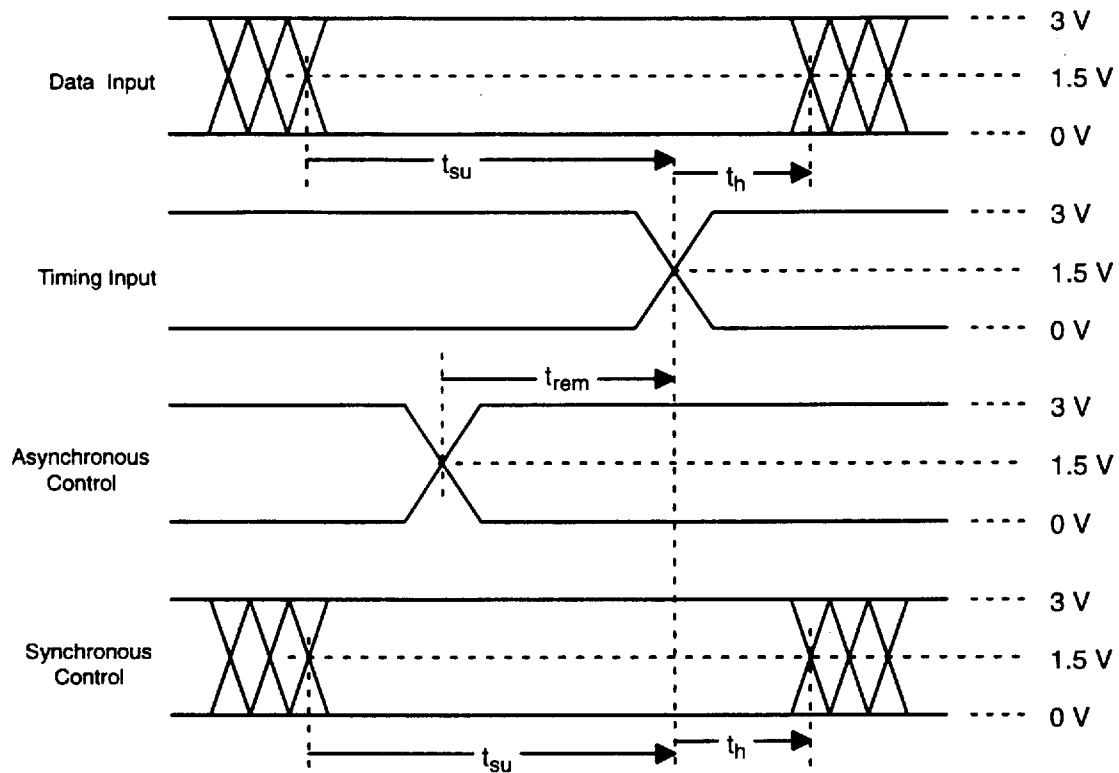
PULSE DURATION (WIDTH) MEASUREMENTS



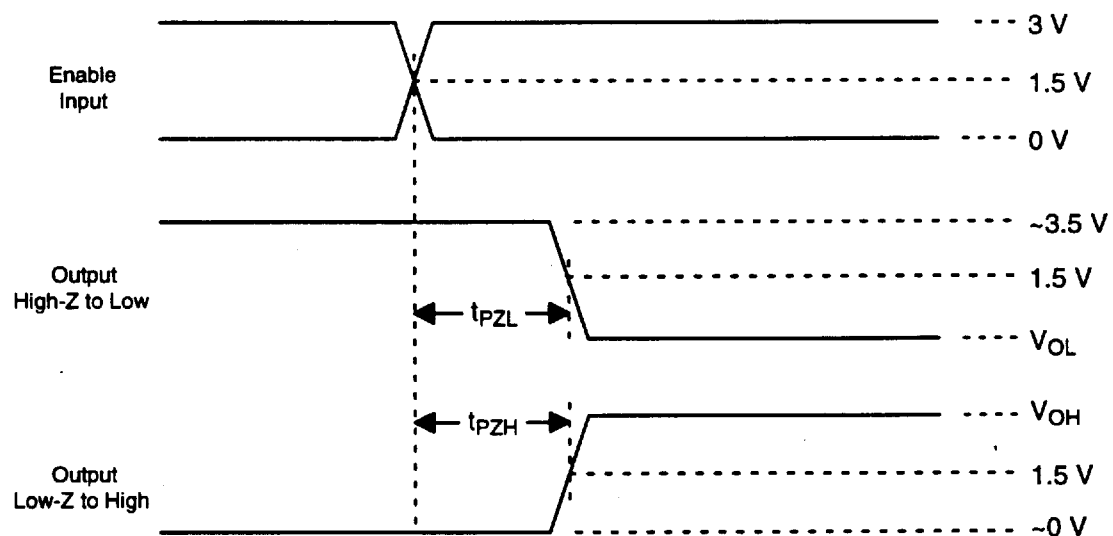
Output requirements: Device must follow truth table
 $V_{OL} \leq 0.8 \text{ V}$
 $V_{OH} \geq 2.0 \text{ V}$
 Standard output loading; $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$

Input Conditions: $t_r = t_f = 2.5 \text{ ns}$ (or as fast as required) from 10% to 90% of 0 V to 3 V.

SETUP AND HOLD TIME MEASUREMENTS



ENABLE TIME MEASUREMENTS



DISABLE TIME MEASUREMENTS

