

JEDEC STANDARD

Isothermal Electromigration Test Procedure

JESD61A.01

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE

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Foreword

The isothermal test is an accelerated electromigration test performed on microelectronic metallizations. In the isothermal test, an attempt is made to maintain a constant mean temperature of the line under test, by varying the stress current and hence the amount of Joule heating imparted to the line.

Given a known and unvarying thermal resistance of the sample to the ambient, the isothermal test uses a feedback control to maintain a constant power dissipated in the metallization under test, so that a constant test line mean temperature is achieved. When the line resistance changes during the test, due to electromigration damage, the power is kept constant, by varying the stress current.

This document presents an algorithm for conducting the isothermal test using computer-controlled instrumentation. The intent is to provide a complete description of a functional isothermal test algorithm that will allow a programmer to implement and start using an accelerated electromigration test with ease. The algorithm is derived from published and unpublished literature. Bibliographic references are listed in Annex C.

This standard was formulated under the cognizance of JC-14.2 Committee on Wafer-Level Reliability and approved by the JEDEC Board of Directors (BoD) Ballot JCB-07-20. It was prepared with the contribution of the National Research Council of Italy, Institute for Microelectronics and Microsystems (CNR-IMM) of Bologna, Italy.

The present revision JESD61A introduces significant technical changes from the previous edition (EIA/JESD61, April 1997) to make it applicable to copper as well as to aluminum metallizations. Substantive changes to the document are listed in Annex D.

Introduction

As the copper damascene technology has gained widespread use for ULSI interconnections, a renewed interest has developed in fast wafer level reliability (WLR) measurements to evaluate electromigration. The standard package level reliability (PLR) tests, used in the semiconductor industry, are very expensive when applied to copper metallizations, in comparison with aluminum-based structures, due to the considerable cost of the high temperature environmental chambers required (a typical stress temperature is 350 °C) and to the time (weeks, months) required to perform some characterizations.

Standardized WLR methods, as the Isothermal Test (JESD61) [1], [2], [3], [4], the Standard Wafer level Electromigration Accelerated Test (JEP119A) [5], and the Constant Current Test (JESD202) have been applied to the evaluation of electromigration in copper, with the aim not to substitute for PLR tests, rather to provide a less expensive tool to complement them: only a wafer prober and some relatively inexpensive measurement instruments are needed. The speed of WLR measurements is a key issue in the production line to monitor and give feedback on the quality of the metallization.

In this scenario it is fundamental to achieve the best correlation between the PLR and WLR tests [6], [7]. The isothermal test has been cited as being the most suitable method [8]: a constant and uniform temperature is assumed in the test line, close to the situation achieved in the moderately accelerated constant-current PLR tests.

Introduction (cont'd)

In fact, the assumption of a uniform temperature in the line during the isothermal test can be a poor approximation unless appropriate thermal modeling and test structure designs are used to minimize the unavoidable temperature gradients at the line ends. Hence, when meaningful correlations between PLR and WLR tests results are desired, such efforts are very important.

Moreover, it is necessary to enhance the temperature accuracy on copper structures, where temperatures as high as 600 °C can be reached during WLR tests. The present revision JESD61A introduces the recommendations for a correct temperature determination [5], [9], [10], previously incorporated in JEP119A (Procedure for SWEAT) and in JESD33B (Standard for TCR measurement).

ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE

1 Scope

This document describes a procedure for conducting the ISOthermal accelerated wafer level electromigration Test (ISOT) [1], [2], [3], [4] using computer-controlled instrumentation. This procedure is suitable for aluminum as well as for copper metallizations. There is no limitation to the use of this procedure at lower acceleration levels, down to and including the levels used for the conventional PLR electromigration test.

This document does not specify what test structure to use with this procedure. A standard describing the design features to be adopted to minimize the temperature gradients (see 7.5) in highly-accelerated WLR measurements is not presently available. However, users of this procedure report its effectiveness with both straight-lines and via-terminated test structures.

2 Normative references

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revision of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative references indicated below. For undated references, the latest edition of the normative document referred to applies.

JEDEC JESD33B, *Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line*, February 2004.

JEDEC JEP119A, *A Procedure for Performing SWEAT*, August 2003.

ASTM F 1259M-96, *Standard Guide for Design of Flat, Straight-Line Test Structures for Detecting Metallization Open-Circuit or Resistance-Increase Due to Electromigration*, Reapproved 2003.

JEDEC JESD87, *Standard Test Structures for Reliability Assessment of AlCu Metallizations with Barrier Materials*, July 2001.

JEDEC JESD37, *Standard for Lognormal Analysis of Uncensored Data, and of Singly Right-Censored Data Utilizing the Persson and Rootzen Method*, October 1992.

JEDEC JESD202, *Method for Characterizing the Electromigration Failure Time Distribution of Interconnect Under Constant-Current and Temperature Stress*, March 2006.

3 Terms and definitions

For the purposes of this standard, the following terms and definitions apply.

3.1 test structure

A passive metallization structure, including a test line, that is fabricated on a semiconductor wafer by procedures used to manufacture microelectronic integrated devices.

NOTE Connections are provided to make Kelvin-like resistance measurements of the test line, i.e., two taps for sensing voltage when two other terminals force a current through the line. Typically, these terminals are located at the ends of the test line in single-level structures, while multi-level structures have vias that connect the ends of the test line to the over- or underlying metal level in which the terminals are located (see also 7.5).

3.2 test line

A metallization line, of specified dimensions, whose length is defined by the position of the two voltage taps for single-level structures or by the position of the vias for multi-level structures, which locate the taps in a different metal level.

NOTE 1 It is assumed that the major portion of the test-line length will have a uniform cross-sectional area. This supports the assumption of approximately uniform temperature along the length. This statement holds true as long as significant voiding has not occurred. The assumption is not true at the forcing ends, where a temperature gradient will exist and should be minimized by a proper design in order that the test structure can be suitable for isothermal tests (see 7.5).

NOTE 2 The cross-sectional area of the test line may be either the mean geometrical cross-sectional area or the electrical cross-sectional area. The latter is determined by a method (see subclause 6.3.2 of JESD202, [9], [11]) based on the knowledge of the parameter $\Delta\rho/\Delta T$ for a given material, e.g., Al or Cu, where ρ is the resistivity of the pure, bulk form of the metal, and T is the temperature.

3.3 temperature coefficient of resistance [TCR(T_{ref})] $\{^{\circ}\text{C}^{-1}\}$

The fractional change in resistance of the test line per unit change in temperature at a specified temperature, T_{ref} , as described in the following equation:

$$\text{TCR}(T_{\text{ref}}) = \frac{1}{R(T_{\text{ref}})} \times \frac{\Delta R}{\Delta T} \quad (1)$$

where

$R(T_{\text{ref}})$ $\{\Omega\}$ is the resistance of the test line at the reference temperature T_{ref} $\{^{\circ}\text{C}\}$;

ΔR $\{\Omega\}$ is the change in resistance;

ΔT $\{^{\circ}\text{C}\}$ is the change in temperature that caused the change in resistance.

NOTE 1 Two choices of T_{ref} are in common use: 0 $^{\circ}\text{C}$ and ambient temperature (typically from 24 to 27 $^{\circ}\text{C}$). They are equivalent as long as self-consistent definitions are used. The choice of 0 $^{\circ}\text{C}$ is preferred, since it facilitates a first-glance comparison of interlaboratory experiments and of experiments conducted at different times in the same laboratory.

NOTE 2 For aluminum-based metallizations, the change in resistance of the test line with temperature, $\Delta R/\Delta T$, is approximately constant from room temperature to about 420 $^{\circ}\text{C}$. For copper-based metallizations, a variation in $\Delta R/\Delta T$ value becomes evident at temperatures as low as 200 $^{\circ}\text{C}$ [9], [10]. Hence, if the TCR is to be used to calculate the temperature of a copper test line at higher temperatures, a correction factor, F_{corr} , will be required (see 6.1.2).

3 Terms and definitions (cont'd)

3.4 thermal resistance (R_{th}) {°C/W}

The change in mean temperature of the test line divided by the change in power dissipation in the line, as described in the following equation:

$$R_{th} = \Delta T / \Delta P \quad (2)$$

where

ΔT {°C} is the change in mean temperature;

ΔP {W} is the change in power dissipation that caused the change in mean temperature.

NOTE 1 It is assumed that the electromigration damage, occurred during the isothermal test, does not affect the thermal resistance of the line to the first order.

NOTE 2 The thermal resistance R_{th} is defined under the assumptions of temperature uniformity along the test line and linear dependence of T versus P : in a plot of T versus P , R_{th} is the slope of the straight line. R_{th} is dependent on the geometry of the test structure and on the thermal conductance of the test line to the ambient. On the other hand, because the thermal conductance of the materials in the path of the heat flow from the test structure are temperature dependent [5], [10], the T versus P relationship is not linear, i.e., the slope of this curve will gradually decrease with increasing power dissipation. In other words, R_{th} is temperature dependent. However, over a limited range of temperatures (typically 50 °C), the T versus P relationship can still be considered linear, assuming the relationship[†]

$$T = T_0^* + R_{th}^* \times P \quad (3)$$

As a consequence, a best straight-line fit of eq. (3), using some measured (T , P) data pairs in this limited temperature range, can be used to estimate the thermal resistance value, R_{th}^* , and the thermal resistance intercept value, T_0^* (see 6.1.7, 6.2.3.3).

3.5 target stress temperature (T_{test}) {°C}

The desired mean temperature of the test line during the stress phase of the test.

3.6 error band (B_E) {°C}

A band of test-line temperatures centered on T_{test} , i.e.

$$T_{test} - B_E/2 \leq T \leq T_{test} + B_E/2 \quad (4)$$

where the isothermal algorithm will consider the test-line temperature to be equal to T_{test} , as required during the stress.

NOTE A typical value for B_E is 1 °C. However, the feedback control loop will continue to adjust the forcing current, to keep a constant target stress temperature, T_{test} , even when the test-line temperature is within the error band (see 6.3.3).

[†] Throughout this document, the quantities thermal resistance R_{th}^* and intercept T_0^* were obtained from a linear fit to eq. (3) and apply only in the limited temperature range (typically 50 °C) within which the fit was performed.

4 Symbols

For the purposes of this standard, the following symbols are used.

A	empirical constant in Black's equation (see 7.6, Annex B)
a	cross-sectional area of the test line
B_E	temperature error band (see 3.6)
D_i	fractional electromigration damage (see Annex B)
D_{st}	total electromigration damage incurred during the initial settling time (see Annex B)
$\Delta R/R\%$	percent failure criterion (see 6.3.4)
$\Delta R/R\% _{init}$	percent failure criterion during the initialization phase (see 6.1.6)
$\Delta R/R\% _{step}$	percent failure criterion during staircase/convergence phase (see 6.2.4)
E_a	activation energy in Black's equation (see 7.6, Annex B)
$F_{corr}, F_{corr, inv}$	correction factors for TCR application at high temperatures (see 6.1.2)
$f_{current}$	initial current multiplication factor (see 6.1.3)
f_{power}	convergence power reduction factor (see 6.2.1, 0)
I	forcing current through the test line
I_G	range of the current generator (see 6.2.2)
$I_{test,1}$	stress current at convergence (see 6.3.1)
I_1	initial forcing current in the test line (see 6.1.3)
i (subscript)	index in temperature control loops
J	current density in the test line
J_{test}	stress current density (see 6.3.1)
$J_{test, av}$	average stress current density in a sample population (see 7.6)
k	Boltzmann's constant
$N_{conv}, N_{staircase}$	number of temperature steps in convergence, staircase phases (see 6.2.3, Annex A)
n (subscript)	index in temperature control loops
n	current density exponent in Black's equation (see 7.6, Annex B)
P	power dissipated across the voltage taps of the test line
P_{test}	power at target stress temperature (see 6.3.1)
R	resistance of the test line
R_{end}	resistance value after the isothermal test
R_{fail}	failure resistance value (see 6.3.4)
$R_{fail, init}$	failure resistance value during the initialization phase (see 6.1.6)
$R_{fail, step}$	failure resistance value during the staircase/convergence phase (see 6.2.4)
$R_{test,1}$	resistance value at convergence
R_{th}	thermal resistance of the test line (see 3.4)
R_{th}^*	R_{th} value, estimated over a limited temperature range (see 3.4, 6.1.7, 6.2.3.3)

4 Symbols (cont'd)

$R_{th, test}^*$	R_{th} value at convergence (see 6.3.1)
ρ	resistivity of the bulk pure form of the test-line metal
T	mean temperature of the test line
T_{cal}	test-line temperature estimated by TCR, without correction (see 6.1.2)
T_{chuck}	chuck (or ambient) temperature (see 7.1)
T_{conv}	starting convergence temperature value (see Annex A)
TCR	Temperature Coefficient of Resistance (see 3.3)
T_{ref}	reference temperature for TCR (see 3.3)
$T_{staircase}$	staircase temperature limit (see 6.2.1)
T_{test}	target stress temperature (see 3.5, 6.3.1, 7.6)
TTF	Time-To-Failure
TTF_{corr}	TTF value corrected to account for the initial EM damage (see 6.4.1, Annex B)
TTF_{norm}	TTF value normalized versus the average stress current density $J_{test,av}$ (see 7.6)
T_0^*	R_{th} intercept value, estimated over a limited temperature range (see 3.4, 6.1.7, 6.2.3.3)
$T_{0, test}^*$	R_{th} intercept value at convergence (see 6.3.1)
t	elapsed time for isothermal test after I_1 is applied (see 6.1.3)
t_{corr}	Time-To-Failure correction time (see 6.4.1, Annex B)
t_{log}	time interval for data logging during the stress phase (see 6.4.4)
t_{st}	initial settling time (see 6.4.1, Annex B)
t_{50}	median time-to-failure calculated by Black's equation (see 7.6)
V_C	voltage range of voltmeter and compliance of the current generator (see 6.1.5, 6.2.2)
V_{meas}	voltage measured across the voltage taps of the test line (see 6.1.4, 6.2.3, 6.3.3)

NOTE Throughout this document, the bar over symbols will indicate the predicted values when should be distinguished from the measured values (indicated by symbols without bar).

5 Technical requirements

5.1 Equipment requirements

- a) A programmable current source capable of supplying sufficient current to attain the required current densities in the metallization test line. Typically, a current density of 1×10^8 A/cm² is sufficient. The voltage compliance of the current source shall be sufficient to allow stressing test lines in the resistance range of interest (typically a few Ω to several k Ω). Minimum forcing current resolution of 12 bits, or 3½ digits, is recommended. The current source settling time (i.e. the time required to deliver 99% of the target current) shall be no greater than 10 ms.
- b) A digital voltmeter capable of measuring the expected voltages. Three or more full scale ranges may be required (e.g. 1, 10 & 100 V). Minimum measurement resolution of 12 bits, or 3½ digits, is required. Voltmeter conversion time shall be no greater than 10 ms (for additional considerations on voltmeter integration time and input filter see 7.3 and 7.4).
- c) A computer acting as a controller. The computer provides a feedback control system. It controls the input current to the metallization under test based on discrete time measurements provided by the voltmeter and computations supervised by the isothermal test algorithm.

The data acquisition time for the feedback control shall be no shorter than the sum of the settling time of the current source and the reading rate of the voltmeter. However, a control cycle time shorter than 50 ms is not recommended (see 7.4 for additional comments).

Time-to-failure (TTF) targets can range from tens of seconds to tens of thousands of seconds. The system should be capable of executing one control cycle with a period short enough to provide a resolution of at least 1% of the TTF.

5.2 Test configuration

Due to the required accuracy for the resistance measurements, a four-wire Kelvin connection to the structure is required. Depending on the test line and stress conditions, a relatively high current may need to be applied. The current-forcing connections to the test structure must be able to sustain this current.

6 The isothermal test algorithm

The isothermal test [1], [2], [3], [4] uses a feedback control loop to adjust the stress current applied to the metallization such that the mean temperature of the test line is maintained within a programmed error band B_E centered around the target stress temperature T_{test} .

The ISOT algorithm is based on a very simple thermal model for the structure. The model assumes linear heat flow from the structure in one dimension based on uniform power dissipation along the length of the structure. It does not consider thermal conduction through the ends to the pads, or temperature gradients in the test line (see 7.5). It is assumed also that the change in resistance of the test line due to electromigration damage does not, to a first-order approximation, affect its thermal resistance. The Temperature Coefficient of Resistance of the test line (see 3.3) must have been determined prior to the test.

The test procedure consists of five main phases, which are briefly described below and in greater detail in 6.1 to 6.4. Figure 1 illustrates how the temperature of the test line increases with time during the first three phases, called the **initial settling time**, t_{st} , followed by the beginning of the stress phase at constant temperature.

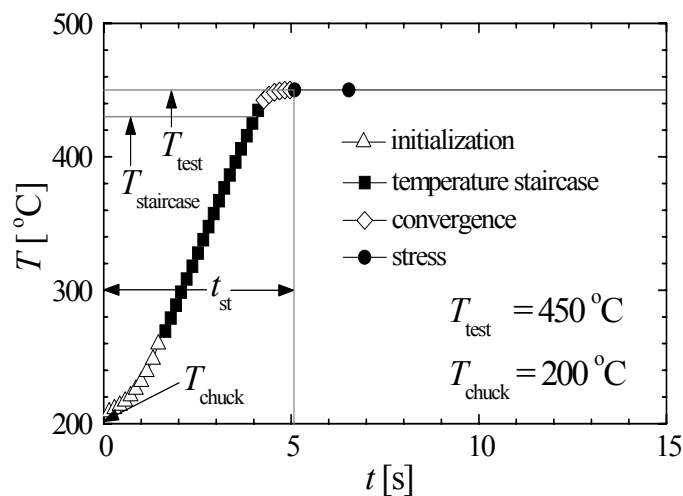


Figure 1 – Measurement phases of the isothermal test

- Initialization phase** (see 6.1): Measure the resistance of the test line at the chuck temperature, T_{chuck} , before the test structure is subjected to Joule heating. Apply a suitable current through the test line and, then, measure the resistance as the current is step-wise increased to elevate the test line temperature to 50°C greater than T_{chuck} . Calculate the initial value for the thermal resistance from the test line temperature data, obtained by the measured resistance data and the TCR, versus applied power data. The time that the current is first applied is the starting time for the isothermal test.
- Temperature staircase phase** (see 6.2): Step-wise increase the temperature of the line due to Joule heating, by increasing the applied current. The procedure relies on the balanced use of the TCR, to correlate temperature and resistance of the line, and of the thermal resistance, to estimate the needed current increment. To account for the non-linearity in the temperature versus power relationship, the thermal resistance is recalculated at each temperature step.