

JEDEC STANDARD

Definition of Skew Specifications for Standard Logic Devices

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DEFINITIONS OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES

(From JEDEC Board Ballots JCB-02-67, JCB-02-112, JCB-02-113, and JCB-02-114, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines skew specifications and skew testing for standard logic devices.

The purpose is to provide a standard for specifications to achieve uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

2 Terms and definitions

These definitions are provided for the purpose of this document. For general definitions of skew time, see the latest revision of JEDEC Standard No. 99 *Terms, Definitions, and Letter Symbols for Microelectronic Devices*.

2.1 Device terms and definitions

PLL device: A logic device that includes a phase-locked loop and may also include other logic functions, such as counters, registers, and buffers.

2.2 Parameter terms and definitions

skew (time): The magnitude of the time difference between two events that ideally would occur simultaneously.

controlled edge: The output signal edge that is locked to the PLL trigger reference.

jitter: The time deviation of a PLL-generated controlled edge from its nominal position.

threshold crossing: The point at which a logic signal transitions from one logic state to another.

primary threshold crossing: The threshold crossing of a clock signal indicating the start of a new cycle and the end of the previous cycle.

secondary threshold crossing: The threshold crossing of a clock signal indicating the second part of the clock cycle.

3 Standard specifications

All skew parameters are specified over the guaranteed temperature and supply operating ranges. If more than one temperature or supply operating range is used, the range(s) for the skew specification(s) must be identified. PLL logic devices must be supplied with a stable input reference clock within the operating frequency range of the component.

Table 1 — Symbols for skew and other specifications

Symbol	Parameter	Units	Notes
$t_{sk(o)}$	output skew	ps, ns	1
$t_{sk(LH)}$	output skew for low-to-high transitions	ps, ns	
$t_{sk(HL)}$	output skew for high-to-low transitions	ps, ns	
$t_{sk(pr)}$	process skew	ps, ns	
$t_{sk(pp)}$	part-to-part skew	ps, ns	
$t_{sk(b)}$	bank skew	ps, ns	1
$t_{sk(p)}$	pulse skew	ps, ns	
$t_{sk(inv)}$	inverting skew	ps, ns	1, 4
$t_{sk(\omega)}$	multiple-frequency skew	ps, ns	
$t_{(\phi)}$	static phase offset	ps, ns	
$t_{(\phi)dyn}$	dynamic phase offset	ps, ns	
$t_{(\phi)tot}$	total phase offset	ps, ns	
$t_{jit(cc)}$	cycle-to-cycle period jitter	ps, ns	2, 5
$t_{jit(per)}$	period jitter	ps, ns	2, 5
$t_{jit(hper)}$	half-period jitter	ps, ns	
$t_{jit(duty)}$	duty cycle jitter	ps, ns	
$t_{jit(\phi)}$	phase jitter	ps, ns	1, 3, 5
lock (f)	frequency locked		
lock (ϕ)	phase locked		
t_L	power-up PLL lock time	ns, ms	
$t_{L(\omega)}$	PLL lock time after frequency change	ns, ms	
$t_{recL(\phi)}$	PLL recovery after phase change	ns, ms	
n_L	cycles to acquire PLL lock	cycles	
ODC	PLL output duty cycle	%	

NOTE 1 This parameter is not production tested.

NOTE 2 The sample size shall be greater than or equal to 1000.

NOTE 3 The sample size shall be greater than or equal to 2000.

NOTE 4 The test load for this parameter may be a nonstandard load identified in the data sheet.

Table 2 — Example of suggested jitter specifications

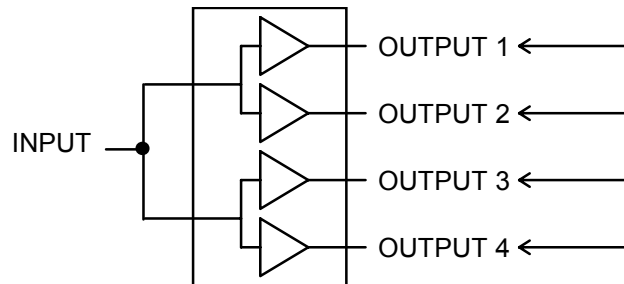
Symbol	Parameter	Sample size	Typ	Max	Unit	Notes
$t_{jit(cc)}$	cycle-to-cycle period jitter	1,000 cycles	x	x	ps	5, 6
$t_{jit(per)}$	period jitter	10,000 cycles	x	x	ps	5, 6
$t_{jit(\phi)}$	phase jitter	2,000 cycles	x	x	ps	5, 6

NOTE 5 Test Loads and Conditions are shown in Clause 4 “Standard test circuits for skew testing” for the designated voltage range.

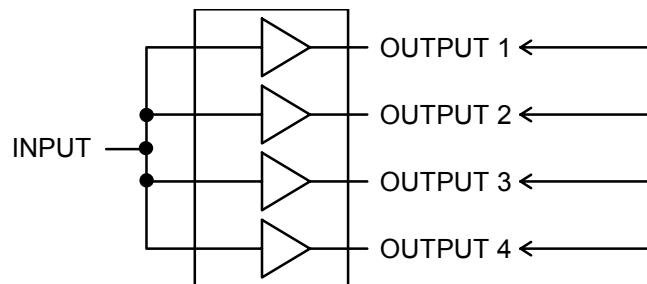
NOTE 6 Operating frequency range is 10 MHz to 100 MHz.

3 Standard specifications (cont'd)

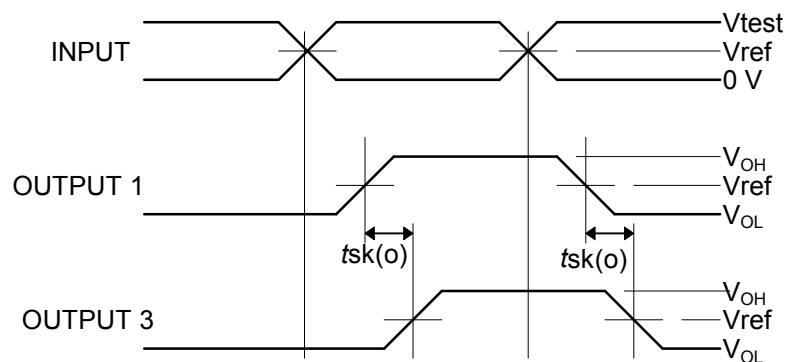
output skew ($t_{sk(o)}$): The skew between specified outputs of a single logic device with all driving inputs switching simultaneously and the outputs driving identical specified loads.



An example of a multiple bank logic device



An example of a logic device without banks



An example of output waveforms