

JEDEC STANDARD

Early Life Failure Rate Calculation Procedure for Semiconductor Components

JESD74A

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR SEMICONDUCTOR COMPONENTS

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EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR SEMICONDUCTOR COMPONENTS

Introduction

Early life failure rate (ELFR) measurement of a product is typically performed during product qualifications or as part of ongoing product reliability monitoring activities. These tests measure reliability performance over the product's first several months in the field. It is therefore important to establish a methodology that will accurately project early life failure rate to actual customer use conditions.

EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR SEMICONDUCTOR COMPONENTS

(From JEDEC Board Ballot JCB-07-03, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and monitoring.)

1 Scope

This standard defines methods for calculating the early life failure rate of a product, using accelerated testing, whose failure rate is constant or decreasing over time. For technologies where there is adequate field failure data, alternative methods may be used to establish the early life failure rate.

The purpose of this standard is to define a procedure for performing measurement and calculation of early life failure rates. Projections can be used to compare reliability performance with objectives, provide line feedback, support service cost estimates, and set product test and screen strategies to ensure that the ELFR meets customers' requirements.

2 Reference documents

JESD22-A108, *Temperature, Bias, and Operating Life*

JESD659, *Failure-Mechanism-Driven Reliability Monitoring*

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*

JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices*

JESD91, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms.*

JESD85, *Methods for Calculating Failure Rate in Units of FIT*

JESD94, *Application Specific Qualification Using Knowledge Based Test Methodology*

JEP143, *Solid State Reliability Assessment Qualification Methodologies*

JEP148, *Reliability Qualification of Semiconductor Devices Based on Physics of Failure Risk and Opportunity Assessment*

3 Terms and definitions

accelerated ELF test time (t_A): The duration of the accelerated ELF test.

acceleration factor (A): For a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition.

acceleration factor, temperature (A_T): The acceleration factor due to changes in temperature.

acceleration factor, voltage (A_V): The acceleration factor due to changes in voltage.

apparent activation energy (E_{aa}): An equivalent energy value that can be inserted in the Arrhenius equation to calculate an acceleration factor applicable to changes with temperature of time-to-failure distributions.

NOTE 1 An apparent activation energy is often associated with a specific failure mechanism and time-to-failure distribution for calculating the acceleration factor.

NOTE 2 A composite apparent activation energy is often used to calculate a single acceleration factor, for a given time-to-failure distribution, that is equivalent to the net effect of the various thermal acceleration factors associated with multiple failure mechanisms.

NOTE 3 Various physical thermal activation energies may contribute to the shape of the time-to-failure distribution.

NOTE 4 The term "apparent" is used because E_{aa} is analogous in use to E_a in the Arrhenius equation; E_{aa} is used for a time-to-failure distribution, while E_a applies to a chemical thermal reaction rate.

bathtub curve: A plot of failure rate versus time or cycles that exhibits three phases of life: infant mortality (initially decreasing failure rate), intrinsic or useful life (relatively constant failure rate), and wear-out (increasing failure rate).

characteristic life (for the Weibull distribution)(η): The time at which $F(t)$ equals $(1-e^{-1})$ ($\approx 63.2\%$)

countable failure: A failure due to an inherent defect in the semiconductor component during early-life-failure (ELF) stress tests.

NOTE Failures due to electrical overstress (EOS), electrostatic discharge (ESD), mechanical damage, etc., are not counted, but the units are considered to have completed testing through the last successful readout when computing device hours.

cumulative distribution function of the time-to-failure; cumulative mortality function [$F(t)$]: The probability that a device will have failed by a specified time t_1 or the fraction of units that have failed by that time.

NOTE 1 The value of this function is given by the integral of $f(t)$ from 0 to t_1 .

NOTE 2 This function is generally expressed in percent (%) or in parts per million (ppm) for a defined early-life failure period.

NOTE 3 The abbreviation CDF is often used; however, the symbol $F(t)$ is preferred.

3 Terms and definitions (cont'd)

cumulative fraction failing (CFF): The total fraction failing based on the starting sample size over a given time interval.

NOTE This is generally expressed in percent (%) or in ppm.

early life: The customer initial use period.

NOTE This period typically ranges from three months to one year of operation.

early-life-failure (ELF) test: An accelerated test designed to measure the early life failure rate (ELFR), which may be experienced during the customer initial use period.

NOTE The test process is specified in JESD47.

early life period (t_{ELF}): The specified early life period as defined by the user or the supplier.

failure rate (λ): The fraction of a population that fails within a specified interval, divided by that interval.

NOTE The statistical upper limit estimate of the failure rate is usually calculated using the chi-squared function.

failures in time (FIT): The number of failures per 10^9 device-hours.

population failure distributions: The applicable mortality functions.

NOTE Typically used failure distributions for early-life failures include the Weibull and Poisson (exponential); for useful life and wear-out and also the Gaussian (normal) and lognormal distributions are used.

ppm: Parts per million.

ppm/time period: The number of failures per million units in the time period of interest.

qualification family: Products sharing the same semiconductor process technology.

signature analysis: The process of assigning the most likely failure mechanism to a countable failure based on its unique electrical failure characteristics and an established physical analysis database for that mechanism.

use condition time (t_U): The time interval equivalent to the ELF test duration, as determined by the product of the acceleration factor and the actual accelerated test time: $A \times t_A$.

4 General requirements

4.1 Test samples

ELFR testing requires, as specified in JESD47D's Table 1 and Table A, a statistically significant sample size at a minimum 60% confidence to measure the ELFR associated with the component. The sample shall be drawn from a minimum of 3 nonconsecutive production lots, and shall be comprised of representative samples from the same qualification family. Samples from any single lot should not exceed 40% of the total sample required. All samples shall be fabricated and assembled in the same production site and with the same production process. The test vehicle should represent the highest design density available for qualification. Lower sample sizes may be used with justification (e.g., high component costs, limited supply).

ELFR is required to show the process capability of each technology, process, or product family. These data are generic in nature and are generally accumulated through an internal reliability monitor program. For a new device qualification that is the first of its kind in the technology, process, or product family, it may take up to one year post-qualification to accumulate adequate statistical sampling to fulfill this requirement.

4.2 Test conditions

Test samples shall be placed under stress as per applicable JEDEC test methods, e.g., JEDEC Standard JESD22-A108. Stress tests will be conducted at a voltage level, frequency, temperature, humidity, and other parameters as recommended in the JEDEC test methods. Alternative stress conditions that yield equivalent results may be used if empirically justified.

4.3 Test duration

Stress test conditions shall be continuously applied for a time sufficient to represent customer's early life period. The minimum duration will be dictated by the acceleration for the expected or established prevailing defect mix. Common practice stress durations are between 48 and 168 hours. Test durations outside the stipulated range may be used with empirical model justification. Determination of failure times prior to the termination of stress can be useful; either continuous monitoring via in situ testing or interim test readouts that can help bound failure times prior to the end of stress. The time of failure is the earliest readout at which a device fails one or more electrical tests per the datasheet specification.

4.4 Failure analysis

It is recommended that failures will be electrically and physically analyzed to root cause. Signature analysis may be applied.

5 Calculating ELFR

A typical time distribution for semiconductor component failures is depicted by the “bathtub” curve in Figure 5.1. The curve has three distinct regions: a rapidly decreasing “infant mortality” portion; a stable, useful life portion where the failure rate continues to decrease or is essentially constant; and a period of increasing failure rate representing the onset of wear-out. Infant mortality and useful life failures are caused by defects introduced during the manufacturing process. Many of these component defects can be removed by effective reliability screens. Early life fails are defect-induced component failures during board or system assembly processes, or during initial customer use.

Reliability models used for ELFR calculations must be established prior to ELFR testing, and must accurately reflect the technology, process, and fabrication and assembly site being measured, including test and screen practices. They must also be statistically updated with any major change in process, tests, or screens. JESD47 provides guidelines for process change qualification of a component.

Product ELFR data typically includes several different failure mechanisms which may contribute failures differently as a function of voltage, temperature and time. It is important to apply the correct voltage and temperature acceleration factors for each individual failure mechanism when projecting reliability performance to actual use conditions. This can be critical when the failure mix includes mechanisms with relatively low acceleration.

A detailed description of how to establish the underlying failure distribution is outside the scope of this standard. The methods described in this document apply to devices which are both sampled and produced without the use of an accelerated stress pre-conditioning, such as burn-in. Devices which are screened in production using accelerated stress methodologies typically require a more complex analysis, e.g., conditional probability, to account for the truncation of the screened portion of the distribution.

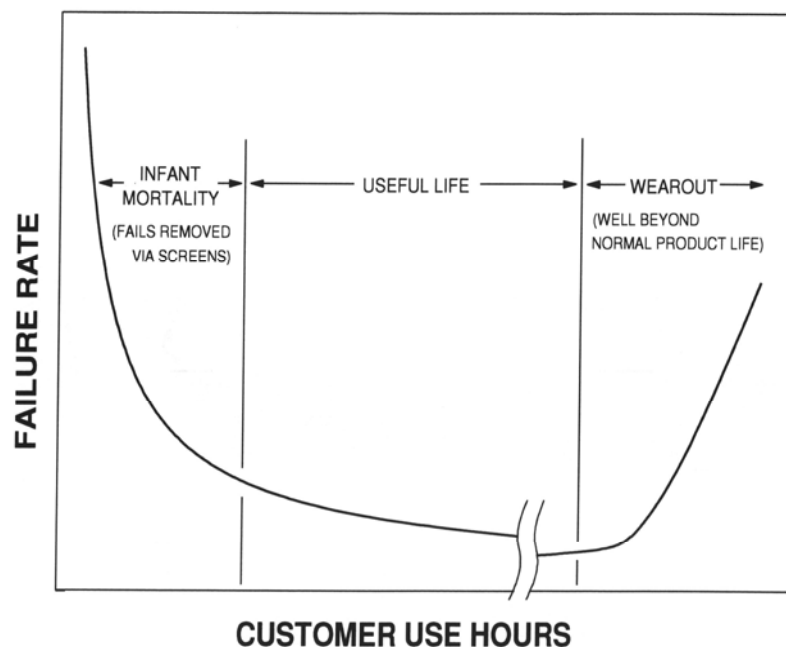


Figure 5.1 — Reliability bathtub curve

5 Calculating ELFR (cont'd)

A method for developing and validating composite temperature and voltage acceleration factors might begin by conducting extended accelerated stress testing of a separate group of samples at a minimum of two different temperatures at the same voltage and a minimum of two different voltages at the same temperature. Testing at a minimum of three temperatures and three voltages is preferred. All failures must be analyzed to root cause and then separated by failure mechanism, noting the unique voltage and temperature behavior of each mechanism. Samples without accelerated stress screening may be used to provide a more comprehensive coverage of product failure mechanisms and allow for better modeling. JESD91 and JEP122 provide method for developing acceleration failure mechanism models for semiconductor devices.

Acceleration models

Temperature Acceleration

Temperature acceleration of semiconductor failure mechanisms is usually described by the Arrhenius equation:

$$A_T = \exp [(E_{aa}/k) \times (1/T_U - 1/T_A)] \quad [1]$$

where

A_T = Temperature acceleration factor

E_{aa} = Apparent activation energy in electron volts (eV)

k = Boltzmann's constant (8.617×10^{-5} electron volts/°Kelvin)

T_U = Junction temperature at normal use conditions in degrees Kelvin

T_A = Junction temperature at accelerated conditions in degrees Kelvin

Voltage Acceleration

Unless an experimentally validated voltage acceleration model has been derived, the following model is recommended:

$$A_V = \exp [(K/X) \times (V_A - V_U)] = \exp [\gamma_V \times (V_A - V_U)] \quad [2]$$

where

A_V = voltage acceleration factor

K = Experimentally determined electric field constant (expressed in thickness per volt)

X = Thickness of stressed dielectric

$\gamma_V = (K/X)$ (units are V^{-1})

V_A = Stress voltage in accelerated ELF test

V_U = Use voltage

The total acceleration factor commonly is equivalent to the product of voltage acceleration and temperature acceleration factors,

$$A = A_T \times A_V \quad [3]$$

where

A = acceleration factor for the ELF test.

The equivalent actual use condition period is calculated as:

$$t_U = A \times t_A \quad [4]$$

where

t_U = use condition time in hours

t_A = accelerated ELF test time in hours