

JEDEC STANDARD

IC Latch-Up Test

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IC LATCH-UP TEST

(From JEDEC Board Ballots JCB-16-08, formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This standard covers the I-test and V_{supply} overvoltage latch-up testing of integrated circuits.

The purpose of this standard is to establish a method for determining IC latch-up characteristics and to define latch-up detection criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up. This test method is applicable to NMOS, CMOS, bipolar, and all variations and combinations of these technologies.

NOTE As these technologies have evolved, it has been necessary to adjust this document to the realities of characterization with limits not imagined when the first latch-up document was generated some 25 years ago. Though it would be simpler to make the original limits of 1.5 times the maximum pin operating voltage an absolute level of goodness, the possibilities of success at this level are limited by the very low voltage technologies, and the medium and high voltage CMOS, BiCMOS and Bipolar technologies (>12 V). The concept of maximum stress voltage (MSV) allows the supplier to characterize latch-up in a way that differentiates between latch-up and EOS. This revision will make it more transparent to the end user that given the limits of certain technologies the subsequent latch-up characterizations are valid.

1.1 Classification

There are two classes for latch-up testing.

- Class I is for testing at room temperature ambient.
- Class II is for testing at the maximum operating ambient temperature (T_a) or maximum operating case temperature (T_c) or maximum operating junction temperature (T_j) in the data sheet.

For Class II testing at the maximum operating T_a or T_c , the ambient temperature or case temperature (T_c) shall be established at the required test value. For Class II testing at the maximum operating T_j , the ambient temperature T_a or the case temperature T_c should be selected to achieve a temperature characteristic of the junction temperature for a given device operating mode(s) during latch-up testing. The maximum operating ambient or case temperature during stress may be calculated based on the methods detailed in Annex B. The values used in Class II testing shall be recorded in the final report.

NOTE Elevated temperature will reduce latch-up resistance, and class II testing is recommended for devices that are required to operate at elevated temperature.

1.2 Latch-up immunity characterization

Product latch-up immunity is characterized by an I/O current injection value and V_{supply} overvoltage value that does not result in a latch-up as defined in this test method. Refer to Table 1 for the recommended range of current and voltage stress, and Table 2 footnotes b, c, and d for the clamping conditions. The actual achieved force current or voltage levels may be reported as mentioned in Annex C.

Table 1 — Latch-up immunity levels

Immunity Level	Test	Magnitude of Trigger Force Current or Voltage
A	Positive I-Test	$\geq 100 \text{ mA}^a$
	Negative I-Test	$\geq 100 \text{ mA}^a$
	Overtvoltage Test	$1.5 \times V_{DD}$ or MSV, whichever is less ^b
B	If immunity level A cannot be achieved	

^a The actual injected current may be less than 100mA if pin voltage clamping limits are reached (See Table 2). If Latch-up does not occur in such a condition, then this constitutes a passing test with Immunity Level A. Otherwise, it is classified with Immunity Level B.

^b The actual applied voltage may be less than $1.5 \times V_{DD}$ or MSV if V_{supply} current clamping limits are reached (See Table 2). If Latch-up does not occur in such a condition, then this constitutes a passing test with Immunity Level A. Otherwise, it is classified with Immunity Level B.

2 Terms and definitions

The following terms and definitions apply to this test method.

cool-down time: The period of time between successive applications of trigger pulses, or the period of time between the removal of the V_{supply} voltage and the application of the next trigger pulse. (See Figure 2, Figure 3, Figure 6, and Table 3.)

DUT: The device under test.

dynamic devices: Devices requiring clocking in order to guarantee a stable state while being tested.

GND (Ground): The common or zero-potential pin(s) of the DUT.

NOTE 1 Ground pins are not latch-up tested. NOTE 2 A ground pin is sometimes called V_{ss} .

input pins: All address, data-in control, V_{ref} , and similar pins.

I/O (bidirectional) pins: Device pins that can be made to operate as an input or an output or in a high-impedance state.

2 Terms and definitions (cont'd)

I_{supply}: The total supply current in each V_{supply} pin (or pin group) with the DUT biased as indicated in Table 2.

I-test: A latch-up test that supplies positive and negative current pulses to the pin under test.

latch-up: A state in which a low-impedance path, resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition.

NOTE 1 The overstress can be a voltage or current surge, an excessive rate of change of current or voltage, or any other abnormal condition that causes the parasitic thyristor structure to become regenerative.

NOTE 2 Latch-up will not damage the device provided that the current through the low-impedance path is sufficiently limited in magnitude or duration.

logic-high: A level within the more positive (less negative) of the two ranges of logic levels chosen to represent the logic states.

NOTE 1 For digital devices, the maximum value of the high logic level voltage is used for latch-up testing. The maximum logic high level is designated as V_{max} .

NOTE 2 For non-digital devices, the maximum operating voltage that can be applied to that pin as defined in the device specification is used for latch-up testing.

logic-low: A level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states.

NOTE 1 For digital devices, the minimum value of the low logic level voltage is used for latch-up testing. The minimum logic low level is designated as V_{min} .

NOTE 2 For non-digital devices, the minimum operating voltage that can be applied to that pin as defined in the device specification is used for latch-up testing.

maximum V_{supply} ; maximum operating voltage: The maximum supply voltage at which a device is specified to operate in compliance with the applicable device specification.

NOTE 1 “Maximum” refers to the magnitude of supply voltage and can be either positive or negative.

NOTE 2 The maximum voltage is *not the absolute maximum rated voltage, i.e., the voltage beyond which permanent damage is likely.*

2 Terms and definitions (cont'd)

maximum stress voltage (MSV): The maximum voltage allowed to be placed on any given pin during latch-up immunity testing without causing irreversible damage to the device from a catastrophic breakdown of the silicon device or circuit not related to latch-up.

NOTE 1 A positive MSV is higher than the maximum operating voltage and a negative MSV is lower than the minimum operating voltage.

NOTE 2 MSV is NOT the same as the absolute maximum voltage rating (AMR) from the device data sheet. MSV applies to latch-up testing only, protecting the DUT from physical damage from stress mechanisms not directly related to latch-up. An example of an unrelated stress is one exceeding the destructive breakdown voltage of a pin resulting in non-latch-up induced catastrophic breakdown of the silicon device / circuit. MSV may be different for each pin and each polarity during testing, depending on process technology and circuit topology. In many medium and high voltage designs (>12 V), MSV may be nearly the same value as AMR. Further, the MSV value depends on the pulse width used during latch-up testing. Shorter pulse widths may allow a higher value for MSV. Therefore, the MSV value chosen should take into account the pulse width as well as process technology and circuit topology.

“no connect” pin: A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device.

NOTE All “no connect” pins shall be left in an open (floating) state during latch-up testing.

nominal I_{supply} (I_{nom}): The measured dc supply current for each V_{supply} pin (or pin group) with the DUT biased at the test temperature as defined in clause 4 and Table 2.

output pin: A device pin that generates a signal or voltage level as a normal function during the normal operation of the device.

NOTE Output pins, though left in an open (floating) state during testing of other pin types, are latch-up tested.

power supply: A component in the test system that supplies voltage and current to the DUT.

preconditioned pin: A device pin that has been placed in a defined state or condition (input, output, high impedance, etc.) by applying control vectors to the DUT.

test condition: The test temperature, supply voltage, current limits, voltage limits, clock frequency, input bias voltages, and preconditioning vectors applied to the DUT during the latch-up test.

timing-related input pin: A pin such as clock crystal oscillator, charge pump circuit, etc., required to place the DUT in a normal operating mode.

NOTE Required timing signals may be applied by the latch-up tester, external equipment, and/or external components as appropriate.

trigger pulse: The positive or negative current pulse (I -Test) or voltage pulse (V_{supply} overvoltage test) applied to any pin under test in an attempt to induce latch-up (see Figure 2, Figure 3 and Figure 6).