

JEDEC STANDARD

IC Latch-Up Test

JESD78F.02

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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IC LATCH-UP TEST

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Foreword

For almost three decades, characterization of the latch-up sensitivity as per JEDEC's JESD78 specification, or its predecessor JESD17, has been an industry accepted qualification test for integrated circuits (ICs) and semiconductor devices. Meeting a certain level of latch-up immunity in its application, as based on JESD78 specifications, is expected to minimize No Trouble Found (NTF) and Electrically Induced Physical Damage (EIPD) failures due to latch-up. JESD78F was essentially an entire rewrite of the earlier version, JESD78E. Since that standard was published in January 2022, there have been two minor updates; JESD78F.01, and this revision, JESD78F.02.

Latch-up is a state in which voltage and current outside of normal conditions triggers a high current, low impedance state not related to normal functionality, which does not end without removing power from the system. Latch-up may or may not cause physical damage. JESD78 tests for latch-up sensitive structures with two test types, overvoltage on supply pins and current injection into signal pins. Current injection is achieved either by current forcing with voltage compliance limit (I-Test) or by applying voltage with current compliance limit (E-Test).

As device technologies have evolved, products have become increasingly complex in design and varied in functionality. Therefore, it has become desirable to periodically revise this specification to meet the realities of device complexity and improve on the characterization methods. An example of such an adjustment is the introduction of the concept of the maximum stress voltage (MSV) in Revision D, allowing one to characterize latch-up in a way that differentiates EIPD between latch-up and non-latch-up damage. The MSV concept has been enhanced in this version with examples on determining MSV in Annex E. MSV is just one example of the modifications to this standard that will ensure successful performance of latch-up characterization.

Latch-up testing has become an increasingly complex task, often requiring experienced engineering assessment and support. Some of the problems with the previous specification arose with the increasing complexity of today's ICs. Many of today's complex devices have individual pins that cannot be characterized unambiguously as either inputs, outputs, or supply pins. Several pin types require special consideration to determine whether they require a voltage test or a current injection test. Furthermore, some pin types require unique pre-configuration or special data assessment methods to properly perform latch-up testing. JESD78E gives only minimal guidance to determine the pin category.

Discussions with industry experts have highlighted the need for major revisions and additions to JESD78E. The JESD78 working group, working on the next revision of the specification, decided that the shortcomings required a re-write of the document. JESD78F introduced some major changes. One of these is the extension of the term "latch-up" itself. Historically, latch-up was restricted to the triggering of a parasitic thyristor structure (PNPN), but there are also other structures within an integrated circuit that can cause a similar low impedance path when triggered. Further, the effects of the low impedance path created by these other structures are indistinguishable from the effects of a triggered parasitic thyristor and, from a customer perspective, are just as detrimental to system performance.

Foreword (cont'd)

In JESD78F, the definition of the triggered structure was extended to an ESD protection device or any structure that, once triggered, will cause higher than normal currents to flow between power and ground, for example, bipolar transistors. Please note that current increase by a change of a functional state is still not considered as latch-up.

Amongst other changes, the problem with the classification of special pins is addressed by introducing a "decision flow" which considers many special pin types such as voltage reference pins, signal pins (formerly called I/O pins) with LDO's and voltage/current sensing pins. A revised Annex A adds decision diagrams and examples to aid with set-up of these types of pins.

JESD78F defined pre-conditioning of the device-under-test (DUT), the latch-up stress pulse, the detection of latch-up, and the failure criteria. JESD78 defines two different types of latch-up stresses, an overvoltage test applied to supply pins (in this document referred to as Supply Test) and a current injection test applied to signal pins (Signal Pin Test). The Signal Pin Test can be performed either as a test with a current stress pulse (in JESD78E and prior revisions as I-Test) or with a voltage stress pulse (known as E-Test in AEC-Q100-004-Rev-D). The possibility of using an E-Test instead of an I-Test for the current injection to a signal pad is new in this revision, although, in reality, the originally defined I-Test was often performed as an E-Test. Current injection in the Signal Pin Test is achieved either by forcing current with voltage compliance limit (I-Test) or by applying voltage with current compliance limit (E-Test). As the current injection test to signal pins can be performed as I-Test or E-Test, the terminology of this current injection test was changed to Signal Pin Test.

This revision does not cover transient-induced latch-up (also known as "Transient Latch-up, TLU") which is covered in ANSI/SP5.4.1-2017. Although the characterization method is in many ways similar, the purpose of JESD78 is to serve as a qualification standard, while transient-induced latch-up is currently a pure characterization methodology of some specific exposed or endangered pins with no specified immunity levels. To distinguish between TLU and "static" JESD78 latch-up, the rise time of the overstress causing latch-up in this document shall be longer than one microsecond.

Significant effort has been put into the ease of use of the document. The document has been re-organized, and the definitions clause (Clause 2) has been extended to describe the new terms and symbols. There have been significant upgrades to existing Annexes and new Annexes added to the document to aid in an improved understanding of the methods that enhance the effectiveness of the stress testing.

JESD78 should be considered as a living document. The JESD78 Working Group hopes that this current revision – JESD78F.02 – will enable smooth latch-up characterization for several years, but further changes, driven by technologies and applications, are already on the horizon.

IC LATCH-UP TEST

(From JEDEC Board Ballot JCB-23-53, formulated under the cognizance of JC-14.1 Committee on Reliability Test Methods for Packaged Devices.)

1 Scope, Purpose and Limitations

1.1 Scope

This standard establishes the procedure for testing, evaluation and classification of devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined latch-up stress. This standard covers a current-injection test (Signal Pin Test) and an overvoltage test (Supply Test). Current injection is achieved either by current forcing with voltage compliance limit (I-Test) or by applying voltage with current compliance limit (E-Test).

All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, optoelectronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this standard. This test method is applicable to NMOS, CMOS, bipolar, and all variations and combinations of these technologies including some Silicon-On-Insulator (SOI).

1.2 Purpose

The purpose (objective) of this standard is to establish a test method that will replicate latch-up failures during device operation and provide reliable, repeatable latch-up test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of latch-up sensitivity levels. The document will also provide guidelines to allow the user to apply engineering judgement when historical testing methods are not compatible with the integrated circuit's functionality.

1.3 Limitations

This standard will only consider direct current injection into and out of a signal pin (formerly called I/O pin), and overvoltage on the power supply pins. Transient induced latch-up will not be addressed. A transient-induced latch-up characterization methodology is defined in the ANSI/ESD Standard Practice SP5.4.1-2017 "Latch-up Sensitivity Testing of CMOS/BiCMOS Integrated Circuits – Transient Latch-up Testing, Device Level".

Latch-up failures will be limited to the detection of a sustained low-impedance path resulting from an applied trigger condition. Other types of potential functional failures, including logic state changes and spurious resets, are not considered by this standard, and are not considered latch-up failures.

2 Terms and Definitions

The following terms and definitions apply to this test method.

cool-down time: The period of time after the post pulse measurement and before the next application of stress.

DUT: The device under test.

dynamic pin: A pin or set of pins that experience a varying voltage or current during stress to other pins, for example, clock pins, crystal pins, etc.

NOTE A dynamic device has dynamic pin(s).

E-Test: A Signal Pin Test method using positive and/or negative voltage trigger pulses with a current compliance, as an alternative to I-Test, to evaluate latch-up sensitivity of an input or an output of a device.

EIPD (Electrically Induced Physical Damage): Damage to an integrated circuit due to electrical/thermal stress beyond the level which the materials could sustain. This would include melting of silicon, fusing of metal interconnects, thermal damage to package material, fusing of bond wires and other damage caused by excess current or voltage. (Ref: JEP174)

Ground: The common or zero-potential pin(s) of the DUT.

NOTE 1 Ground pins are not latch-up tested.

NOTE 2 A ground pin is sometimes called VSS. However, in some cases there can be multiple VSS pins, in which case these VSS pins may be referenced to a common ground.

I_{limit}: The value of the current limit for the power supplies and pulse sources for both the Signal Pin Test and Supply Test.

NOTE The I_{limit} is sometimes referred to as the current compliance on a power supply.

input pins: A subgroup of signal pins that is designed or can be configured to receive an external signal during latch-up testing. Examples of DUT pins that are typically defined as input pins for latch-up testing are address, data-in, control, clock, or similar pins.

NOTE 1 An input pin gets tied to a specific logic-low voltage level (V_{minOP}) or a specific logic-high voltage level (V_{maxOP}) during latch-up testing.

NOTE 2 Input pins are typically in a high-impedance state. There may be exceptions, for example, high-speed input pins with on-chip impedance matching/termination or input pins that have a weak-pull function enabled.

2 Terms and Definitions (cont'd)

NOTE 3 Pins defined in a datasheet as bi-directional (I/O) pins would also be defined as input pins for latch-up testing if they can be configured to receive an input signal.

NOTE 4 This definition reflects the usage within this latch-up test specification. Datasheets may use a different definition of input pins focusing on actual system applications (see clause 5.4.1).

I_{supply}: The total supply current in each V_{supply} pin (or pin group) with the DUT biased.

I-Test: A Signal Pin Test method using positive and/or negative current trigger pulses with a voltage compliance, as an alternative to E-Test, to evaluate latch-up sensitivity of an input or an output of a device.

latch-up: A Sustained High-Current Event within an integrated circuit caused by the triggering of any structure resulting in a sustained low impedance path that persists even after the removal of the triggering condition.

NOTE 1 Examples of structures causing latch-up include thyristors (PNPN), BJTs (PNP or NPN) and similar structures that are either of a parasitic nature or part of the electrical protection structures. Other structures causing latch-up include active ESD clamp circuits that remain in a triggered condition. Most changes in a functional state related to normal chip operation (for example switching of power modes due to the triggering condition) are not considered latch-up.

NOTE 2 The classical definition of latch-up explicitly refers to a parasitic thyristor (PNPN), whereas this specification document uses a more generic definition to include other latching structures that can be identified by the described test method.

NOTE 3 Latch-up typically occurs between power and ground, but could also involve signal pins as described in Annex H.

NOTE 4 The applied triggering condition can be a voltage or current impulse, an excessive rate of change of current or voltage, or any other abnormal condition that causes latch-up.

latch-up immunity: The ability of an integrated circuit to resist any impulses of current or voltage that might create a latch-up condition.

logic-high: A valid voltage level within the more positive (less negative) of the two ranges of logic levels chosen representing the logic states during setting high and low levels.

logic-low: A valid voltage level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states during setting high and low levels.

maximum stress voltage (MSV): The maximum voltage (duration dependent) allowed to be placed on a given pin during latch-up immunity testing without causing irreversible damage to the device from a permanent physical breakdown of the silicon device or circuit not caused by latch-up.

2 Terms and Definitions (cont'd)

NOTE 1 A positive MSV is higher than the maximum operating voltage and a negative MSV is lower than the minimum operating voltage.

NOTE 2 MSV is NOT the same as the absolute maximum voltage rating (AMR) from the device datasheet. MSV applies to latch-up testing only, protecting the DUT from physical damage from stress mechanisms not directly related to latch-up. An example of an unrelated stress is one exceeding the destructive breakdown voltage of a pin resulting in non-latch-up induced catastrophic breakdown of the silicon device/circuit.

NOTE 3 MSV may be different for each pin and each polarity during testing, depending on process technology and circuit topology. In many medium and high voltage designs, MSV is very rarely the same value as AMR.

NOTE 4 The MSV value depends on the pulse width used during latch-up testing. Shorter pulse widths may allow a higher value for MSV. Therefore, the MSV value chosen should consider the pulse width as well as process technology and circuit topology.

“no connect” pin: A pin that has no internal electrical connection to the die.

NOTE All “no connect” pins are to be left in an open (floating) state and should not be stressed during latch-up testing.

nominal I_{supply} (I_{nom}): The measured dc supply current for each V_{supply} pin (or pin group) with the DUT biased at the maximum operating conditions.

output pins: A subgroup of signal pins that are not configured to receive an external signal during latch-up testing because they drive out a signal or a voltage level.

NOTE 1 Output pins, though left in an open (floating) state during testing of other pin types, should be latch-up tested.

NOTE 2 Output pins are typically in a low-impedance state.

NOTE 3 This definition reflects the usage within this latch-up test specification. Datasheets may use a different definition of output pins focusing on actual system applications (see clause 5.4.1.)

power supply: A component in the test system that supplies voltage and current to the DUT.

preconditioned pin: A device pin that has been placed in a defined state or condition by applying static or dynamic control signals to the DUT or biasing the appropriate steady state control pin(s) in order to put the device into a known, controlled and stable state.

preconditioning vectors: a series of commands sent to an integrated circuit instructing the circuit to perform a specified series of functions or place it into a known state.

2 Terms and Definitions (cont'd)

pre-stress & post-stress current (I_{psPRE} & I_{psPOST}): The pulse supply current corresponding to the Signal Pin Test or Supply Test before (pre-stress) & after (post-stress) pulse application.

NOTE 1 I_{psPRE} & I_{psPOST} can either be a forced value or the limit value depending on the mode of the source (I-Test or E-Test).

NOTE 2 It is also known as parking current in some commercial systems.

pre-stress & post-stress voltage (V_{psPRE} & V_{psPOST}): The pulse supply voltage corresponding to the Signal Pin Test or Supply Test before (pre-stress) & after (post-stress) pulse application. It is not dependent on polarity.

NOTE 1 V_{psPRE} & V_{psPOST} can either be a forced value or the limit value depending on the mode of the source (I-Test or E-Test).

NOTE 2 V_{psPRE} & V_{psPOST} are typically either V_{maxOP} or V_{minOP} for these systems.

NOTE 3 It is also known as parking voltage in some commercial systems.

PUT: Pin Under Test

signal pins: Device pins that carry an electrical signal (information) during stable operation of the device and are not used as supply pins.

Signal Pin Test: A test that injects positive and negative current pulses to the pin under test (PUT) by either injecting a current pulse (I-Test) with a voltage limit or injecting a voltage pulse (E-Test) with a current limit.

steady state control pins: Pins used to place the DUT in the desired configuration (IO configuration pins, reset, power good/OK, enable, other control pins) whose logic or bias state remains constant for the duration of the test. (See Clause 5.4.1)

NOTE Steady state control pins, though remaining in a constant state, may still be latch-up tested with a stress pulse polarity that does not alter their logic state.

Supply Test (previously V_{supply} overvoltage test): A latch-up test that supplies overvoltage pulses to the supply pin (or pin group) under test.

temperature, maximum operating junction (T_{jmax}): The maximum junction temperature of a device to operate within its specifications, as listed in its data sheet and to avoid damage (latent or otherwise). It is frequently specified by device manufacturers for a specific device and/or technology.

2 Terms and Definitions (cont'd)

temperature, junction (T_j): The temperature of a semiconductor junction in a device.

temperature, ambient (T_a): The local air temperature surrounding the device, in an environment controlled only by natural air convection and not materially affected by reflective and radiant surfaces.

temperature, case (T_c): The temperature measured or calculated on the case surface of a device. (As per JESD88F)

NOTE See Clause 3.2 and/or Annex B for further information on measuring/calculating case temperature using ambient or junction.

timing-related input pin: A pin such as clock crystal oscillator, charge pump circuit, etc., required to place the DUT in a stable operating mode. Required timing signals may be applied by the latch-up tester, external equipment, and/or external components as appropriate.

test condition: The test temperature, supply voltage, current limits, voltage limits, clock frequency, input bias voltages and preconditioning vectors applied to the DUT during the latch-up test.

trigger duration: The duration of an applied pulse from the trigger source.

trigger pulse: The positive or negative current pulse (Signal Pin Test) or voltage pulse (Supply Test or E-Test) applied to any pin under test for latch-up sensitivity.

tri-state (also known as three-state): Cells or macros whose outputs can be placed in a high-impedance state and can also generate low-impedance V_{maxOP} and V_{minOP} levels. (Ref JESD12-4, 4/87)

Vlimit: The value of voltage used to limit the actual voltage, and thereby restricts the forced current into and out of a signal pin during latch-up stress.

V_{maxOP} : The maximum operating bias voltage of the PUT given in the device datasheet.

V_{maxSUP} : It is the maximum supply voltage at which a supply is specified to operate in conformance with the applicable device specification; formerly maximum V_{supply} in previous revisions.

V_{minOP} : The minimum operating bias voltage of the PUT given in the device datasheet.

V_{supply} pin (or pin group): A supply pin is any pin that provides current to a circuit. Supply pins typically transmit no information (such as digital or analog signals, timing, clock signals, and voltage or current reference levels). Supply pins are often referred to as power pins.

2 Terms and Definitions (cont'd)

NOTE 1 It is generally permissible to treat supply pins with the same or similar voltage as one V_{supply} pin (or pin group) and connect them to one power supply.

NOTE 2 When combining V_{supply} pins (or pin groups) with the same or similar voltage, combining V_{supply} pins with significantly different supply current levels is not recommended as this would make it difficult to detect significant current changes on low supply current pins.

3 Latch-Up Characterization

A component's susceptibility to a latch-up event is characterized by its response to a stress when either current is injected into a signal pin or when a supply overvoltage occurs operating within the temperature range of the component's specified operating junction temperature. This clause describes the Immunity Levels (A and B) and the temperature classification (II and I) for latch-up characterization.

3.1 Latch-Up Immunity

Product latch-up immunity is characterized by the forced current or voltage value at the signal pin and overvoltage value on the supplies that does not result in latch-up as defined in this test standard. Table 1 defines Immunity Levels A and B at specified ranges for injected current and applied voltage stress levels.

Table 1 --- Latch-Up Immunity Levels

Immunity Level	Test	Absolute Magnitude of Injected Trigger Current or Absolute Magnitude of Applied Trigger Voltage
A	Positive Signal Pin Test (1)	$\geq 100 \text{ mA}$ The actual injected current may be less than 100 mA, if pin voltage preset limits are reached
	Negative Signal Pin Test (1)	
	Supply Test	$1.5 \times V_{\text{maxSUP}}$ or MSV, whichever is less The actual applied voltage may be less than $1.5 \times V_{\text{maxSUP}}$ or MSV, if supply current limits are reached
B	If Immunity Level A cannot be achieved	
(1) In the Signal Pin Test, current injection is achieved either by current forcing with voltage compliance limit (I-Test) or by applying voltage with current compliance limit (E-Test).		

3.1 Latch-Up Immunity (cont'd)

The actual current injected into the signal pin during the Signal Pin Test may be limited by the signal pin design or due to the test methods described in Table 2 for the preset conditions that limit the signal pin voltage during the current injection. Likewise, the actual applied voltage during the Supply Test may be limited by the preset current limit into the supply. If latch-up does not occur in such a condition, then this constitutes a passing test with Immunity Level A. Otherwise, it is classified with Immunity Level B.

3.2 Temperature Classification

Since the likelihood for a latch-up occurrence increases with temperature, latch-up testing shall be performed at a junction temperature (T_j) equivalent to its maximum operating junction temperature (T_{jmax}).

The two latch-up temperature classifications for latch-up testing are:

- Class II – For latch-up testing at T_{jmax} , or the T_{amax}/T_{cmax} equivalent of T_{jmax} . Class I testing is not required if Class II testing achieves Immunity Level A (Table 1).
- Class I – For latch-up stress testing at junction temperatures below Class II. If the passing temperature is below T_{jmax} , the maximum passing temperature shall be reported.

NOTE See Annex B for further information on T_{amax} , T_{cmax} and T_{jmax} .

3.3 Overall Requirements

The requirements to classify latch-up susceptibility are the following:

- Class II.A: Meets Level A latch-up immunity requirements at T_{jmax}
- Class I.A: Meets Level A latch-up immunity requirements at temperatures lower than T_{jmax}
- Class II.B: Meets Level B immunity latch-up requirements at T_{jmax}
- Class I.B: Meets Level B immunity latch-up requirements at temperatures lower than T_{jmax}

NOTE Class II.A in this document is a Revision E Class II enhancement.

4 Apparatus and Material

The apparatus required for this test method includes the following:

4.1 Latch-Up Tester

4.1.1 Hardware Requirements and Capabilities

Test equipment capable of performing the tests as specified in this document consist of the following:

- Bias power supplies having the ability of providing the required voltage and current, plus the ability to monitor the voltage and current being drawn by the DUT. The response time of the supply should also be considered, as to avoid incorrect measurements during transient events.
 - Bias power supplies should also have the capability to drive input pins to their $V_{\max OP}$ or $V_{\min OP}$ when not being stressed.
- The stress power supply shall have the ability to force and measure both current and voltage before, during and after stressing of the DUT. The supply shall have the ability to set compliance limits, with adequate response time to avoid over stressing of the DUT. It shall be capable of meeting the timing requirements in Table 5. See Annex F for further discussion on pulse source verification and for possible supply sensitivities that can occur during stressing.
- For devices requiring dynamic testing, the test equipment shall be capable of supplying timing signals. The required timing signals may be applied by the latch-up tester itself, external equipment, and/or external components as appropriate.
- For devices requiring setup vectors to place the device into a state suitable for latch-up testing the test equipment shall be capable of supplying the required vectors. The required timing signals and logic vectors may be applied by the latch-up tester itself, external equipment, and/or external components as appropriate as specified in 5.4.3.

4.1.2 Test Board

Test board options will depend on the test system capabilities and hardware configurations. The common options are listed below.

- Many commercial systems will use generic test boards for both ESD and latch-up testing. Reusability for both ESD and latch-up testing is possible by having only a single board trace from the test system channel pin to the socket pin. The board shall not have any other components that limit the ability to perform latch-up on any pin. Supply and signal pins can be assigned to any tester channel pin. This adds flexibility during debug and failure analysis by having the ability to reassign supply pins to determine the failing supply.

NOTE Some devices may need a latch-up specific board, where high supply current capability is needed on a limited number of V_{supply} pin groups which may be connected via an inner plane

4.1.2 Test Board (cont'd)

- Use of passive or active elements:
 - Series passive or active elements that may limit the magnitude of the injected pulse are strongly discouraged (see Annex A for additional guidance).
 - Parallel passive or active elements used to support control pin regulation or add to the DUT stability are allowed if required for stable device operation. The use of inductors is strongly discouraged (see Annex A for additional guidance).
 - Any use of these elements shall be recorded as part of the latch-up data as described in Annex D.
- Boards for ATE testing or similar device test board for functional and parametric testing can be used for latch-up testing. These boards may have components, such as capacitors and resistors for device stability; thus, the supply pins and signal pins are not easily reassigned. These boards may emulate actual end user system boards.

For all board types, the trace cross-sectional areas should be sufficient to carry expected current levels without excessive IR drops during latch-up testing. During latch-up testing, currents will exceed nominal levels both on supply pins and signal pins.

4.1.3 Temperature Control

Equipment capable of heating (or in some cases cooling) a device to maintain the DUT at the maximum operating junction temperature (T_{jmax}) as specified by the device specification during the latch-up test is required. Refer to Annex B for further details on controlling temperature.

5 Latch-Up Test Procedure

5.1 General Latch-Up Test Overview

This clause describes the standard procedures to stress a component to trigger and detect a latch-up event. Its ability to resist latch-up will determine the device's Immunity Level as described in Table 1.

Two stress methods, called the Signal Pin Test and Supply Test, are used to trigger a possible latch-up event.

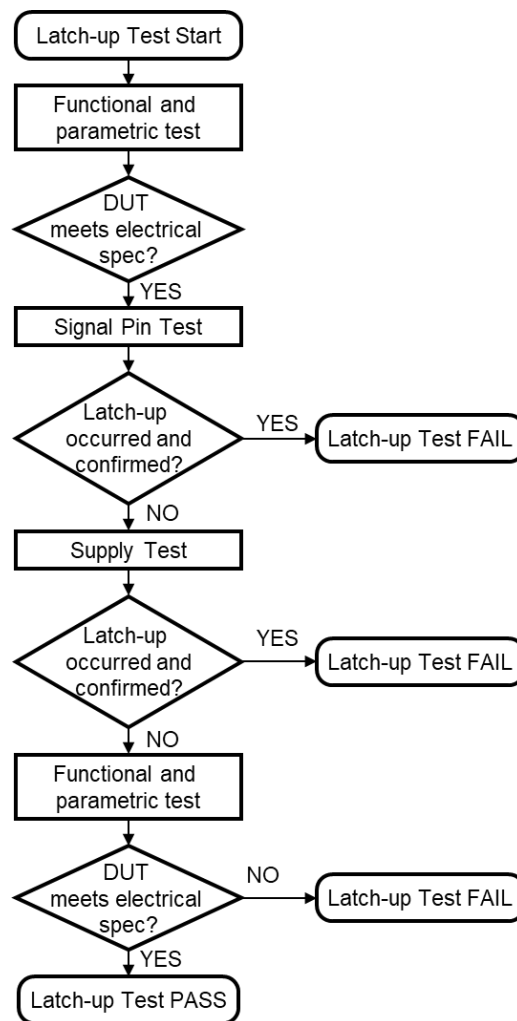
- For the Signal Pin Test, current flows into a signal pin by either injecting current while limiting the signal pin voltage, or by applying a voltage with the current limited to the minimum required current level, such as 100 mA for Immunity Level A (see Table 1).
- The Supply Test attempts to trigger latch-up by an overvoltage of the supply at stress levels described in Table 1.

Signal Pin and Supply latch-up tests are required to be performed to meet the Immunity Levels requirements.

5.1 General Latch-Up Test Overview (cont'd)

Figure 1 shows the general latch-up test flow for the Signal Pin Test and Supply Tests. Prior to stressing, complete static and dynamic testing shall be performed on all submitted devices with adequate test coverage to be able to detect any latch-up induced degradation. Parametric and functional results shall be within the limits specified in the datasheet.

NOTE Some failures may only be found when static and dynamic testing is completed at the datasheet high temperature limits.



NOTE The order of the Signal Pin Test and the Supply Test is arbitrary.

Figure 1 — General Latch-Up Test Flow for the Signal Pin Test and Supply Tests.

After latch-up stress the device will be retested to determine if the device continues to meet specification or if any possible damage has occurred.

5.1 General Latch-Up Test Overview (cont'd)

All input and output pins shall be tested with the Signal Pin Test as described in more detail in Clause 5.6 using the limits in Table 2, unless these pins fall into specific cases, listed in Clause 5.4.1. Pins stressed with the Signal Pin Test will be stressed at positive and negative polarities of the current injection, while input pins not under test are all tied to the maximum pin operational voltage $V_{\max OP}$ or all tied to minimum pin operational voltage $V_{\min OP}$ (see Table 2), followed by testing with the pins in the opposite states unless these pins fall into specific cases listed in Clause 5.4.1.

The Signal Pin Test can be accomplished by using either a forced pulsed current with voltage limiting (I-Test) or an applied pulsed voltage with limiting current (E-Test). Historically, I-Test has been the stress used most often for latch-up stress testing. E-Test provides an option to Signal Pin stress with forced pulsed voltage. Signal Pin response to the type of pulse may dictate which stress test is appropriate. I-Test and E-Test are considered to be equivalent stress tests as long as the forcing and limiting values are set properly. See Annex G for additional information.

All supply pins shall be tested with the Supply Test, as described in more detail in Clause 5.7 and using the limits in Table 7. Input pins not under test are all at $V_{\max OP}$ or all at $V_{\min OP}$ (see Table 2), followed by testing with the pins in the opposite states unless these pins fall into specific cases listed in Clause 5.4.1.

In the latch-up test, all devices shall pass the latch-up criteria specified in Table 3. A failure of any of the devices tested during the Signal Pin Test or Supply Test, or if any of the devices do not meet the electrical specification after stress, constitutes a latch-up failure.

Table 2 — Overview of Latch-Up Tests for a Complete Latch-Up Characterization

Stress Type	Stress Polarity of Trigger	Input Pins Not Under Test ⁽¹⁾
Signal Pin Test (I-Test OR E-Test)	Positive current injection	Maximum pin operational voltage V _{maxOP}
		Minimum pin operational voltage V _{minOP}
	Negative current injection	Maximum pin operational voltage V _{maxOP}
		Minimum pin operational voltage V _{minOP}
Supply Test	Overvoltage	Maximum operational voltage V _{maxOP}
		Minimum operational voltage V _{minOP}
(1) All pins which are not excluded according to Clause 5.4.1.		

5.2 Device Handling

Devices used for latch-up testing shall not have been used for any prior stress tests. ESD damage prevention procedures shall be used before, during, and after latch-up testing and post parametric and functional testing.

NOTE See the latest revision of ANSI/ESD S20.20, JESD625, or IEC61340-5-1 for guidance.

5.3 Sample Size

A minimum of three (3) devices shall be subjected to testing using the Signal Pin Test and Supply Test. It is allowed to partition Signal Pin Test and Supply Test, or test combinations by using at least three (3) fresh devices for each partition. All partitions used shall cover all combinations of stresses originally planned for the product.

All devices to be tested shall have passed functional and parametric testing to the device specification requirements.

5.4 Preparation of the Latch-Up Test

5.4.1 Pin Types and Grouping

In preparation for testing, pin grouping and test limits are determined based on the product datasheet.

- 1) Identify all pins as signal, supply pins or no connects. Whether a pin is tested as a signal pin (Signal Pin Test) or as a supply pin (Supply Test), depends on the functionality and/or the configuration of the pin in the system. For special pins, Annex A gives guidance on how these pins shall be treated. Some examples of special pins are pins connected to passive components, voltage regulators, reference pins or debug pins.
 - Shorted input pins that are connected by a low resistance connection in the package or on the die or by a common bond pad shall be represented by a single pin with all other pins shorted to that pin configured as “no connect pins” to avoid contention. Alternatively, the pins may be shorted on the test board and controlled and stressed by a single supply. These methods may be applied to shorted output pins.
- 2) Split the group of all signal pins into groups of input pins and output pins. For the purpose of latch-up testing, all signal pins that can be placed in a high-impedance state should be defined as input pins. All pins that are in a low-impedance state (driving out a signal or voltage level) and which cannot be placed in a high-impedance state should be defined as output pins. The product datasheet may provide guidance for this pin categorization. For example, pins that are described as “Input”, “I/O”, or “Bi-Directional” in a datasheet would typically be treated as input pins for latch-up testing. Pins that are described as “Output” in a datasheet would typically be treated as output pins for latch-up testing unless they can be tri-stated, in which case the pins should be defined as input pins.

5.4.1 Pin Types and Grouping (cont'd)

- 3) Identify the pins that may have special consideration for testing. Some of these pins should still be tested but may need to be tested separately from the primary testing of the signal pins or may need to be preconditioned in special states. These pins typically fall into the following categories:
 - “no connect” pins are not required to be tested.
 - Timing related pins, such as a clock input or crystal oscillator pins required to maintain the device in a stable mode or for dynamic testing. If an alternate means of placing the DUT in stable operating mode can be achieved, then the full Signal Pin Test can be accomplished on the timing related pins.
 - Steady state control pins used to precondition the device in the desired configuration, such as signal pin configuration pins, reset, and power enable, or other control pins, may require special testing. Steady state control pins may be subject to reduced testing with the current stress polarity that does not disrupt the DUT, such as a reset pin that shall be kept in one logic state.
- 4) For all input and output pins determine the $V_{\max\text{OP}}$ and $V_{\min\text{OP}}$. Input and output pins with common operating voltages may be grouped as single pin groups for testing. When possible, separating grouped signal pins on a tester supply not used as a device power supply is advised for easier determination of possible failures. $V_{\max\text{OP}}$ and $V_{\min\text{OP}}$ shall be used for the logic-high and logic-low for input pins, and also used to calculate the maximum voltage (compliance limit) for the Signal Pin Test for these pins.
- 5) All supply pins with the same supply voltage may be grouped into a single supply group. Determine the maximum supply current for each device supply, $V_{\max\text{SUP}}$. See Clause 5.4.2 below.

NOTE: In most test systems, there are insufficient power supplies to provide power individually to each supply pin (group). Grouping of supply pins (groups) allows for efficient use of the power supplies available. More details are given in 5.4.2.

5.4.2 Power Supply Assignments

Some devices may have several power rails that exceed the number of available power supplies in the latch-up test system, therefore, grouping of the supplies will be necessary. In this case, planning of the supply assignment should be optimized to improve the detectability of a latch-up occurrence when several supply groups are assigned to a single power supply on the tester. Therefore, it is recommended to group the device supply pins and assign the power supplies so that device supply rails with small currents are not combined with those with large currents, to avoid masking of a latch-up occurrence on the small current supply rail.

Latch-up testing requires the input pins to be tied to the maximum pin operational voltage ($V_{\max\text{OP}}$) or tied to the minimum pin operational voltage ($V_{\min\text{OP}}$), see Table 2. $V_{\min\text{OP}}$ is typically tied to ground but may be a value other than 0 V if the test system is capable. There are two suggested methods to assign the supply for the bias on the signal pin to $V_{\max\text{OP}}$ or $V_{\min\text{OP}}$.

- 1) For optimal latch-up detection, assign a separate supply for the signal pins to bias for $V_{\max\text{OP}}$ or $V_{\min\text{OP}}$. The advantage is that any latch-up of the signal pin itself (see Annex H) or a state change may be more easily detected.

5.4.2 Power Supply Assignments (cont'd)

- 2) If $V_{\max\text{OP}}$ and $V_{\max\text{SUP}}$ are the same, the same power supply may be used for the pin groups.

NOTE If there is a sufficient number of power supplies, it is recommended to use separate supplies for the supply pin power and for the supply to tie the signal pins to $V_{\max\text{OP}}$.

NOTE If the number of power supplies are limited, making it necessary to use the same power supply for $V_{\max\text{OP}}$ on the inputs and provide power to the DUT, ensure that the MSV for the signal pins is not exceeded when performing the Supply Test stress. Otherwise, reconfigure the supplies to avoid exceeding the MSV on these input pins to avoid overstress.

5.4.3 Product Pre-Conditioning

To avoid masking a latch-up occurrence, the device shall be in a low power-consuming state or a stable operating mode for latch-up testing. Output pins capable of being put into tri-state should be tested with both positive and negative pulses.

All voltage rails, including internal power supplies, shall be powered up at $V_{\max\text{SUP}}$ and all functional blocks shall be supplied.

Typically, either a static signal, a dynamic and/or vector pattern is required to pre-condition the DUT in a stable test mode. Often the static signal, a dynamic and/or vector pattern should be re-run after each latch-up stress to ensure that the initial state of the DUT is well defined.

5.4.4 Device Temperature Set-Up

Proper temperature control for latch-up testing is critical to accurately test a product. Product datasheets typically specify $T_{j\max}$. Since T_j can vary spatially across the die in operation, using the datasheet $T_{j\max}$ for latch-up testing ensures that any latch-up sensitivities are evaluated at the maximum field operating temperature.

If $T_{j\max}$ is not listed in the product datasheet, it can be calculated from other datasheet temperature specifications such as maximum case temperature (T_c) or ambient operating temperature (T_a) using field thermal resistance coefficients. Annex B provides equations for calculating T_j , T_a and T_c based on dissipated power and thermal resistances (θ).

5.5 Latch-Up Detection Criteria

5.5.1 Latch-Up Detection

A device is considered to have experienced latch-up if it meets the latch-up detection criteria in Table 3 or it is not within the device datasheet specification after both latch-up and ATE testing (Clause 5.8).

5.5.1 Latch-Up Detection (cont'd)

Table 3 — Latch-Up Detection Criteria

Stress Type	Trigger Stress	Latch-Up Detection Criteria
Signal Pin Test⁽¹⁾ (I-Test OR E-Test)	Positive current injection	If $ I_{nom_pre} \leq 25 \text{ mA}$: LU occurs if $ I_{nom_post} > I_{nom_pre} + 10 \text{ mA}^{(2)}$ or If $ I_{nom_pre} > 25 \text{ mA}$: LU occurs if $ I_{nom_post} > 1.4 \times I_{nom_pre} ^{(2)}$
	Negative current injection	
Supply Test	Overvoltage	
(1) In the Signal Pin Test, current injection is achieved either by current forcing with voltage compliance limit (I-Test) or by applying voltage with current compliance limit (E-Test). (2) During I-Test, E-Test or Supply Test, the supply currents for all supply groups are monitored before and after the stress pulse. Comparison of I_{nom_post} to I_{nom_pre} and the criteria above determine if latch-up occurs.		

5.5.2 Power Supply Current Limits

Latch-up test equipment power supplies, used for supply pins or for biasing signal pins, generally have current limits (I_{limit}) assigned for device and test fixture protection considerations. When a supply current or signal pin biasing current reaches these power supply limits, the test result may be invalid.

A latch-up event that reaches the I_{limit} could collapse the power supply below the latch-up holding voltage and terminate latch-up before the automated test equipment detects it as a latch-up failure. The stability of the voltage levels of all the tester supplies that measure currents should be monitored during latch-up testing to ensure that the currents are kept below the assigned I_{limit} . This includes tester power supplies used for biasing signal pins at V_{maxOP} or V_{minOP} or for preconditioning of signal pins, for instance.

Unlike bias power supplies used to precondition signal pins during the test, pin drivers (vectors) used to precondition signal pins may not have current measuring capabilities, as they are intended to drive signal pins with a specified pattern. Other stress methods may need to be used to verify latch-up has not occurred on these pins. Use of unmonitored supplies is not recommended and should be limited to devices requiring set-up vectors.

General test procedures and recommendations:

- All monitored tester supply voltages shall remain within their specified range, including the time before, after, and while the current trigger is applied. If a tester supply, including vector supplies cannot be monitored, it shall be reported (see Clause 6).

5.5.2 Power Supply Current Limits (cont'd)

- It is recommended that for each V_{supply} pin (or pin group), the I_{limit} is initially set to at least:
 - I_{nom} plus 2 times the injection current, or
 - 1.4 times I_{nom} , whichever is higher.
- If the voltage of any V_{supply} collapses or reaches its I_{limit} prior to the trigger source being applied and/or while the trigger source is applied to any pin, the Signal Pin Test and/or Supply Test becomes invalid; review of the latch-up test set-up may be required and/or the stress needs to be repeated with a higher I_{limit} setting.

It is permissible to provide any Signal Pin Test and/or Supply Test characterization results obtained with lower I_{limit} settings in the latch-up report. These characterization results can be provided in addition to the required absolute Signal Pin Test and/or Supply Test passing levels with stable tester supplies (see examples in Annex D). Reported entries should include the specific I_{limit} settings used and the corresponding collapsing power supplies during the current trigger. The additional characterization data may appropriately reflect latch-up robustness in system applications exhibiting supply current limitations, similar to these lower I_{limit} settings.

Every product pin tested shall be classified as either a Pass, a Fail or Invalid.

5.6 Signal Pin Test

5.6.1 Signal Pin Test Flow

All signal pins on the package are tested with the Signal Pin Test, with possible exceptions, listed in Clause 5.4.1 or the pin is non-standard requiring an unusual configuration and it may meet the criteria in Annex A.

The Signal Pin Test shall be performed according to the testing matrix summarized in Table 2. Each signal pin will be stressed with both a positive and a negative current injection, with inputs tied to maximum pin operational voltage V_{maxOP} and repeated with inputs tied to minimum pin operational voltage V_{minOP} , in total four combinations. There may be exceptions for pins that cannot be in one of the conditions based on being a preconditioning pin such as control and reset pins, clock pin, crystal pins, etc. Latch-up testing will be performed with the waveforms and timing diagrams specified in Clause 5.6.2 (positive current injection) and Clause 5.6.3 (negative current injection).

The Signal Pin Test can be accomplished by using either a forced pulsed current with voltage limiting (I-Test) or a forced pulsed voltage with current limiting (E-Test). Historically, I-Test has been the stress used most often for latch-up stress testing. E-Test provides an option to stress with forced pulsed voltage. Signal pin response to the type of pulse may dictate which stress test is appropriate. I-Test and E-Test are considered to be equivalent stress tests as long as the forcing and limiting values are set properly.

5.6.1 Signal Pin Test Flow (cont'd)

One suggested Signal Pin Test procedure is given below. It covers all the conditions in the test matrix in Table 2. The testing order of the stress conditions may vary as long as all conditions are met in the test matrix table. The procedure below describes one possible sequence:

- 1) Positive current injection with non-stressed input pins tied to minimum pin operational voltage $V_{\min OP}$
- 2) Positive current injection with non-stressed input pins tied to maximum pin operational voltage $V_{\max OP}$
- 3) Negative current injection with non-stressed input pins tied to minimum pin operational voltage $V_{\min OP}$
- 4) Negative current injection with non-stressed input pins tied to maximum pin operational voltage $V_{\max OP}$

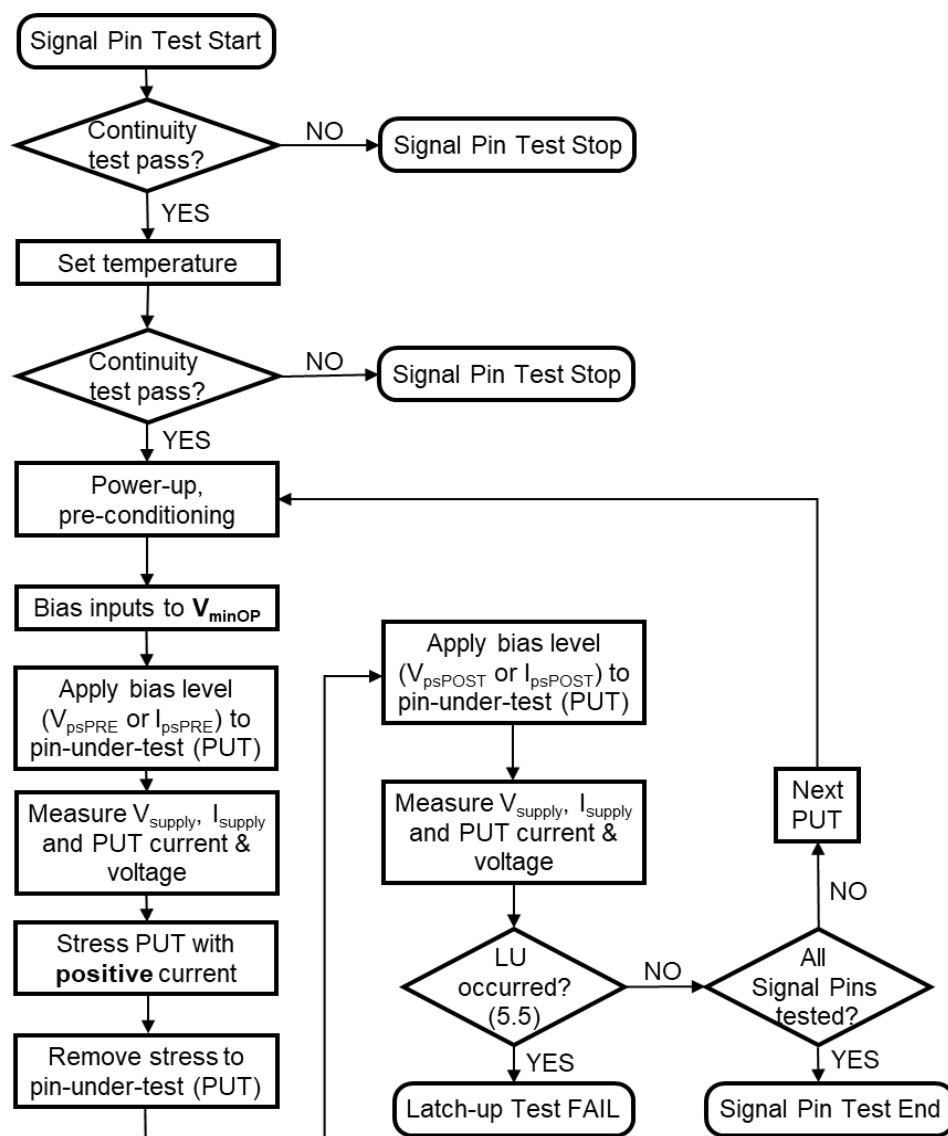


Figure 2 — Signal Pin Test Flow Example: Positive Current Stress with Input Pins Biased to Low ($V_{\min OP}$). Also Applicable to $V_{\max OP}$.

5.6.1 Signal Pin Test Flow (cont'd)

Step:

- 1) Insert a device that has met electrical specification in the test socket. Ensure that the desired temperature at the DUT has been reached and has stabilized. Check the DUT continuity to ensure that each pin makes good electrical contact. If the DUT continuity fails, re-seat the DUT in the socket until good contact is achieved.
- 2) Power up the device per power-up sequence specification.
- 3) Precondition the device according to Clause 5.4.3.
- 4) Bias the DUT. All inputs pins that are not used for preconditioning are tied to $V_{\max OP}$ if possible, and output pins should remain floating unless being stressed. See Annex H for additional guidance.

NOTE Input pins used for preconditioning, such as control and reset pins, shall be tested in their defined state. That is, pins that are tied to $V_{\max OP}$ to precondition the DUT can only be tested with $V_{\max OP}$, and pins that are tied to $V_{\min OP}$ to precondition the DUT can only be tested with $V_{\min OP}$.

- 5) For positive current injection into the PUT, apply a pre-stress voltage (V_{psPRE}) equivalent to $V_{\max OP}$ to the PUT.
- 6) Measure nominal I_{supply} at $V_{\max SUP}$ for each V_{supply} pin (or pin group).
- 7) After the wait period, force a positive current trigger into the PUT as specified in Clause 5.6.2. Measure the current and voltage of the Stress Supply and each V_{supply} during the stress period.
- 8) After completion of the trigger pulse, return the PUT to the level before the application of the trigger pulse (voltage equivalent to $V_{\max OP}$) and measure the I_{supply} at $V_{\max SUP}$ for each V_{supply} pin (or pin group). If any I_{supply} is greater than or equal to the failure criteria specified in Clause 5.5, latch-up has occurred and the DUT has failed latch-up testing. The power supply shall be removed from the DUT to end latch-up, further testing is stopped if latch-up has occurred.

NOTE If the device is not damaged it is permissible to restart latch-up testing to determine if there are other pins which fail the latch-up test.

- 9) If latch-up has not occurred, after the necessary cool-down time, continue to the next pin under test and repeat Steps 2-8 until all signal pins are tested for positive current injection.

NOTE Signal Pin Tests do not necessarily require the removal of the power supplies and pre-conditioning between the stresses, so it is permitted to repeat only Steps 5–8.

- 10) Repeat steps 2-9 with inputs pins that are not used for preconditioning tied to $V_{\min OP}$ and outputs are floated (Step 5).
- 11) Repeat steps 2-10 for negative current injection into the PUT, apply a pre-stress voltage (V_{psPRE}) equivalent to $V_{\min OP}$ to the PUT (Step 6) and a negative current trigger into the PUT as specified in Clause 5.6.2.
- 12) It is good practice to perform continuity testing at completion of the stress.