

JEDEC STANDARD

DDR2 SDRAM SPECIFICATION

JESD79-2F

(Revision of JESD79-2E)

November 2009

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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1 Scope

This document defines the DDR2 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Specification is to define the minimum set of requirements for JEDEC-compliant 256 Mb through 4 Gb for x4, x8, and x16 DDR2 SDRAM devices. This specification was created based on the DDR specification (JESD79). Each aspect of the changes for DDR2 SDRAM operation were considered and approved by committee ballot(s). The accumulation of these ballots were then incorporated to prepare this JESD79-2 specification.

2 Package ballout & addressing

2.1 DDR2 SDRAM package ballout

(Top view: see balls through package)

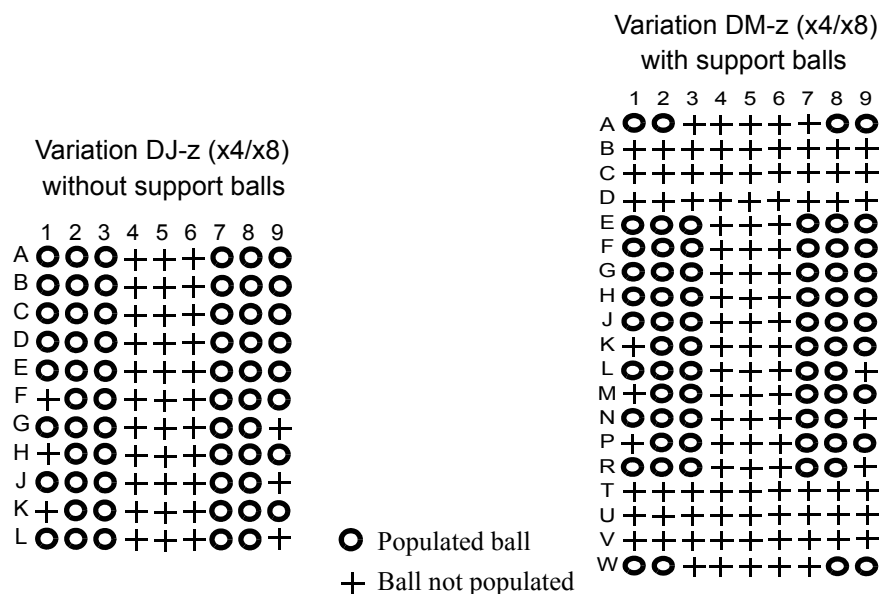
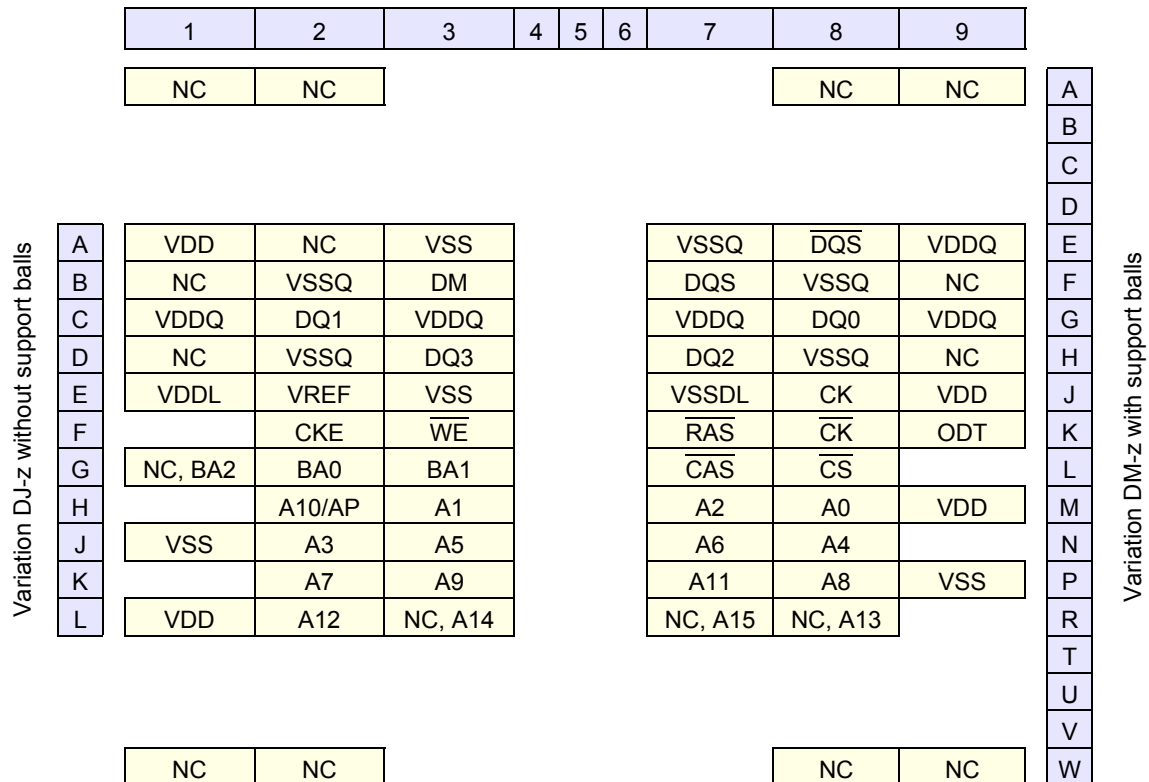


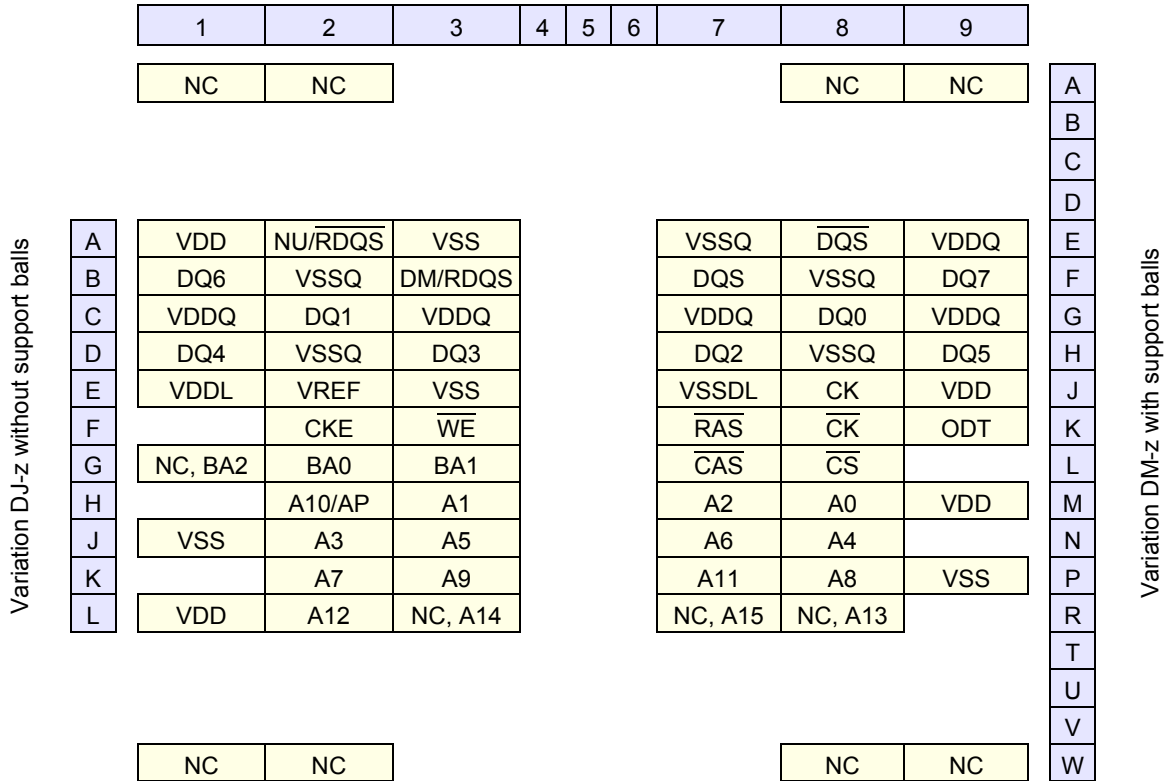
Figure 1 — DDR2 SDRAM x4 ballout using MO-207



2 Package ballout & addressing (cont'd)

2.1 DDR2 SDRAM package ballout (cont'd)

(Top view: see balls through package)



- NOTE 1 B1, B9, D1, D9 = NC for x4 organization per variation DJ-z.
- NOTE 2 Pins B3 and A2 have identical capacitances as pins B7 and A8.
- NOTE 3 For a Read, when enabled, strobe pair RDQS & $\overline{\text{RDQS}}$ are identical in function and timing to strobe pair DQS & $\overline{\text{DQS}}$ and input data masking function is disabled.
- NOTE 4 The function of DM or RDQS/ $\overline{\text{RDQS}}$ is enabled by EMRS command.
- NOTE 5 VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ. However as this is not required, users should refer to vendor data sheet for actual implementation information.

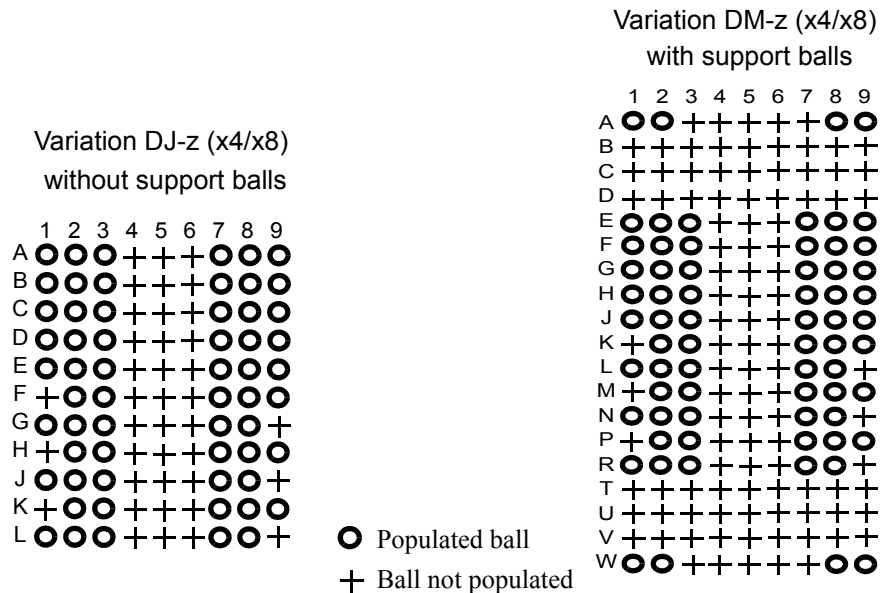
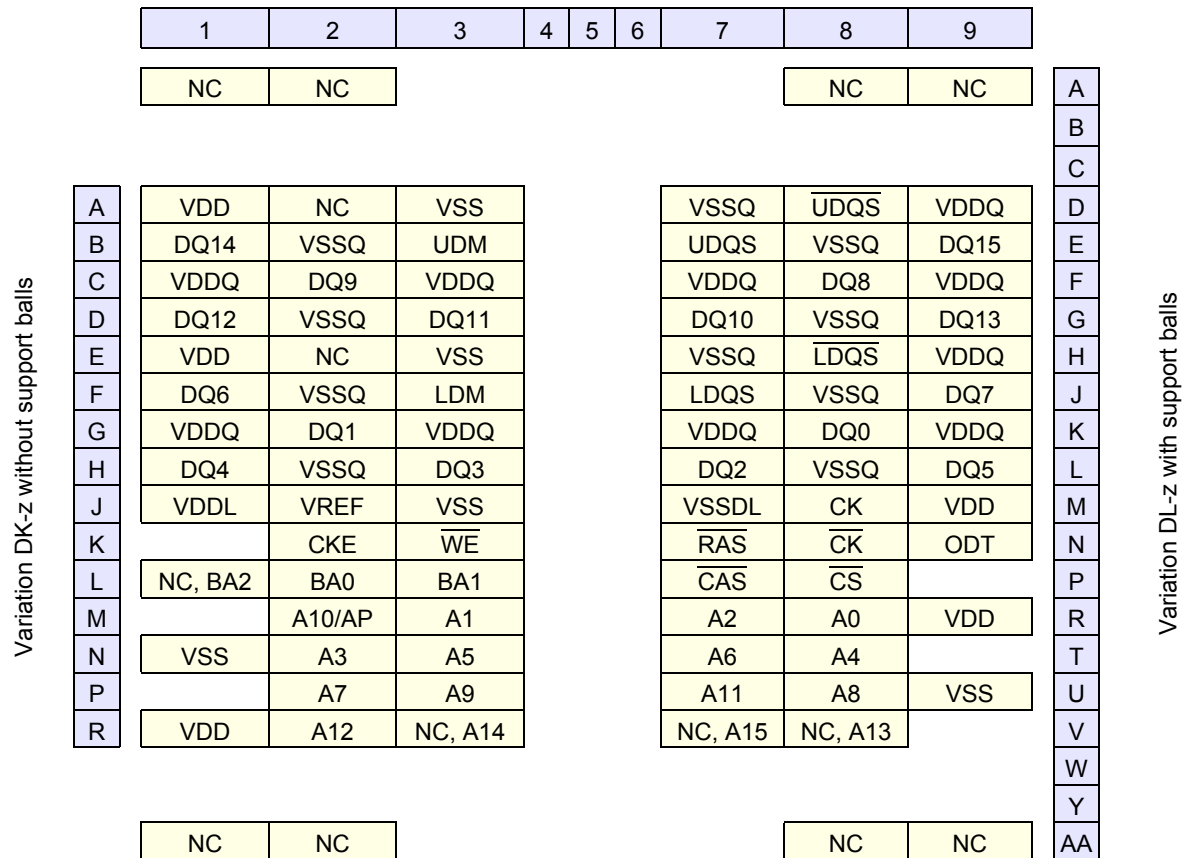


Figure 2 — DDR2 SDRAM x8 ballout using MO-207

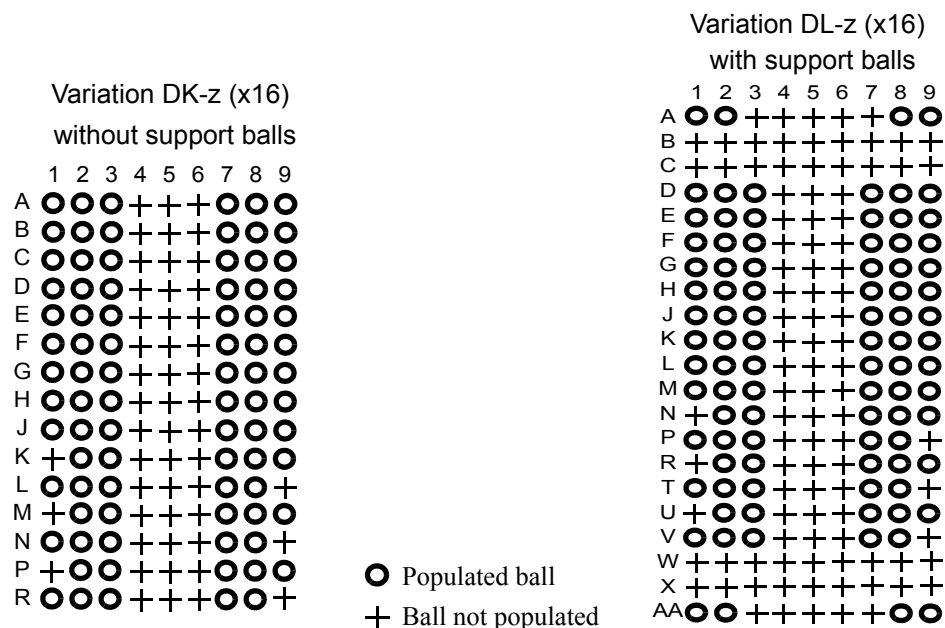


2 Package ballout & addressing (cont'd)**2.1 DDR2 SDRAM package ballout (cont'd)**

(Top view: see balls through package)



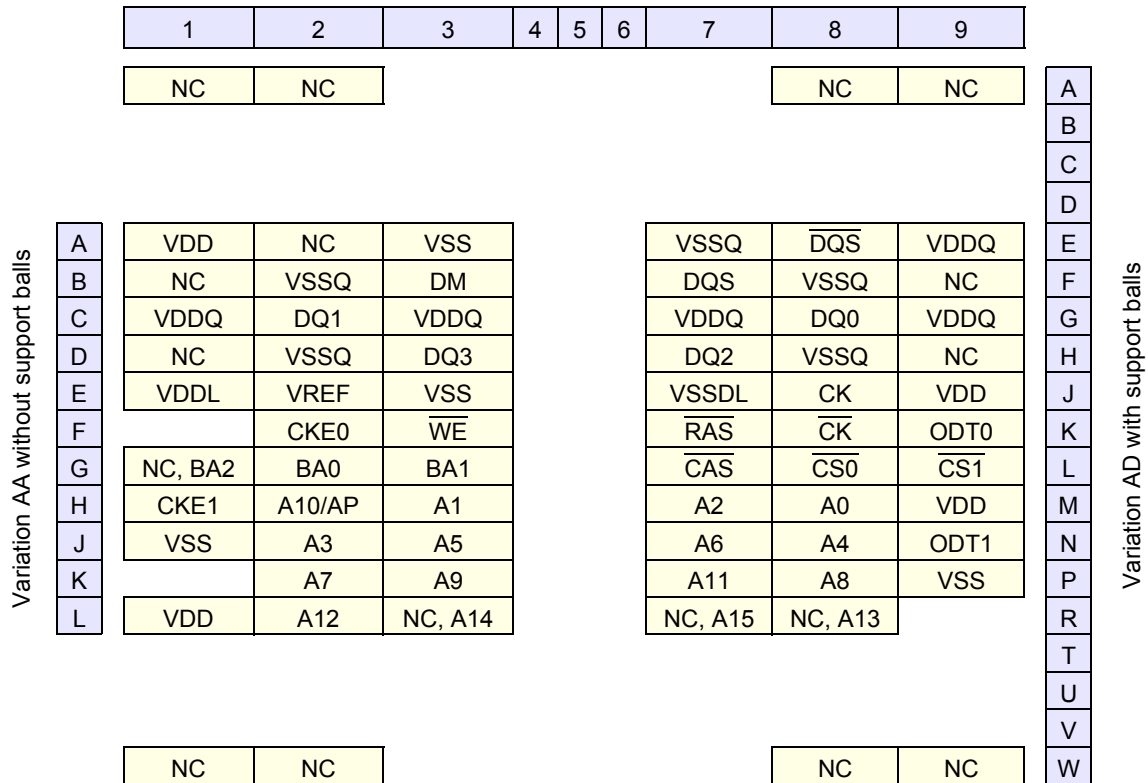
NOTE VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ. However as this is not required, users should refer to vendor data sheet for actual implementation information.

**Figure 3 — DDR2 SDRAM x16 ballout using MO-207**

2 Package ballout & addressing (cont'd)

2.1 DDR2 SDRAM package ballout (cont'd)

(Top view: see balls through package)



NOTE This stacked ballout is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 7, 8 and 9.

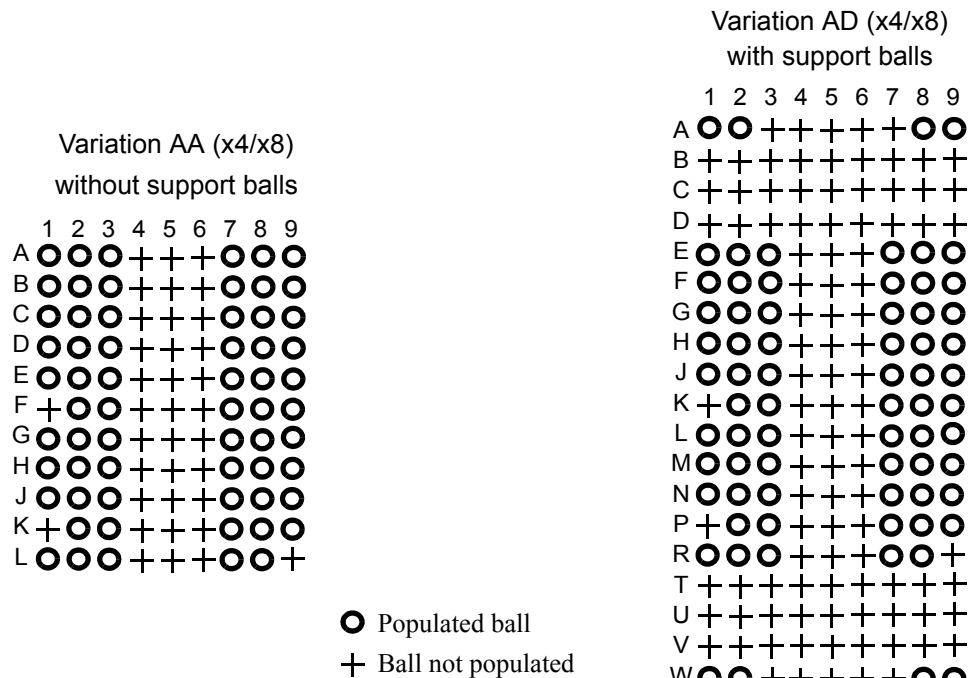
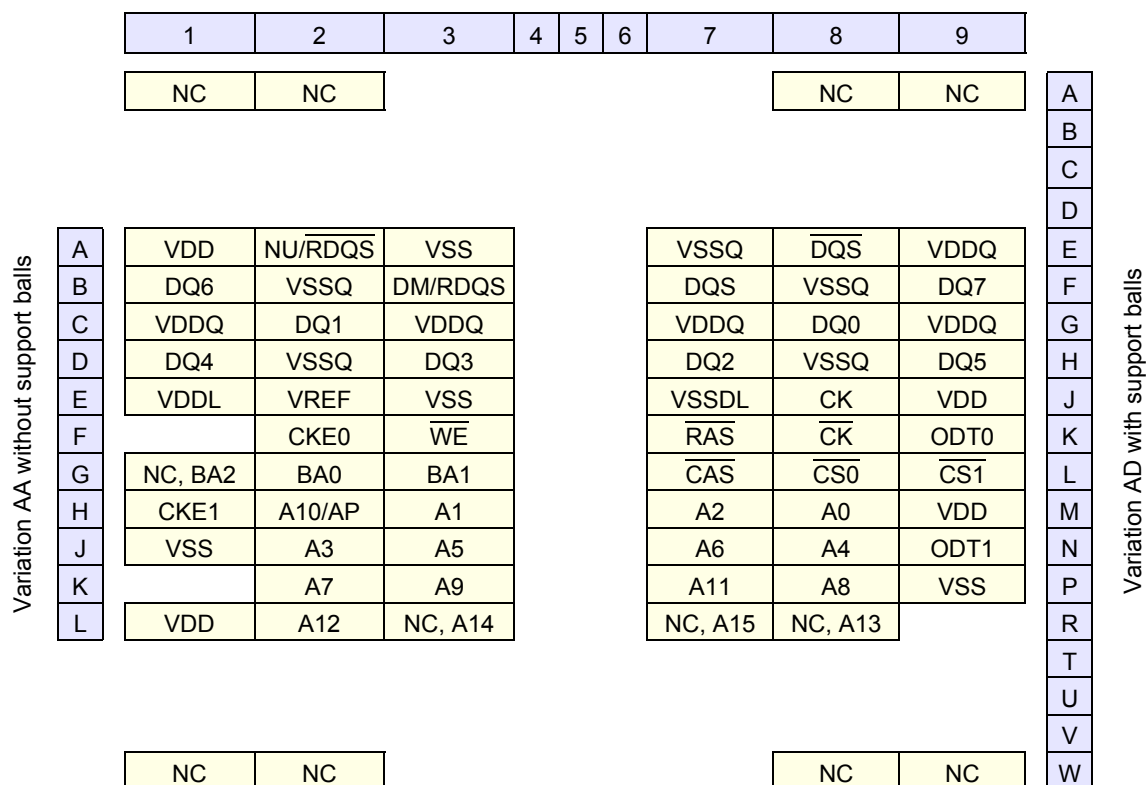


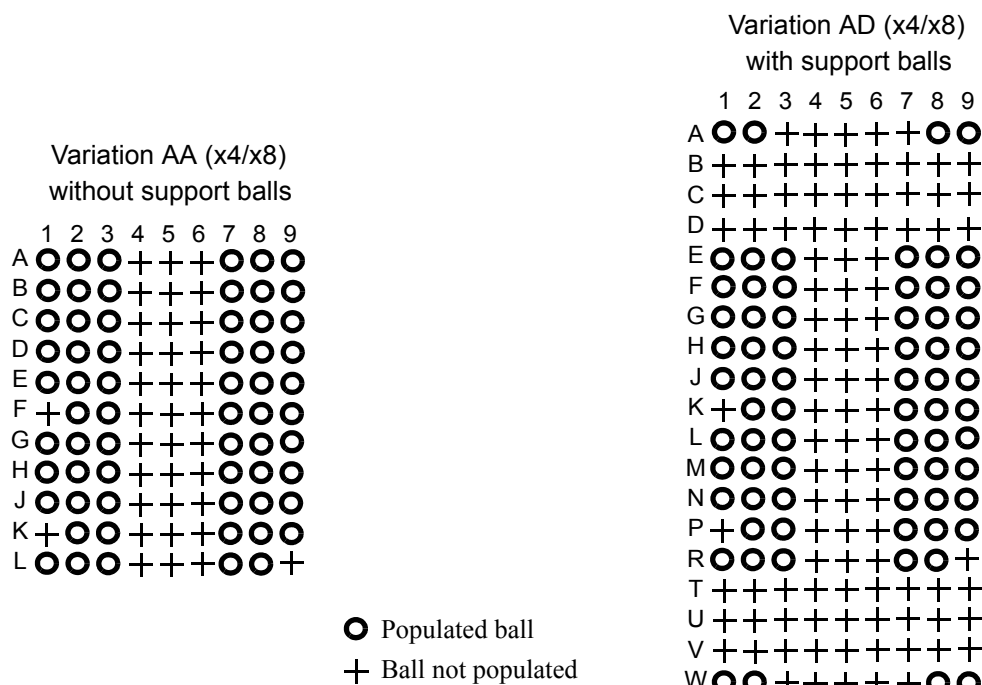
Figure 4 — Stacked/dual-die DDR2 SDRAM x4 ballout using MC 242

2 Package ballout & addressing (cont'd)**2.1 DDR2 SDRAM package ballout (cont'd)**

(Top view: see balls through package)



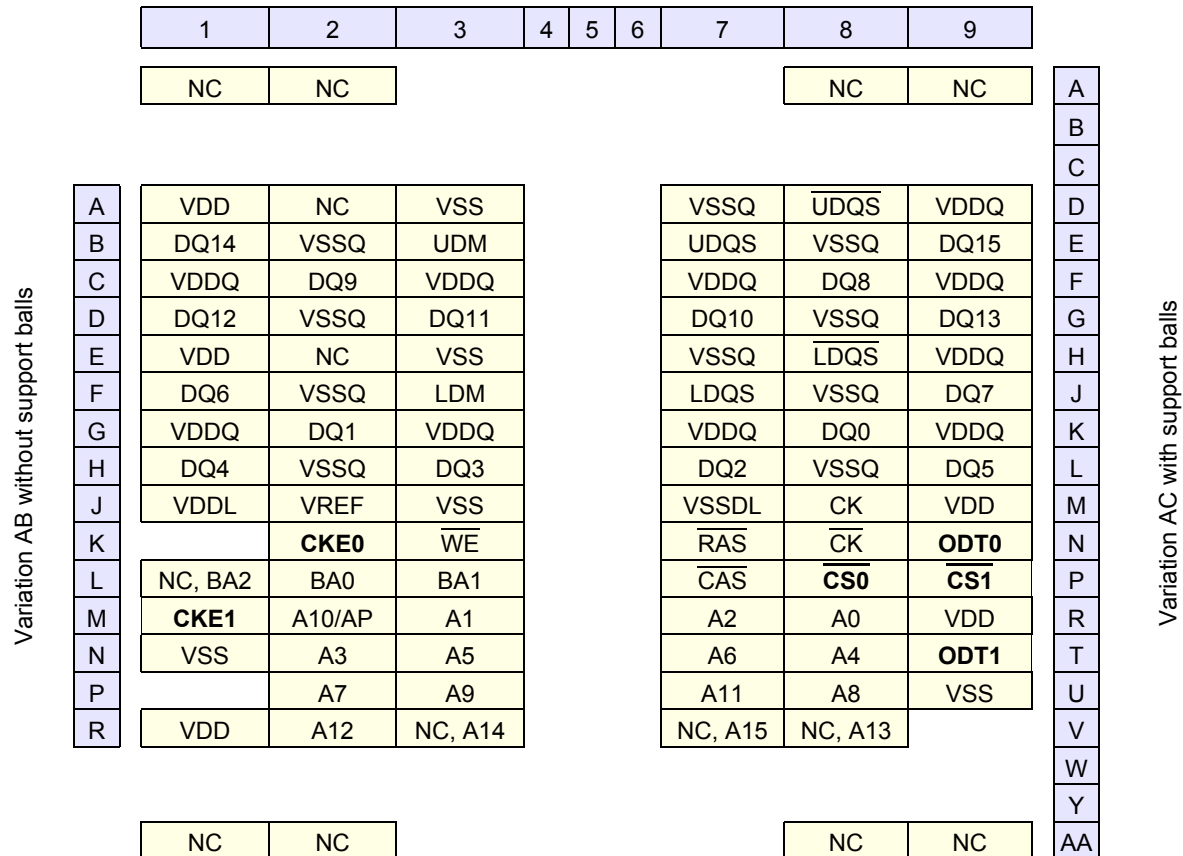
NOTE This stacked ballout is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 7, 8 and 9.

**Figure 5 — Stacked/dual-die DDR2 SDRAM x8 ballout using MO-2/2**

2 Package ballout & addressing (cont'd)

2.1 DDR2 SDRAM package ballout (cont'd)

(Top view: see balls through package)



NOTE This stacked ballout is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 7, 8 and 9.

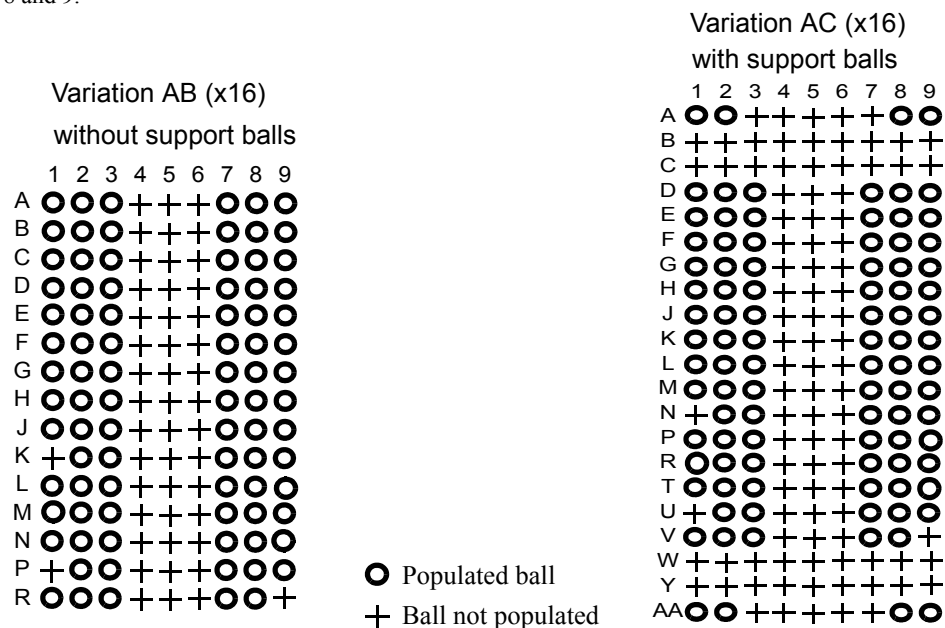
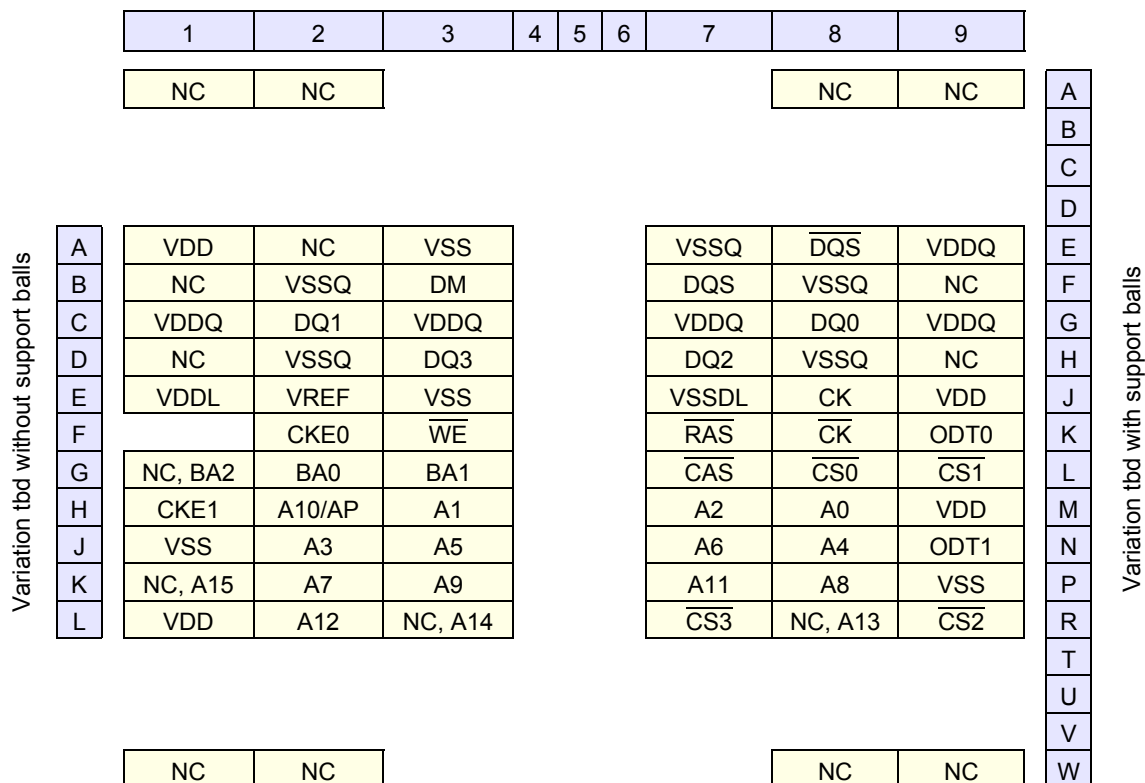


Figure 6 — Stacked/dual-die DDR2 SDRAM x16 ballout using MD 24

2 Package ballout & addressing (cont'd)

2.1 DDR2 SDRAM package ballout (cont'd)

(Top view: see balls through package)



NOTE This stacked ballot is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 7, 8 and 9.

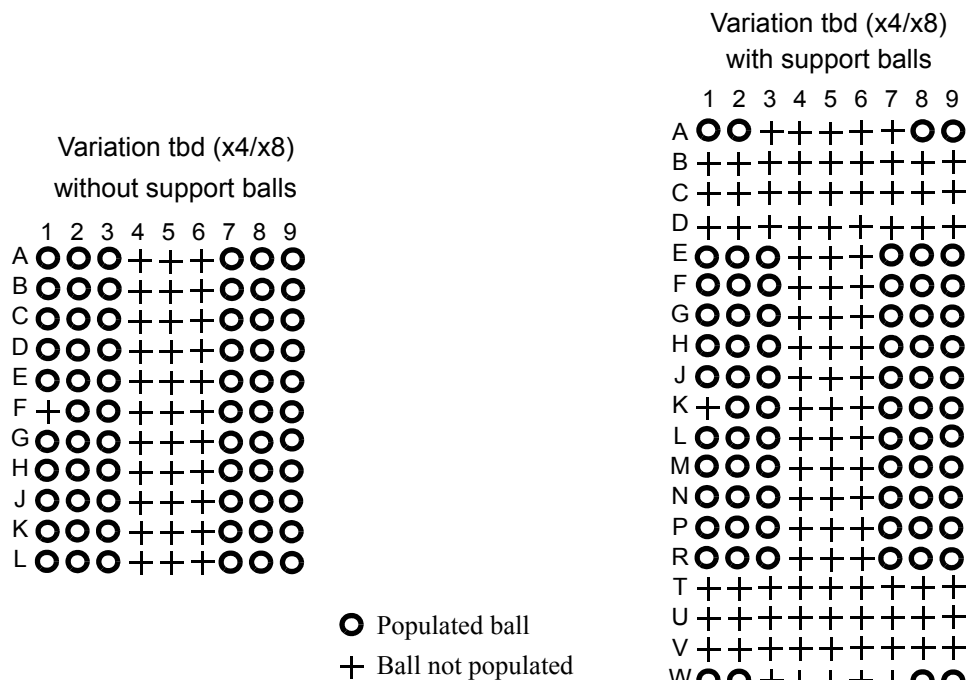
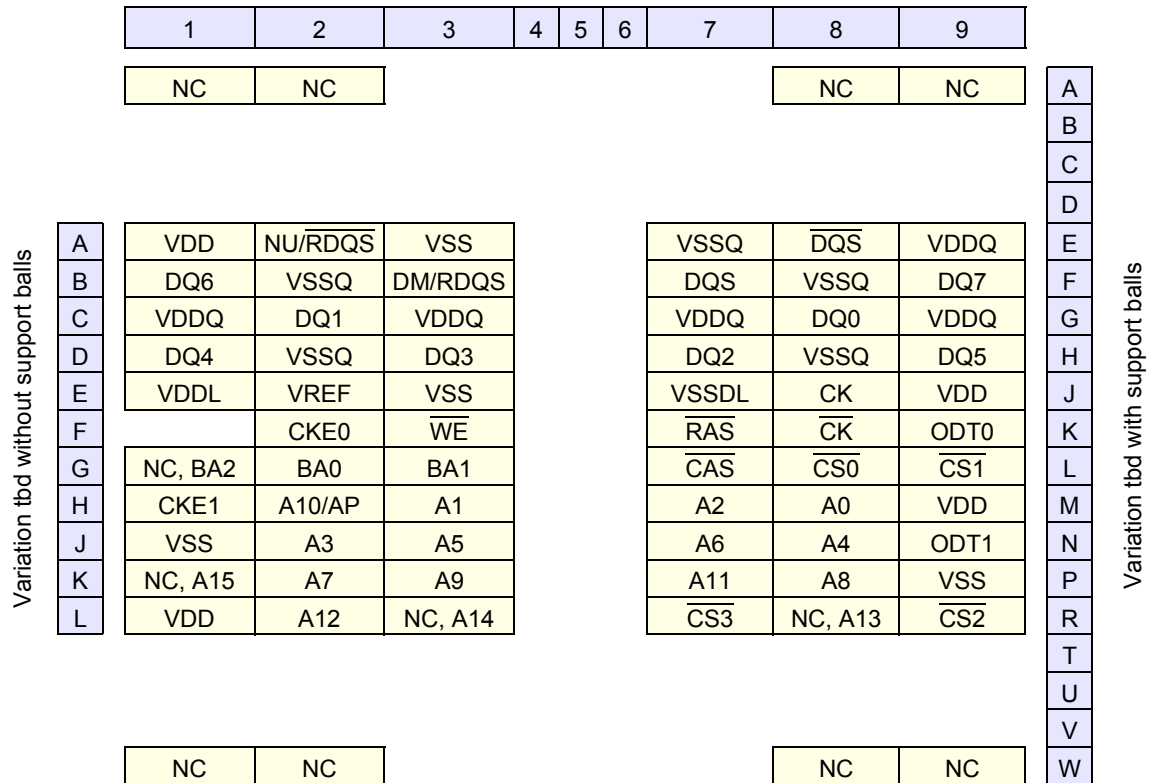


Figure 7 — Quad-stacked/quad-die DDR2 SDRAM x4 ballout using MC-242

2 Package ballout & addressing (cont'd)

2.1 DDR2 SDRAM package ballout (cont'd)

(Top view: see balls through package)



NOTE This stacked ballout is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 7, 8 and 9.

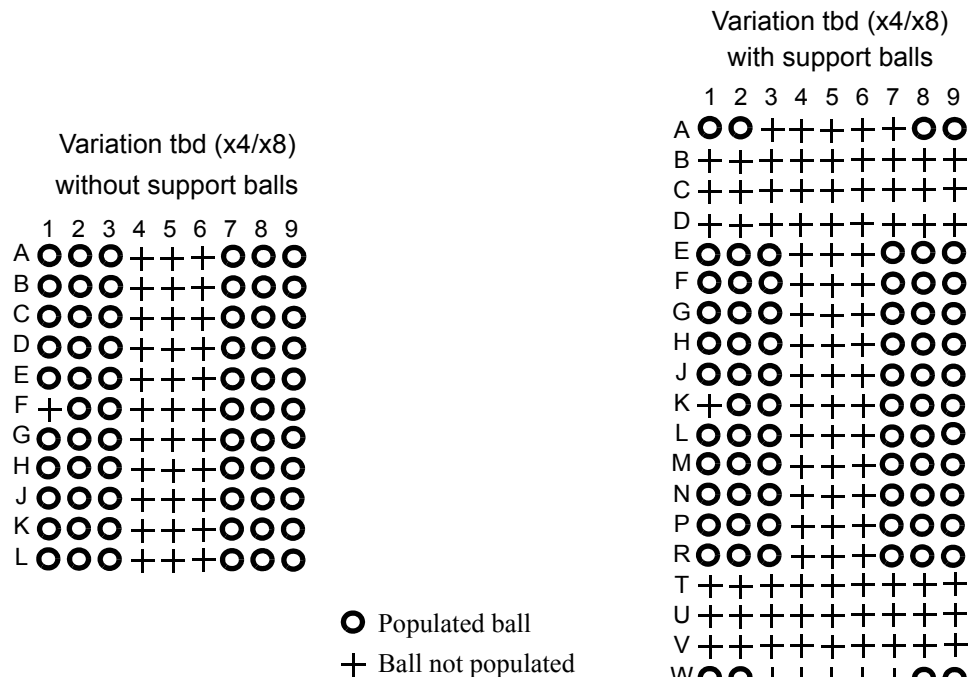
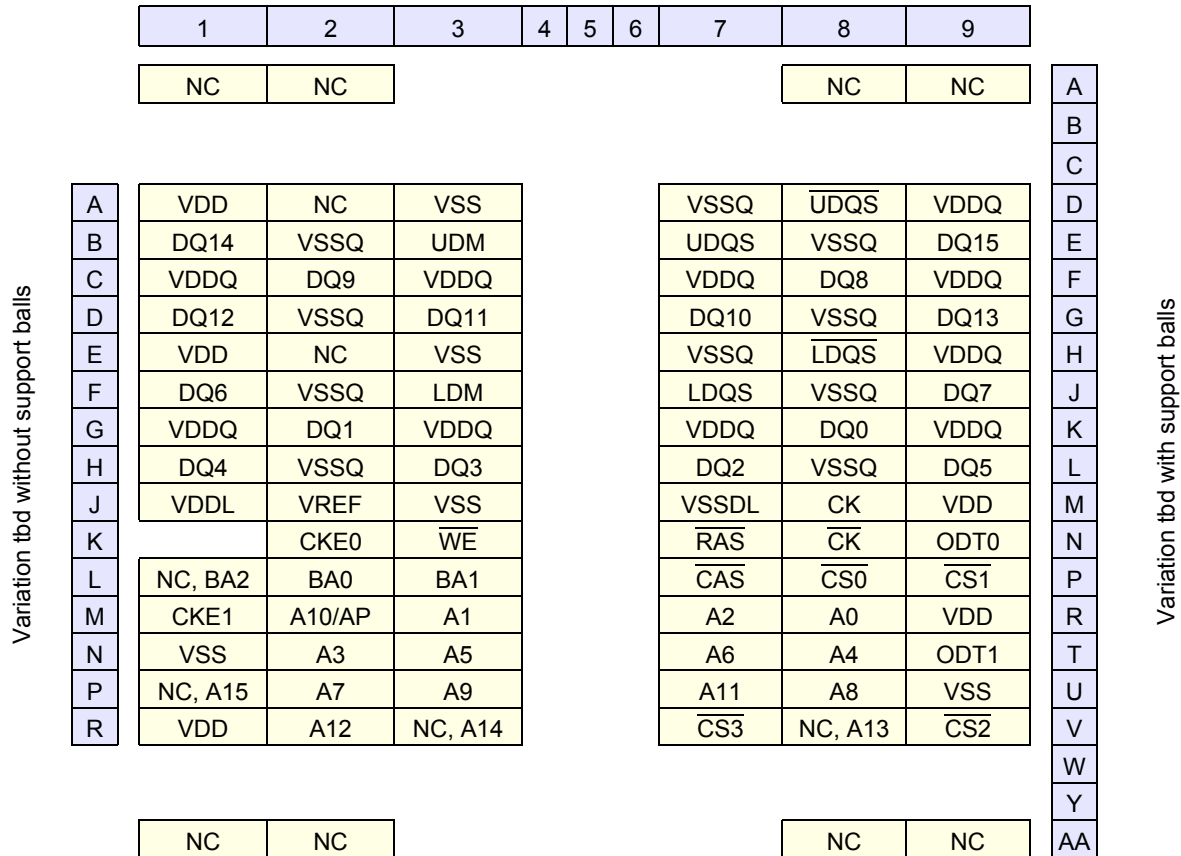


Figure 8 — Quad-stacked/quad-die DDR2 SDRAM x8 ballout using JMC-242

2 Package ballout & addressing (cont'd)

2.1 DDR2 SDRAM package ballout (cont'd)

(Top view: see balls through package)



NOTE This stacked ballout is intended for use only in stacked packages, and does not apply to any non-stacked package. This document (JESD79-2) focuses on non-stacked single-die devices with a few exceptions like the stacked ballout diagrams in Figures 4, 5, 7, 8 and 9.

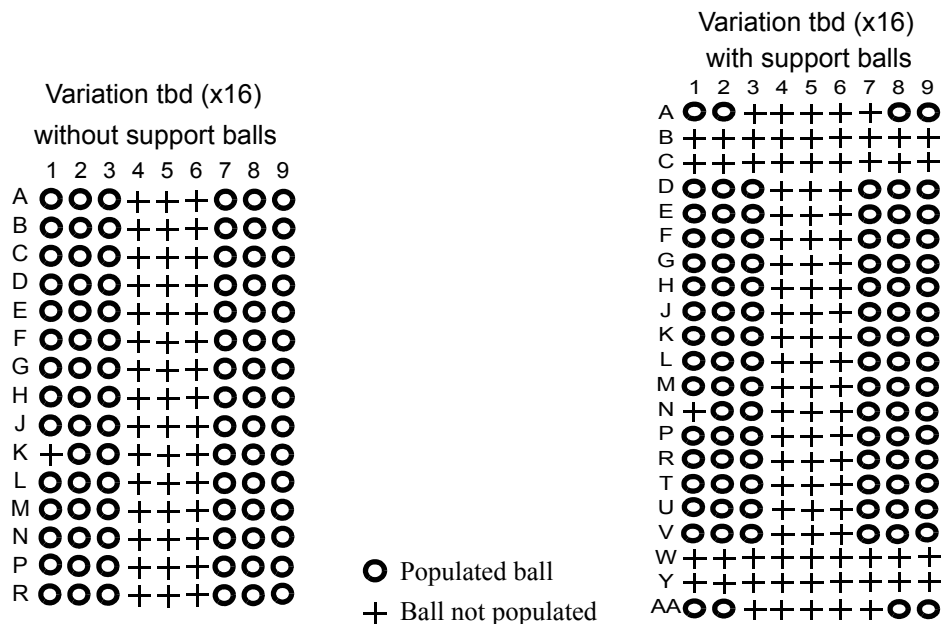


Figure 9 — Quad-stacked/quad-die DDR2 SDRAM x16 ballout using MC 242

2 Package ballout & addressing (cont'd)

2.2 Quad-stacked/quad-die DDR2 SDRAM internal rank associations

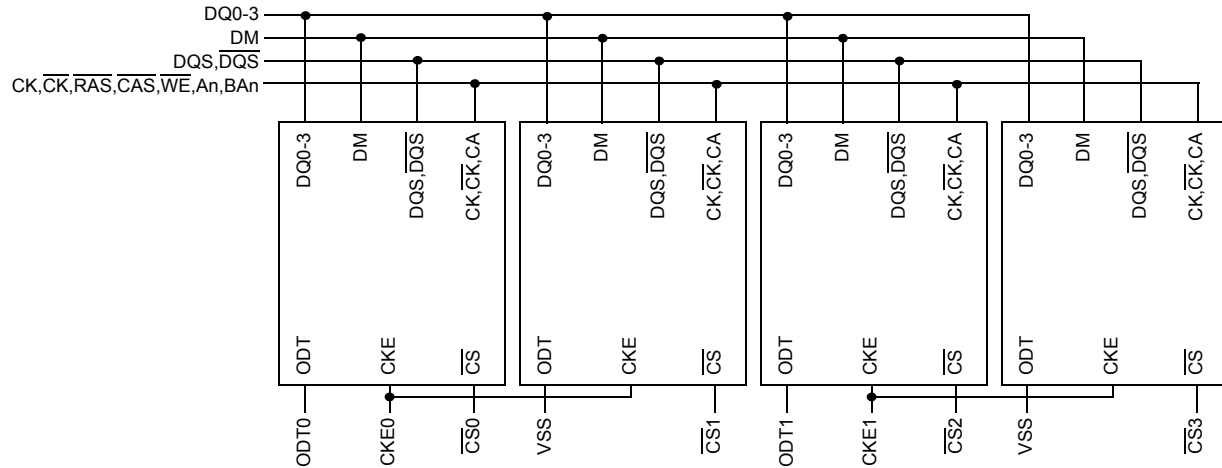


Figure 10 — Quad-stacked/quad-die DDR2 SDRAM x4 rank association

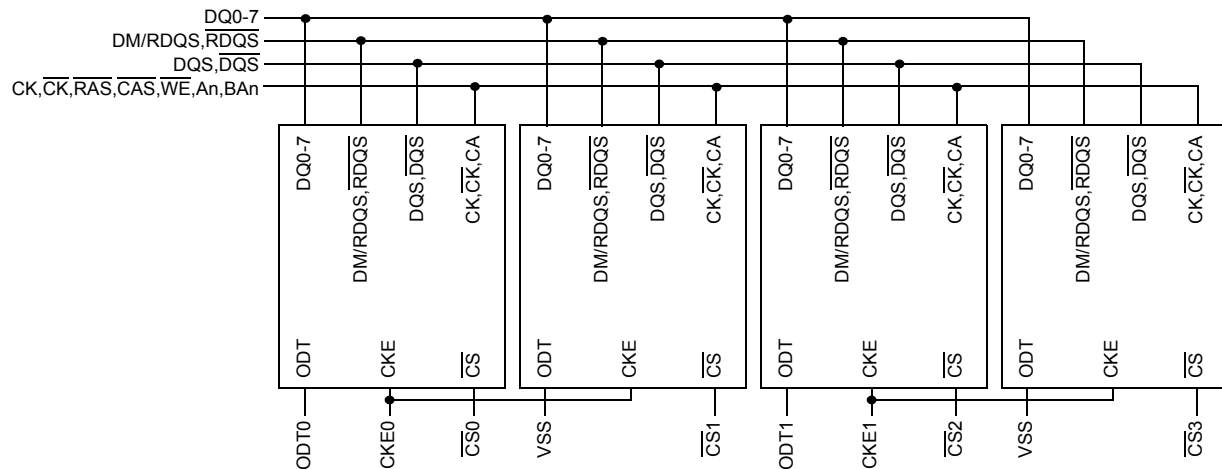


Figure 11 — Quad-stacked/quad-die DDR2 SDRAM x8 rank association

2 Package ballout & addressing (cont'd)

2.2 Quad-stacked/quad-die DDR2 SDRAM internal rank associations (cont'd)

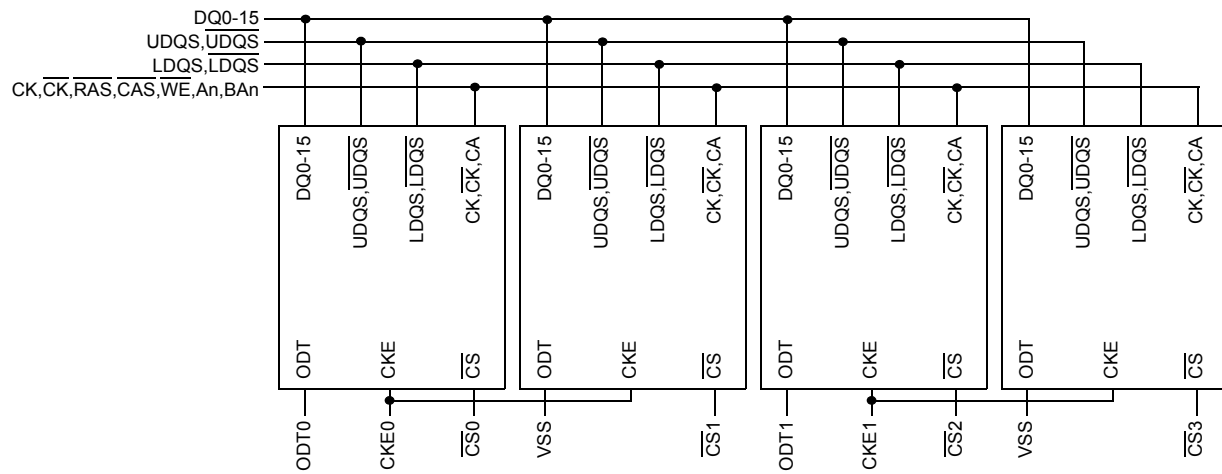


Figure 12 — Quad-stacked/quad-die DDR2 SDRAM x16 rank association

2 Package ballout & addressing (cont'd)

2.3 Input/output functional description

Table 1 — Ball descriptions

Symbol	Type	Function
CK, $\overline{\text{CK}}$	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to the crossings of CK and $\overline{\text{CK}}$ (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates, internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, $\overline{\text{CK}}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{\text{CS}}$	Input	Chip Select: All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external Rank selection on systems with multiple Ranks. $\overline{\text{CS}}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$, and DM signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/ $\overline{\text{UDQS}}$, LDQS/ $\overline{\text{LDQS}}$, UDM, and LDM signal. The ODT pin will be ignored if the EMR(1) is programmed to disable ODT.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
DM (UDM), (LDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/ $\overline{\text{RDQS}}$ is enabled by EMRS command to EMR(1).
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied (For 256Mb and 512Mb, BA2 is not applied). Bank address also determines if the mode register or one of the extended mode registers is to be accessed during a MRS or EMRS command cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0 - BA2. The address inputs also provide the op-code during MRS or EMRS commands.
DQ	Input/Output	Data Input/ Output: Bi-directional data bus.
DQS, $\overline{\text{DQS}}$ (UDQS), ($\overline{\text{UDQS}}$) (LDQS), ($\overline{\text{LDQS}}$) (RDQS), ($\overline{\text{RDQS}}$)	Input/Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMR(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals $\overline{\text{DQS}}$, $\overline{\text{LDQS}}$, $\overline{\text{UDQS}}$, and $\overline{\text{RDQS}}$ to provide differential pair signaling to the system during both reads and writes. A control bit at EMR(1)[A10] enables or disables all complementary data strobe signals. In this data sheet, "differential DQS signals" refers to any of the following with EMR(1)[A10] = 0 x4 DQS/$\overline{\text{DQS}}$ x8 DQS/$\overline{\text{DQS}}$ if EMR(1)[A11] = 0 x8 DQS/$\overline{\text{DQS}}$, RDQS/$\overline{\text{RDQS}}$, if EMR(1)[A11] = 1 x16 LDQS/$\overline{\text{LDQS}}$ and UDQS/$\overline{\text{UDQS}}$ "single-ended DQS signals" refers to any of the following with EMR(1)[A10] = 1 x4 DQS x8 DQS if EMR(1)[A11] = 0 x8 DQS, RDQS, if EMR(1)[A11] = 1 x16 LDQS and UDQS
NC		No Connect: No internal electrical connection is present.
V _{DDQ}	Supply	DQ Power Supply: 1.8 V +/- 0.1 V
V _{SSQ}	Supply	DQ Ground

2 Package ballout & addressing (cont'd)

2.3 Input/output functional description (cont'd)

Table 1 — Ball descriptions (cont'd)

Symbol	Type	Function
V _{DDL}	Supply	DLL Power Supply: 1.8 V +/- 0.1 V
V _{SSDL}	Supply	DLL Ground
V _{DD}	Supply	Power Supply: 1.8 V +/- 0.1 V
V _{SS}	Supply	Ground
V _{REF}	Supply	Reference voltage

2.4 DDR2 SDRAM addressing

Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

$$\text{page size} = 2^{\text{COLBITS}} \times \text{ORG} \div 8$$

where

COLBITS = the number of column address bits

ORG = the number of I/O (DQ) bits

Table 2 — 128 Mb Addressing

Configuration	32 Mb x4	16 Mb x 8	8 Mb x16
# of Bank	N/A	N/A	4
Bank Address	N/A	N/A	BA0 - BA1
Auto precharge	N/A	N/A	A10/AP
Row Address	N/A	N/A	A0 - A11 ^{Note1}
Column Address	N/A	N/A	A0 - A8
Page size	N/A	N/A	1 KB
Note1 : A12 is not used in Addressing but must be maintained in package ballout and supporting MR/EMR(#) functionality			

Table 3 — 256 Mb addressing

Configuration	64 Mb x 4	32 Mb x 8	16 Mb x 16
# of Banks	4	4	4
Bank Address	BA0, BA1	BA0, BA1	BA0, BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A12	A0 - A12	A0 - A12
Column Address	A0 - A9, A11	A0 - A9	A0 - A8
Page size	1 KB	1 KB	1 KB

Table 4 — 512 Mb addressing

Configuration	128 Mb x 4	64 Mb x 8	32 Mb x 16
# of Banks	4	4	4
Bank Address	BA0, BA1	BA0, BA1	BA0, BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A13	A0 - A13	A0 - A12
Column Address	A0 - A9, A11	A0 - A9	A0 - A8
Page size	1 KB	1 KB	2 KB

2 Package ballout & addressing (cont'd)

2.4 DDR2 SDRAM addressing (cont'd)

Table 5 — 1 Gb addressing

Configuration	256 Mb x 4	128 Mb x 8	64 Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A13	A0 - A13	A0 - A12
Column Address	A0 - A9, A11	A0 - A9	A0 - A9
Page size	1 KB	1 KB	2 KB

Table 6 — 2 Gb addressing

Configuration	512 Mb x 4	256 Mb x 8	128 Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A14	A0 - A14	A0 - A13
Column Address	A0 - A9, A11	A0 - A9	A0 - A9
Page size	1 KB	1 KB	2 KB

Table 7 — 4 Gb addressing

Configuration	1 Gb x 4	512 Mb x 8	256 Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A15	A0 - A15	A0 - A14
Column Address	A0 - A9, A11	A0 - A9	A0 - A9
Page size	1 KB	1 KB	2 KB

3 Functional Description

3.1 Simplified state diagram

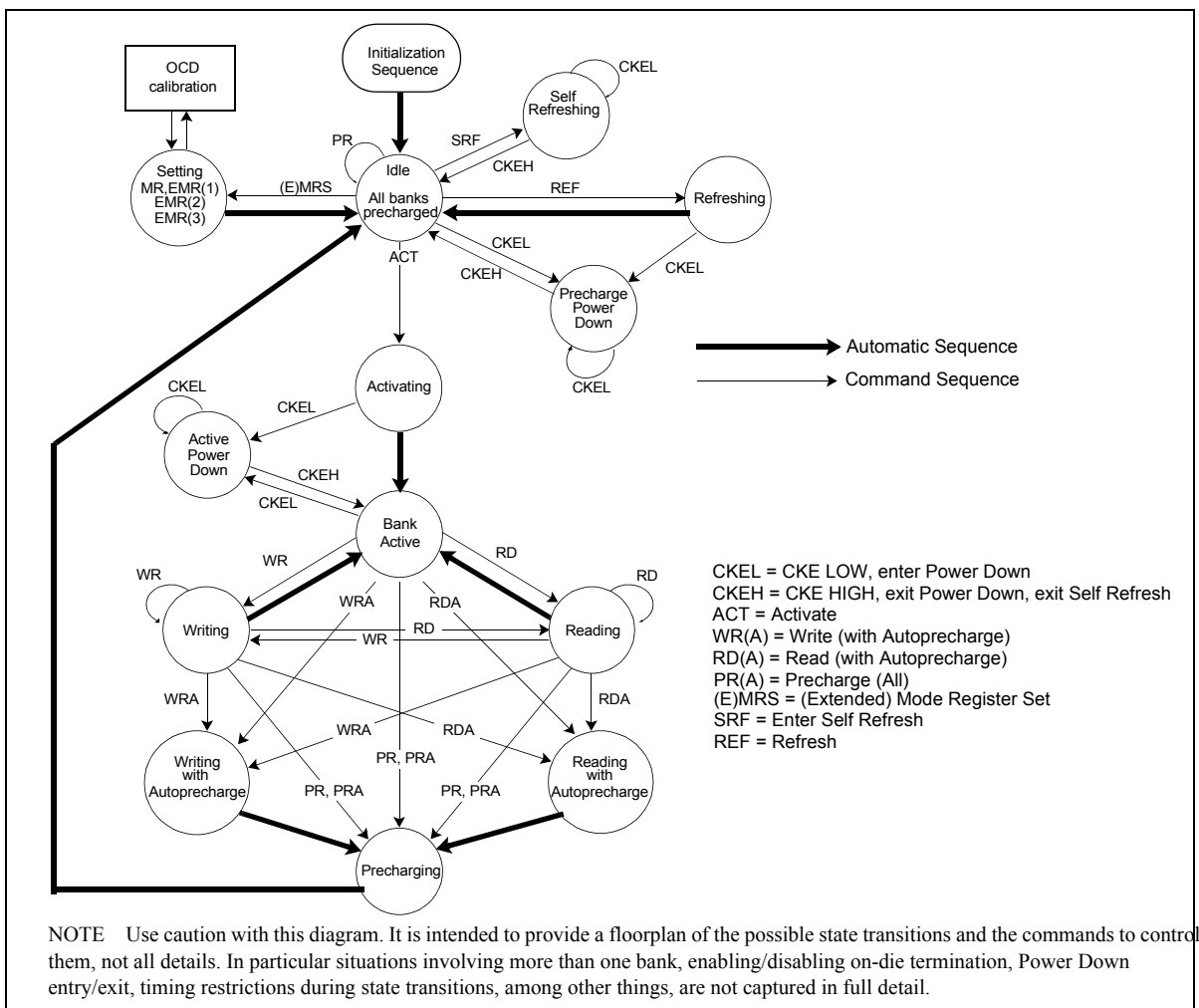


Figure 13 — DDR2 SDRAM simplified state diagram

3.2 Basic functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

3.3 Power-up and initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

For DDR2 SDRAMs, both bits BA0 and BA1 must be decoded for Mode/Extended Mode Register Set (MRS/EMRS) commands. Users must initialize all four Mode Registers. The registers may be initialized in any order.

3 Functional Description (cont'd)

3.3 Power-up and initialization (cont'd)

3.3.1 Power-up and initialization sequence

The following sequence is required for Power-up and Initialization.

a) Either one of the following sequence is required for Power-up.

a1) While applying power, attempt to maintain CKE below $0.2 \times VDDQ$ and ODT^{*1} at a LOW state (all other inputs may be undefined.) The VDD voltage ramp time must be no greater than 200 ms from when VDD ramps from 300 mV to VDD min; and during the VDD voltage ramp, $|VDD - VDDQ| \leq 0.3$ volts. Once the ramping of the supply voltages is complete (when VDDQ crosses VDDQ min), the supply voltage specifications provided in section 6, Table 17 Recommended DC operating conditions (SSTL_1.8), prevail.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2, VREF must be within +/- 300 mV with respect to VDDQ/2 during supply ramp time.
- VDDQ $\geq$ VREF must be met at all times.

a2) While applying power, attempt to maintain CKE below $0.2 \times VDDQ$ and ODT^{*1} at a LOW state, all other inputs may be undefined, voltage levels at I/Os and outputs must be less than VDDQ during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, $VDD \geq VDDL \geq VDDQ$ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete, which is when VDDQ crosses VDDQ min. Once the ramping of the supply voltages is complete, the supply voltage specifications provided in section 6, Table 17 Recommended DC operating conditions (SSTL_1.8), prevail.

- Apply VDD/VDDL before or at the same time as VDDQ.
- VDD/VDDL voltage ramp time must be no greater than 200 ms from when VDD ramps from 300 mV to VDD min
- Apply VDDQ before or at the same time as VTT.
- The VDDQ voltage ramp time from when VDD min is achieved on VDD to when VDDQ min is achieved on VDDQ must be no greater than 500 ms.
(Note: While VDD is ramping, current may be supplied from VDD through the DRAM to VDDQ.)
- Vref must track VDDQ/2, Vref must be within +/- 300 mv with respect to VDDQ/2 during supply ramp time.
- VDDQ $\geq$ VREF must be met at all times.
- Apply VTT.
- The VTT voltage ramp time from when VDDQ min is achieved on VDDQ to when VTT min is achieved on VTT must be no greater than 500 ms.

b) Start clock and maintain stable condition.

c) For the minimum of 200 us after stable power (VDD, VDDL, VDDQ, VREF and VTT are between their minimum and maximum values as stated in section 6, Table 17 Recommended DC operating conditions (SSTL_1.8)) and stable clock (CK, $\overline{CK}$), then apply NOP or Deselect & take CKE HIGH.

d) Wait minimum of 400 ns then issue precharge all command. NOP or Deselect applied during 400 ns period.

e) Issue an EMRS command to EMR(2). (To issue EMRS command to EMR(2), provide LOW to BA0 and BA2, HIGH to BA1.)

f) Issue an EMRS command to EMR(3). (To issue EMRS command to EMR(3), provide LOW to BA2, HIGH to BA0 and BA1.)

g) Issue EMRS to enable DLL. (To issue DLL Enable command, provide LOW to A0, HIGH to BA0 and LOW to BA1-BA2 and A13-A15. And A9=A8=A7=LOW must be used when issuing this command.)

h) Issue a Mode Register Set command for DLL reset.

(To issue DLL Reset command, provide HIGH to A8 and LOW to BA0-BA2, and A13-A15.)

i) Issue a precharge all command.

j) Issue 2 or more auto-refresh commands.

k) Issue a MRS command with LOW to A8 to initialize device operation. (i.e. to program operating parameters.)

3.3 Power-up and initialization (cont'd)

3.3.1 Power-up and initialization sequence (cont'd)

without resetting the DLL.)

- l) At least 200 clocks after step h, execute OCD Calibration (Off Chip Driver impedance adjustment).
If OCD calibration is not used, EMRS to EMR(1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR(1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).
- m) The DDR2 SDRAM is now ready for normal operation.

*1: To guarantee ODT off, VREF must be valid and a LOW level must be applied to the ODT pin.

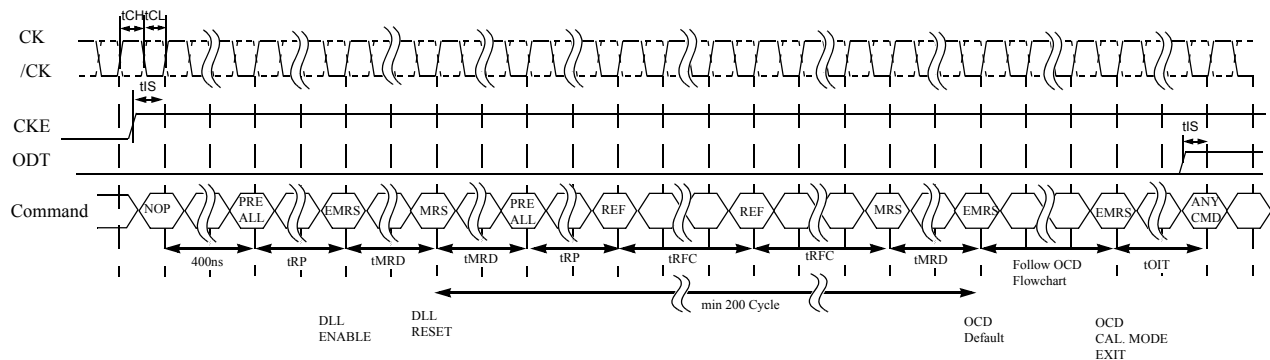


Figure 14 — Initialization sequence after power-up

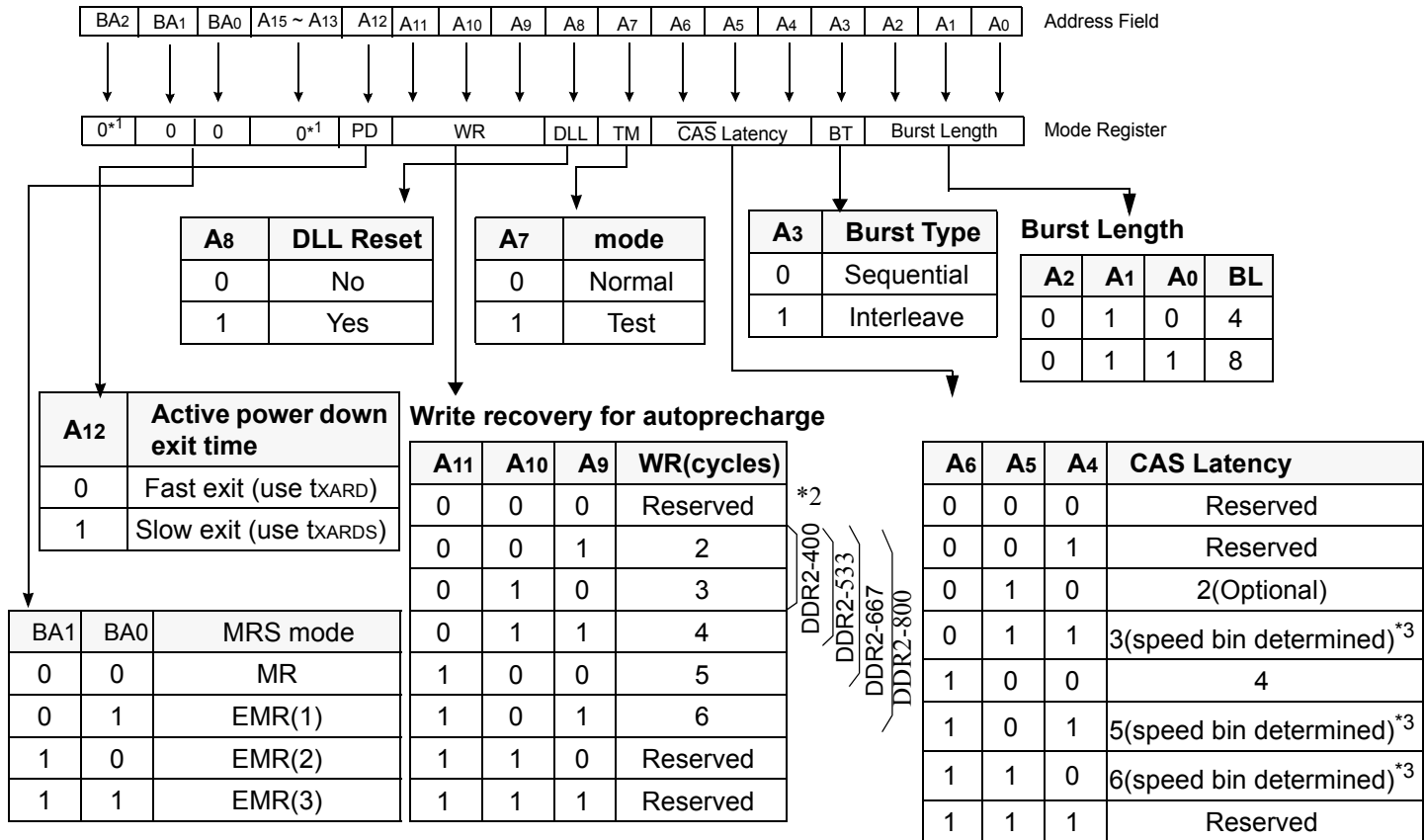
3.4 Programming the mode and extended mode registers

For application flexibility, burst length, burst type, $\overline{\text{CAS}}$ latency, DLL reset function, write recovery time (WR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT (On Die Termination), single-ended strobe, and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers (EMR(#)) can be altered by re-executing the MRS or EMRS Commands. Even if the user chooses to modify only a subset of the MR or EMR(#) variables, all variables within the addressed register must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means re-initialization including those can be executed at any time after power-up without affecting array contents.

3.4.1 DDR2 SDRAM mode register (MR)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls $\overline{\text{CAS}}$ latency, burst length, burst sequence, test mode, DLL reset, WR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be programmed during initialization for proper operation. The mode register is written by asserting LOW on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, BA0 and BA1, while controlling the state of address pins A0 - A15. The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 - A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, $\overline{\text{CAS}}$ latency is defined by A4 - A6. The DDR2 does not support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to LOW for normal MRS operation. Write recovery time WR is defined by A9 - A11. Refer to the mode for specific codes.

3.4 Programming the mode and extended mode registers (cont'd)**3.4.1 DDR2 SDRAM mode register (MR) (cont'd)**

NOTE 1 BA2 and A13-A15 are reserved for future use and must be set to 0 when programming the MR.

NOTE 2 For DDR2-400/533, WR (write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR[cycles] = RU { tWR[ns] / tCK[ns] }, where RU stands for round up). For DDR2-667/800, WR min is determined by tCK(avg) max and WR max is determined by tCK(avg) min. WR[cycles] = RU { tWR[ns] / tCK(avg)[ns] }, where RU stands for round up. The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

NOTE 3 Speed bin determined. Not required on all speed bins.

Figure 15 — DDR2 SDRAM mode register set (MRS)

3.4.2 DDR2 SDRAM extended mode registers (EMR(#))**3.4.2.1 EMR(1)**

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, DQS disable, OCD program, RDQS enable. The default value of the extended mode register(1) is not defined, therefore the extended mode register(1) must be programmed during initialization for proper operation. The extended mode register(1) is written by asserting LOW on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, HIGH on BA0 and LOW on BA1, while controlling the states of address pins A0 - A15. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the extended mode register(1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(1). Extended mode register(1) contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a reduced strength output driver. A3 - A5 determines the additive latency, A7 - A9 are used for OCD control. A10 is used for DQS disable and A11 is used for RDQS enable. A2 and A6 are used for ODT setting.

3.4 Programming the mode and extended mode registers (cont'd)

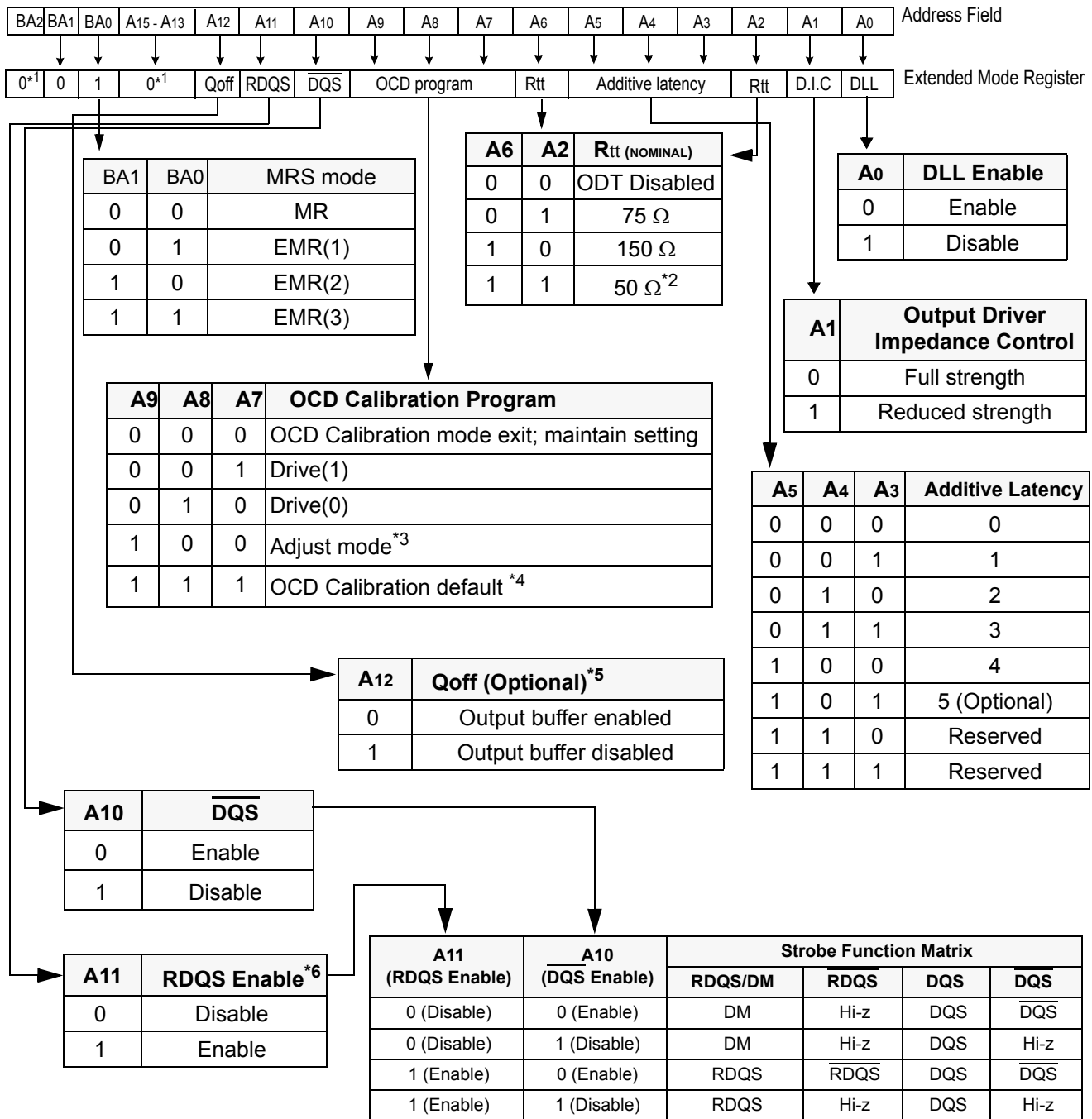
3.4.2 DDR2 SDRAM extended mode registers (EMR(#)) (cont'd)

3.4.2.2 DLL enable/disable

The DLL must be enabled for normal operation. DLL enable is required during power-up and initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

3.4.2.3 EMR(1) programming

Figure 16 shows the EMR(1) programming.

3.4.2 DDR2 SDRAM extended mode registers (EMR(#)) (cont'd)**3.4.2.3 EMR(1) programming (cont'd)**

NOTE 1 BA2 and A13-A15 are reserved for future use and must be set to 0 when programming the EMR(1).

NOTE 2 Optional for DDR2-400/533/667, mandatory for DDR2-800.

NOTE 3 When Adjust mode is issued, AL from previously set value must be applied.

NOTE 4 After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000. Refer to section 3.4.3 for detailed information.

NOTE 5 Output disabled - DQs, DQSs, $\overline{DQS}$ s, RDQS, $\overline{RDQS}$. This feature is used in conjunction with DIMM IDD measurements when IDDQ is not desired to be included.

NOTE 6 If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

Figure 16 — EMR(1) programming

3.4 Programming the mode and extended mode registers (cont'd)

3.4.2 DDR2 SDRAM extended mode registers (EMR(#)) (cont'd)

3.4.2.4 EMR(2)

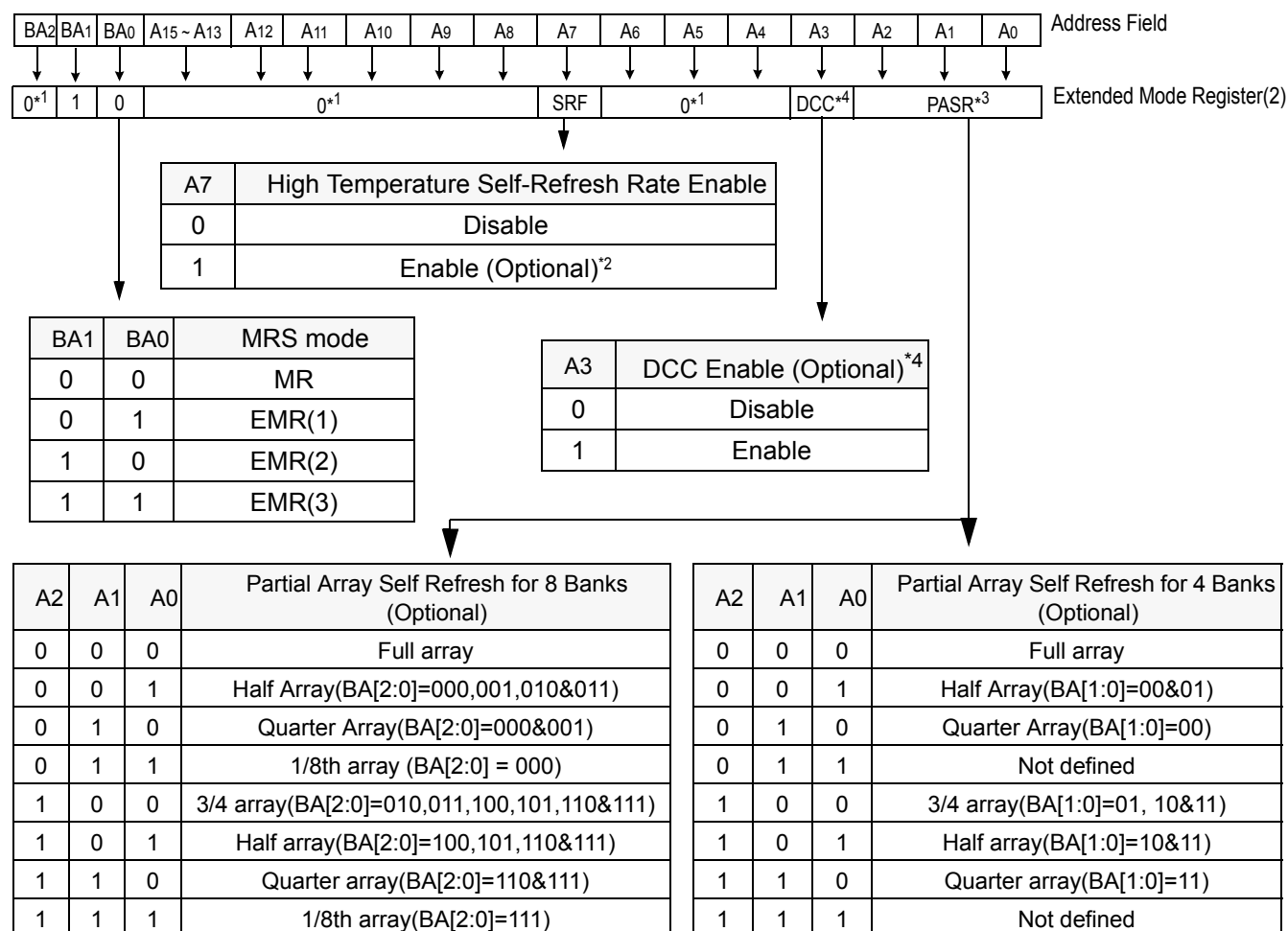
The extended mode register(2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register(2) must be programmed during initialization for proper operation. The extended mode register(2) is written by asserting LOW on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, HIGH on BA1 and LOW on BA0, while controlling the states of address pins A0 - A15. The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the extended mode register(2). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

3.4.2.5 EMR(2) programming

Figure 17 shows the EMR(2) programming.

3.4.2 DDR2 SDRAM extended mode registers (EMR(#)) (cont'd)

3.4.2.5 EMR(2) programming (cont'd)



NOTE 1 BA2 and A4-A6, A8-A15 are reserved for future use and must be set to 0 when programming the EMR(2).

NOTE 2 As industry adoption of high temperature parts proceeds, users need to determine if a DRAM supports High Temperature Self-Refresh Rate Enable mode before attempting to use it in that mode. JEDEC standard DDR2 SDRAM Module user can look at DDR2 SDRAM Module SPD field Byte 49 bit [0]. If the high temperature self-refresh mode is supported then controller can set the EMR(2)[A7] bit to enable the self-refresh rate in case of higher than 85 °C temperature self-refresh operation. For the loose part user, please refer to DRAM Manufacturer's part number and data sheet to check the high temperature self-refresh rate availability.

NOTE 3 Optional in DDR2 SDRAM. If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if self refresh is entered. Data integrity will be maintained if tREF conditions are met and no Self Refresh command is issued. If the PASR feature is not supported, EMR(2)[A0-A2] must be set to 000 when programming EMR(2).

NOTE 4 Optional in DDR2 SDRAM. JEDEC standard DDR2 SDRAM may or may not have DCC (Duty Cycle Corrector) implemented, and in some of the DRAMs implementing DCC, user may be given the controllability of DCC thru EMR(2)[A3] bit. JEDEC standard DDR2 SDRAM users can look at manufacturer's data sheet to check if the DRAM part supports DCC controllability. If Optional DCC Controllability is supported, user may enable or disable the DCC by programming EMR(2)[A3] accordingly. If the controllability feature is not supported, EMR(2)[A3] must be set to 0 when programming EMR(2).

Figure 17 — EMR(2) programming

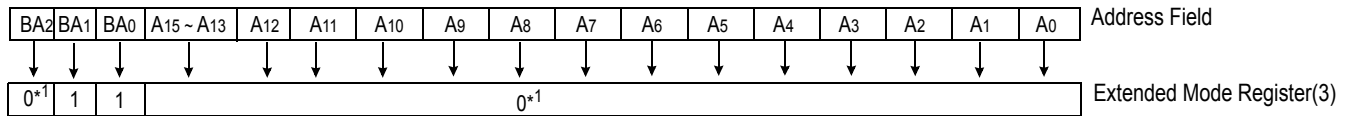
3.4 Programming the mode and extended mode registers (cont'd)

3.4.2 DDR2 SDRAM extended mode registers (EMR(#)) (cont'd)

3.4.2.6 EMR(3)

No function is defined in extended mode register(3). The default value of the extended mode register(3) is not defined, therefore the extended mode register(3) must be programmed during initialization for proper operation.

3.4.2.7 EMR(3) programming



NOTE 1 All bits in EMR(3) except BA0 and BA1 are reserved for future use and must be set to 0 when programming the EMR(3).

Figure 18 — EMR(3) programming

3.4.3 Off-chip driver (OCD) impedance adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart in Figure 19 is an example of sequence. Every calibration mode command should be followed by “OCD calibration mode exit” before any other command being issued. All MR should be programmed before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.

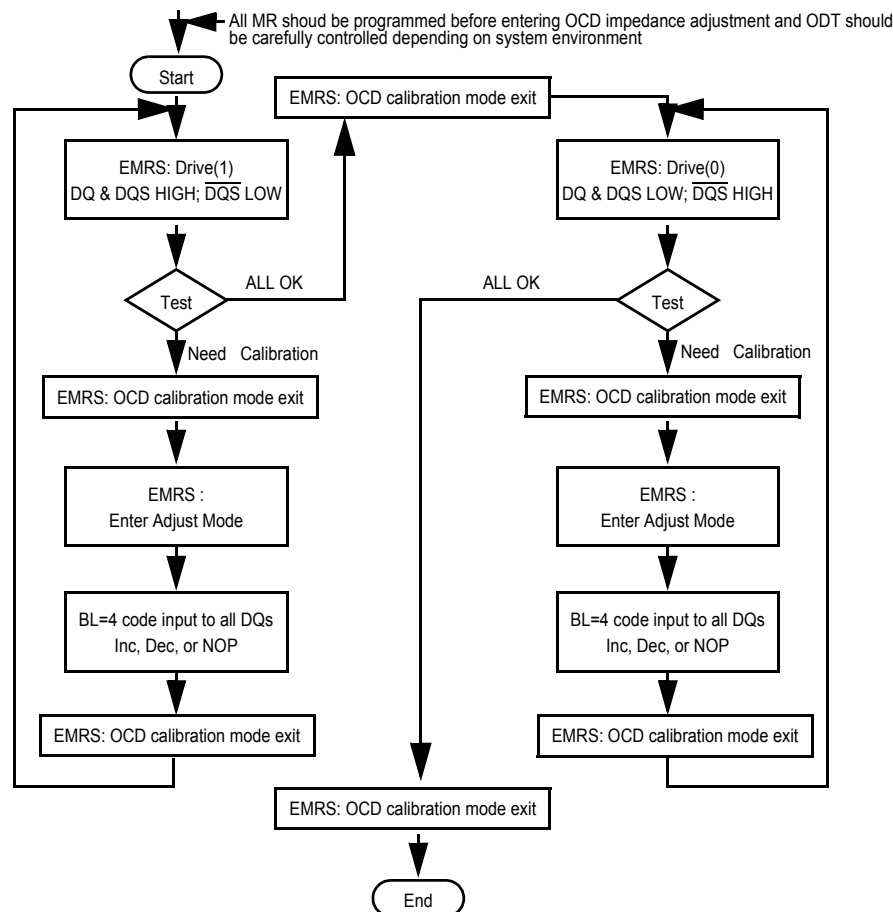


Figure 19 — OCD impedance adjustment

3.4.3.1 Extended mode register for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMR bit enabling RDQS operation. In Drive(1) mode, all

3.4.3 Off-chip driver (OCD) impedance adjustment (cont'd)**3.4.3.1 Extended mode register for OCD impedance adjustment (cont'd)**

DQ, DQS (and RDQS) signals are driven HIGH and all $\overline{\text{DQS}}$ signals are driven LOW. In drive(0) mode, all DQ, DQS (and RDQS) signals are driven LOW and all $\overline{\text{DQS}}$ signals are driven HIGH. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of $18\ \Omega$ during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in Tables 31 and 32. OCD applies only to normal full strength output drive setting defined by EMR(1) and if reduced strength is set, OCD default output driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A9-A7 as '000' in order to maintain the default or calibrated value.

Table 8 — OCD drive mode program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) HIGH and $\overline{\text{DQS}}$ LOW
0	1	0	Drive(0) DQ, DQS, (RDQS) LOW and $\overline{\text{DQS}}$ HIGH
1	0	0	Adjust mode
1	1	1	OCD calibration default

3.4.3.2 OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in Table 9. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in table 9 means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs and DQS's of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied.

Table 9 — OCD adjust mode program

4bit burst code inputs to all DQs				Operation	
DT0	DT1	DT2	DT3	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

For proper operation of adjust mode, $WL = RL - 1 = AL + CL - 1$ clocks and t_{DS}/t_{DH} should be met as shown in Figure 20. For input data pattern for adjustment, DT0 - DT3 is a fixed order and is not affected by burst type (i.e., sequential or interleave).

3.4.3 Off-chip driver (OCD) impedance adjustment (cont'd)

3.4.3.2 OCD impedance adjust (cont'd)

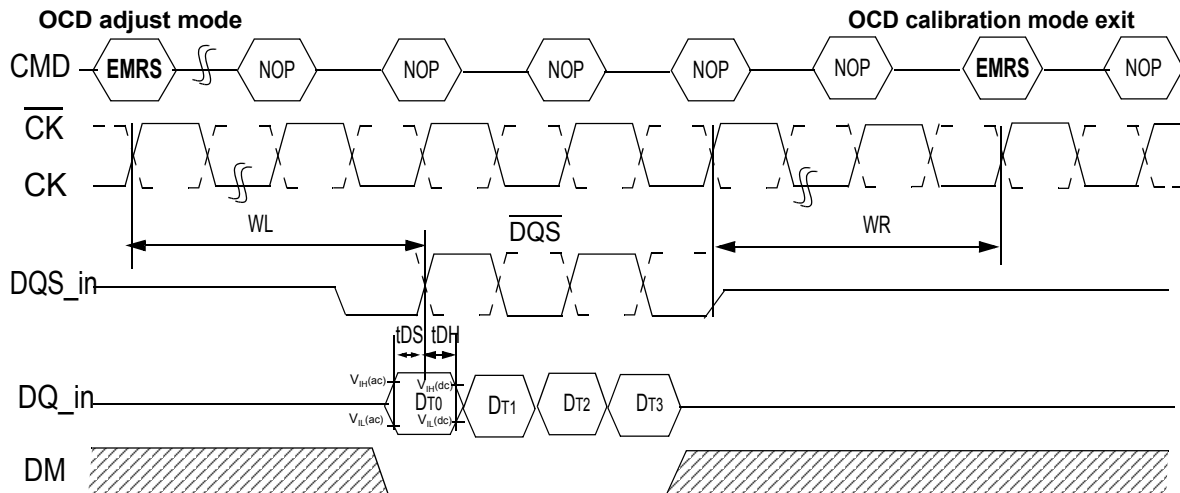


Figure 20 — OCD adjust mode

3.4.3.3 Drive mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out t_{OIT} after “enter drive mode” command and all output drivers are turned-off t_{OIT} after “OCD calibration mode exit” command as shown in Figure 21..

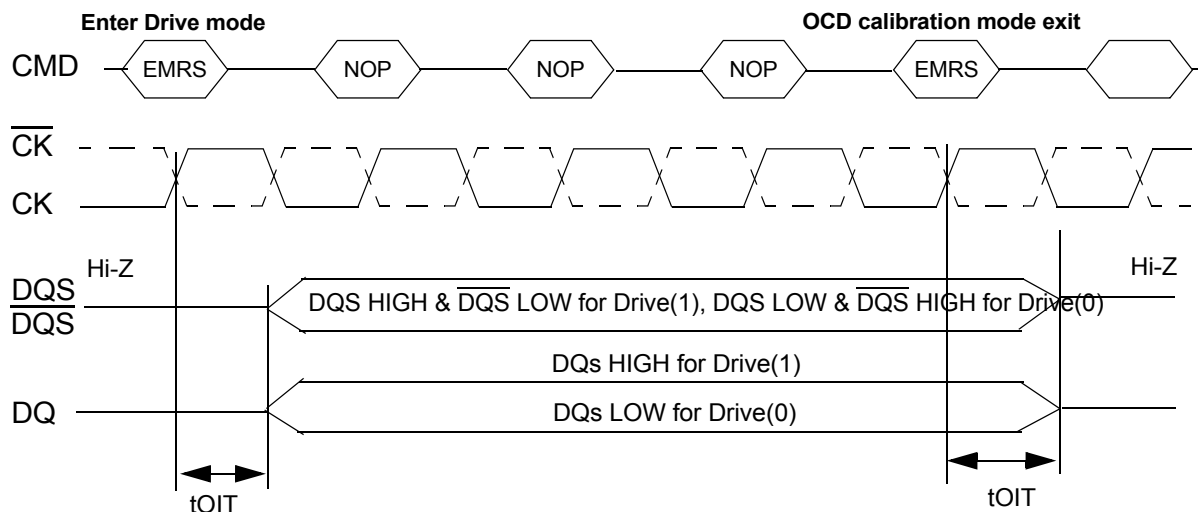


Figure 21 — OCD drive mode

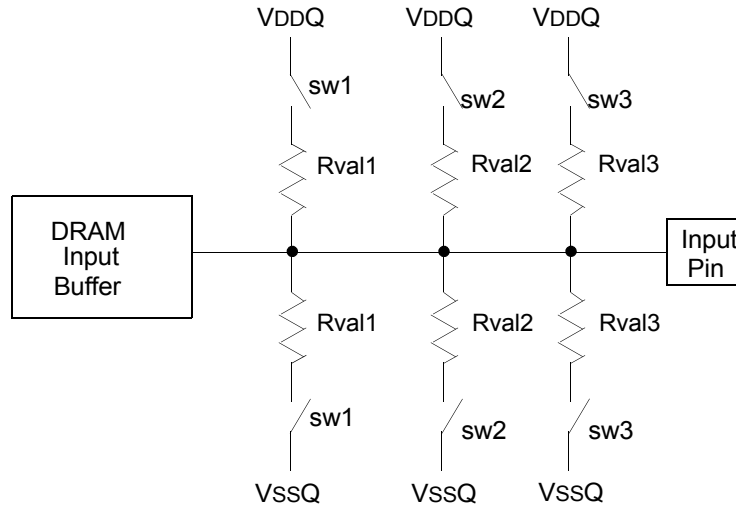
3 Functional Description (cont'd)

3.4 Programming the mode and extended mode registers (cont'd)

3.4.4 ODT (on-die termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/ $\overline{\text{DQS}}$, RDQS/ $\overline{\text{RDQS}}$, and DM signal for x4/x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/ $\overline{\text{UDQS}}$, LDQS/ $\overline{\text{LDQS}}$, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is supported for ACTIVE and STANDBY modes. ODT is turned off and not supported in SELF REFRESH mode.



Switch (sw1, sw2, sw3) is enabled by ODT pin.

Selection among sw1, sw2, and sw3 is determined by "Rtt (nominal)" in EMR.

Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.

Figure 22 — Functional representation of ODT

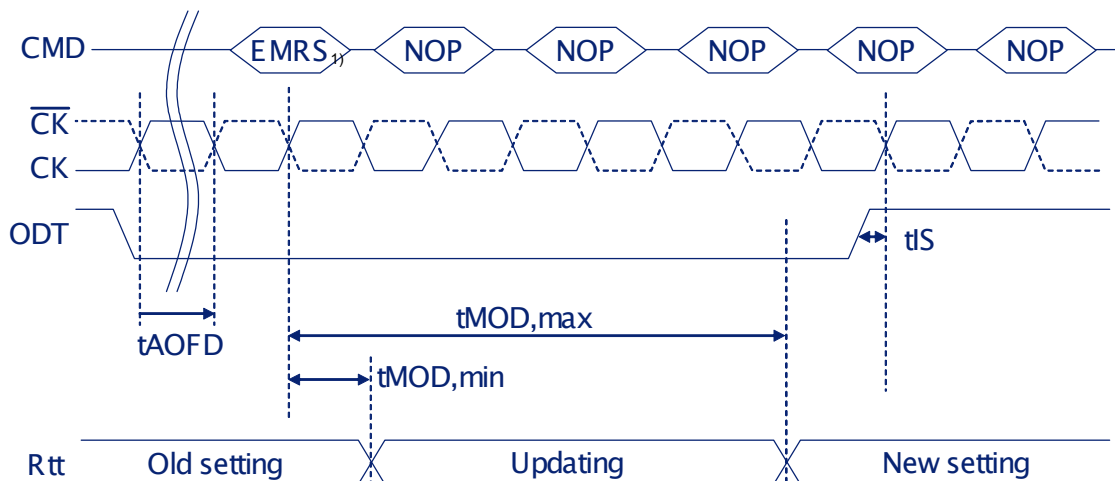
3.4.5 ODT related timings

3.4.5.1 MRS command to ODT update delay

During normal operation the value of the effective termination resistance can be changed with an EMRS command. The update of the Rtt setting is done between $t_{\text{MOD,min}}$ and $t_{\text{MOD,max}}$, and CKE must remain HIGH for the entire duration of tMOD window for proper operation. The timings are shown in the following timing diagram.

3.4.5 ODT related timings (cont'd)

3.4.5.1 MRS command to ODT update delay (cont'd)



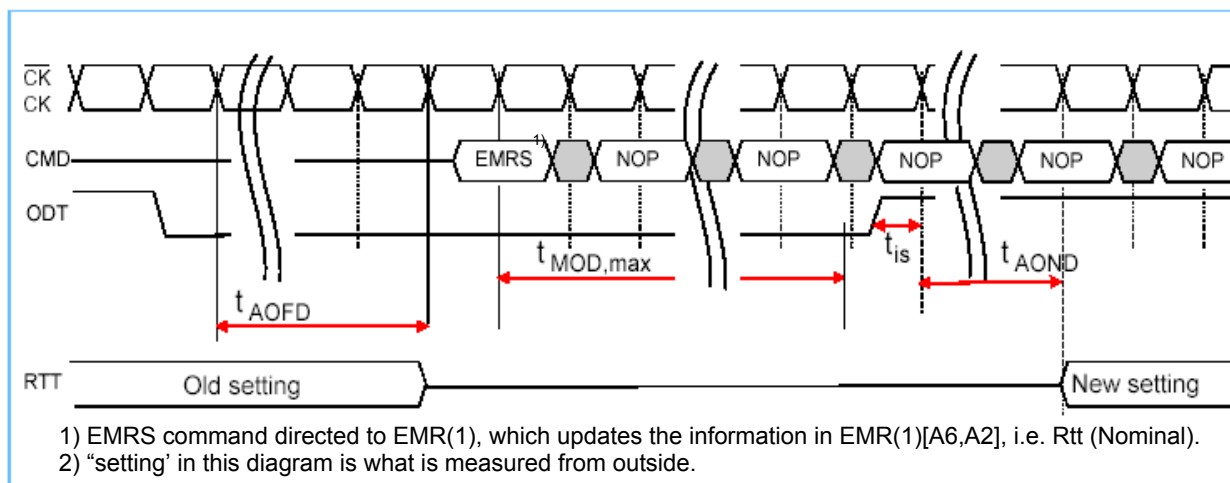
- 1) EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
- 2) "setting" in this diagram is the Register and I/O setting, not what is measured from outside.

Figure 23 — ODT update delay timing - tMOD

However, to prevent any impedance glitch on the channel, the following conditions must be met.

- tAOFD must be met before issuing the EMRS command
- ODT must remain LOW for the entire duration of tMOD window, until tMOD,max is met

Now the ODT is ready for normal operation with the new setting, and the ODT signal may be raised again to turned on the ODT. Following timing diagram shows the proper Rtt update procedure.



- 1) EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
- 2) "setting" in this diagram is what is measured from outside.

Figure 24 — ODT update delay timing - tMOD, as measured from outside

3.4 Programming the mode and extended mode registers (cont'd)

3.4.5 ODT related timings (cont'd)

3.4.5.2 ODT On/Off timings

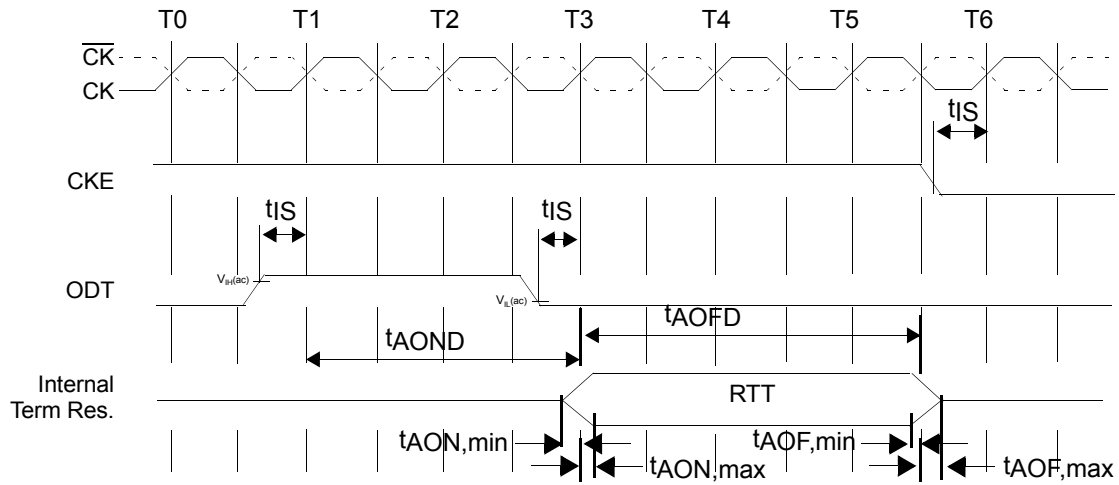


Figure 25 — ODT timing for active/standby mode

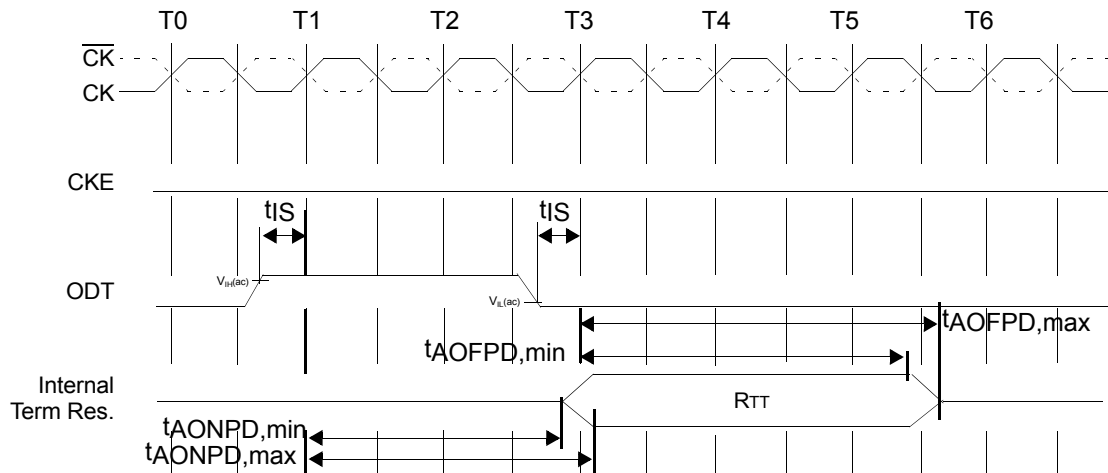


Figure 26 — ODT timing for power-down mode