

JEDEC STANDARD

Addendum No. 1 to JESD79-3 - 1.35 V DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1866

JESD79-3-1A.01

(Minor Editorial Revision of JESD79-3-1A, January 2013)

MAY 2013

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Published by
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3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

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1.35 V DDR3-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1866

(From JEDEC Board Ballot, JCB-10-12 and JCB-11-95, formulated under the cognizance of the JC-42.3 Subcommittee on Volatile RAM.)

1 Scope

The JESD79-3 document defines DDR3L SDRAM, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments with the exception of what is stated within this standard.

The purpose of this standard is to define the DDR3L specifications that supersede the DDR3 specifications as defined in JESD79-3. The use of DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600, and DDR3-1866 titles in JESD79-3 are to be interpreted as DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1866, respectively, when applying towards DDR3L definition; unless specifically stated otherwise.

2 DDR3L VDD/VDDQ requirements

Table 1 — Input/output functional description

Symbol	Type	Function
V_{DD}	Supply	Power Supply: DDR3L operation = 1.283 V to 1.45 V; DDR3 operation = 1.425 V to 1.575 V
V_{DDQ}	Supply	DQ Power Supply: DDR3L operation = 1.283 V to 1.45 V; DDR3 operation = 1.425 V to 1.575 V

Table 2 — Recommended DC Operating Conditions - DDR3L (1.35 V) operation

Symbol	Parameter/Condition	min	Typ	max	Units	Notes
V_{DD}	Supply voltage	1.283	1.35	1.45	V	1,2,3,4
V_{DDQ}	Supply voltage for Output	1.283	1.35	1.45	V	1,2,3,4

NOTE 1 Maximum DC value may not be greater than 1.425V. The DC value is the linear average of $V_{DD}/V_{DDQ}(t)$ over a very long period of time (e.g., 1 sec).

NOTE 2 If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.

NOTE 3 Under these supply voltages, the device operates to this DDR3L specification.

NOTE 4 Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3 operation (see Figure 1).

2 DDR3L VDD/VDDQ requirements (cont'd)

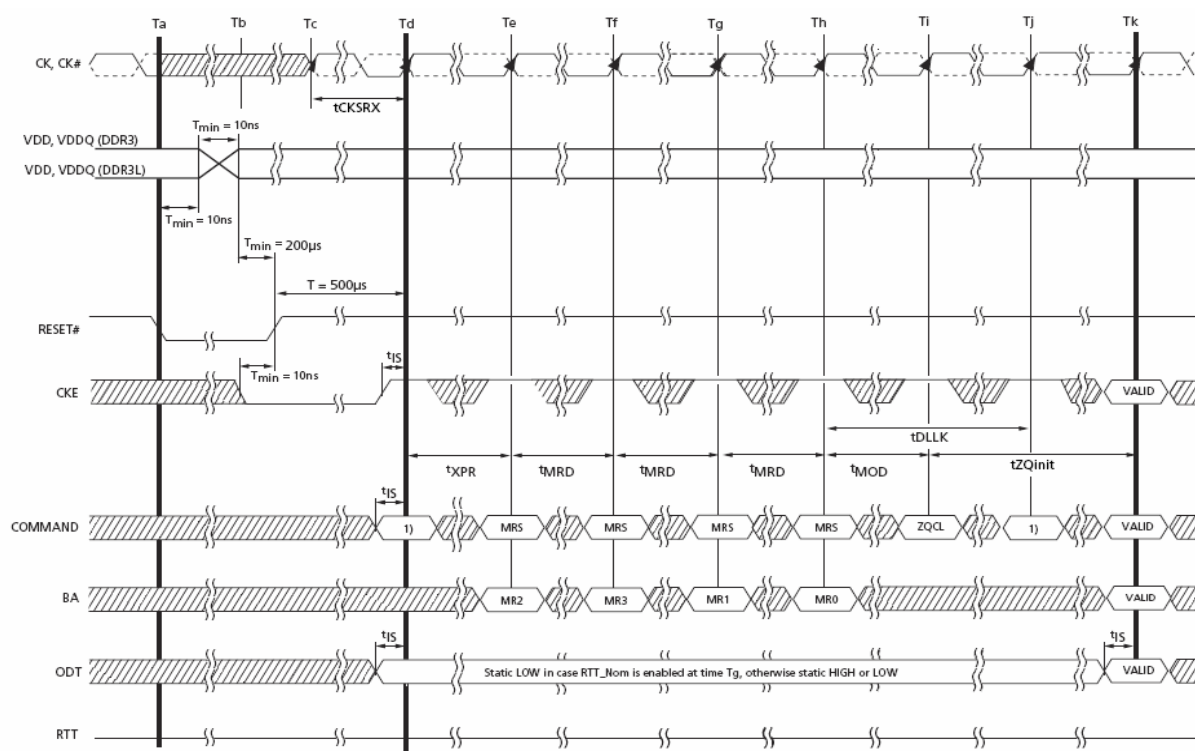
Table 3 — Recommended DC Operating Conditions - DDR3 (1.5 V) operation

Symbol	Parameter/Condition	min	Typ	max	Units	Notes
V_{DD}	Supply voltage	1.425	1.5	1.575	V	1,2,3
V_{DDQ}	Supply voltage for Output	1.425	1.5	1.575	V	1,2,3

NOTE 1 If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.

NOTE 2 Under 1.5 V operation, this DDR3L device operates to the DDR3 specifications under the same speed timings as defined for this device.

NOTE 3 Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3L operation (see Figure 1).



NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK DON'T CARE

Figure 1 — V_{DDQ}/V_{DDQ} Voltage Switch Between DDR3L and DDR3

3 1.35 V DDR3L AC and DC Logic Input Levels for Single-Ended Signals

3.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Table 4 — Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3L-800, DDR3L-1066		DDR3L-1333, DDR3L-1600		DDR3L-1866		Unit	Notes
		min	max	min	max	min	max		
VIH.CA(DC90)	DC input logic high	Vref + 0.09	V _{DD}	Vref + 0.09	V _{DD}	Vref + 0.09	V _{DD}	V	1
VIL.CA(DC90)	DC input logic low	V _{SS}	Vref - 0.09	V _{SS}	Vref - 0.09	V _{SS}	Vref - 0.09	V	1
VIH.CA(AC160)	AC input logic high	Vref + 0.160	Note 2	Vref + 0.160	Note 2	-	-	V	1, 2, 5
VIL.CA(AC160)	AC input logic low	Note 2	Vref - 0.160	Note 2	Vref - 0.160	-	-	V	1, 2, 5
VIH.CA(AC135)	AC input logic high	Vref + 0.135	Note 2	Vref + 0.135	Note 2	Vref + 0.135	Note 2	V	1, 2, 5
VIL.CA(AC135)	AC input logic low	Note 2	Vref - 0.135	Note 2	Vref - 0.135	Note 2	Vref - 0.135	V	1, 2, 5
VIH.CA(AC125)	AC input logic high	-	-	-	-	Vref + 0.125	Note 2	V	1, 2, 5
VIL.CA(AC125)	AC input logic low	-	-	-	-	Note 2	Vref - 0.125	V	1, 2, 5
VRefCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * V _{DD}	0.51 * V _{DD}	0.49 * V _{DD}	0.51 * V _{DD}	0.49 * V _{DD}	0.51 * V _{DD}	V	3, 4

NOTE 1 For input only pins except RESET#. Vref = VrefCA(DC).

NOTE 2 See JESD79-3E, 9.6 "Overshoot and Undershoot Specifications", 9.6.1.

NOTE 3 The AC peak noise on V_{Ref} may not allow V_{Ref} to deviate from V_{RefDQ(DC)} by more than +/-1% V_{DD} (for reference: approx. +/- 13.5 mV).

NOTE 4 For reference: approx. V_{DD}/2 +/- 13.5 mV

NOTE 5 These levels apply for 1.35 Volt (see Table 4) operation only. If the device is operated at 1.5 V (see Table 23), the respective levels in JESD79-3 (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), VIH/L.CA(AC135), VIH/L.CA(AC125), etc.) apply. The 1.5 V levels (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), VIH/L.CA(AC135), VIH/L.CA(AC125), etc.) do not apply when the device is operated in the 1.35 voltage range.

3.2 AC and DC Input Levels for Single-Ended Data Signals

Table 5 — Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800, DDR3L-1066		DDR3L-1333, DDR3L-1600		DDR3L-1866		Unit	Notes
		min	max	min	max	min	max		
VIH.DQ(DC90)	DC input logic high	Vref + 0.09	V _{DD}	Vref + 0.09	V _{DD}	Vref + 0.09	V _{DD}	V	1
VIL.DQ(DC90)	DC input logic low	V _{SS}	Vref - 0.09	V _{SS}	Vref - 0.09	V _{SS}	Vref - 0.09	V	1
VIH.DQ(AC160)	AC input logic high	Vref + 0.160	Note 2	-	-	-	-	V	1, 2, 5
VIL.DQ(AC160)	AC input logic low	Note 2	Vref - 0.160	-	-	-	-	V	1, 2, 5
VIH.DQ(AC135)	AC input logic high	Vref + 0.135	Note 2	Vref + 0.135	Note 2	-	-	V	1, 2, 5
VIL.DQ(AC135)	AC input logic low	Note 2	Vref - 0.135	Note 2	Vref - 0.135	-	-	V	1, 2, 5
VIH.DQ(AC130)	AC input logic high	-	-	-	-	Vref + 0.130	Note 2	V	1, 2, 5
VIL.DQ(AC130)	AC input logic low	-	-	-	-	Note 2	Vref - 0.130	V	1, 2, 5
VRefDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * V _{DD}	0.51 * V _{DD}	0.49 * V _{DD}	0.51 * V _{DD}	0.49 * V _{DD}	0.51 * V _{DD}	V	3, 4

NOTE 1 For input only pins except RESET#. Vref = VrefDQ(DC).

NOTE 2 See JESD79-3E, 9.6 "Overshoot and Undershoot Specifications", 9.6.2.

NOTE 3 The AC peak noise on V_{Ref} may not allow V_{Ref} to deviate from V_{RefDQ(DC)} by more than +/-1% V_{DD} (for reference: approx. +/- 13.5 mV).

NOTE 4 For reference: approx. V_{DD}/2 +/- 13.5 mV.

NOTE 5 These levels apply for 1.35 Volt (see Table 5) operation only. If the device is operated at 1.5 V (see Table 24), the respective levels in JESD79-3 (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135), etc.) apply. The 1.5 V levels (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135), etc.) do not apply when the device is operated in the 1.35 voltage range.

4 1.35 V DDR3L Electrical Characteristics and AC Timing

Table 6 — Timing Parameters by Speed Bin^a

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units	Notes
		min	max	min	max	min	max	min	max	min	max		
Data Timing													
Data setup time to DQS, DQS# referenced to Vih.DQ(ac) / Vil.DQ(ac) levels	tDS(base) AC160 SR = 1V/ns	90	-	40	-	-	-	-	-	-	-	ps	Refer to JESD79-3 d, 17
	tDS(base) AC135 SR = 1V/ns	140	-	90	-	45	-	25	-	-	-	ps	Refer to JESD79-3 d, 17
	tDS(base) AC130 SR = 2V/ns	-	-	-	-	-	-	-	-	70	-	ps	Refer to JESD79-3 d
Data hold time from DQS, DQS# referenced to Vih.DQ(dc) / Vil.DQ(dc) levels	tDH(base) DC90 SR = 1V/ns	160	-	110	-	75	-	55	-	-	-	ps	Refer to JESD79-3 d, 17
	tDH(base) DC90 SR = 2V/ns	-	-	-	-	-	-	-	-	75	-	ps	Refer to JESD79-3 d
Command and Address Timing													
Command and Address setup time to CK, CK# referenced to Vih.CA(ac) / Vil.CA(ac) levels	tIS(base) AC160 SR = 1V/ns	215	-	140	-	80	-	60	-	-	-	ps	Refer to JESD79-3 b, 16
	tIS(base) AC135 SR = 1V/ns	365	-	290	-	205	-	185	-	65	-	ps	Refer to JESD79-3 b, 16
	tIS(base) AC125 SR = 1V/ns	-	-	-	-	-	-	-	-	150	-	ps	Refer to JESD79-3 b, 16
Command and Address hold time from CK, CK# referenced to Vih.CA(dc) / Vil.CA(dc) levels	tIH(base) DC90 SR = 1V/ns	285	-	210	-	150	-	130	-	110	-	ps	Refer to JESD79-3 b, 16
a The setup and hold parameters in this table apply for 1.35 V (see Table 2) operation only. If the device is operated at 1.5 V (see Table 3), the respective parameters in JESD79-3 (tIS(base, AC175), tIS(base, AC150), tIH(base, DC100), tDS(base, AC175), tDS(base, AC150), tDH(base, DC100), etc.) apply. The 1.5 V setup/hold parameters (tIS(base, AC175), tIS(base, AC150), tIH(base, DC100), tDS(base, AC175), tDS(base, AC150), tDH(base, DC100), etc.) do not apply when the device is operated in the 1.35 voltage range.													
NOTE 1	The general notes from JESD79-3E, 13.4, apply to Table 6.												
NOTE 2	VDD =VDDQ = 1.35 V +0.100/- 0.067V												

Table 7 — ADD/CMD Setup and Hold Base-Values for 1 V/ns

Symbol	Reference	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Units	Note
tIS(base) AC160	V _{IH/L} (AC) : SR=1 V/ns	215	140	80	60	-	ps	1
tIS(base) AC135	V _{IH/L} (AC) : SR=1 V/ns	365	290	205	185	65	ps	1, 2
tIS(base) AC125	V _{IH/L} (AC) : SR=1 V/ns	-	-	-	-	150	ps	1, 3
tIH(base) DC90	V _{IH/L} (DC) : SR=1 V/ns	285	210	150	130	110	ps	1

NOTE 1 (AC/DC referenced for 1 V/ns Address/Command slew rate and 2 V/ns differential CK-CK# slew rate)

NOTE 2 The tIS(base) AC135 specifications are adjusted from the tIS(base) AC160 specification by adding an additional 125 ps for DDR3L-800/1066 or 100 ps for DDR3L-1333/1600 of derating to accommodate for the lower alternate threshold of 135 mV and another 25 ps to account for the earlier reference point [(160 mV - 135 mV) / 1 V/ns].

NOTE 3 The tIS(base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75 ps for DDR3L-1866 of derating to accommodate for the lower alternate threshold of 135 mV and another 10 ps to account for the earlier reference point [(135 mV - 125 mV) / 1 V/ns].