

JEDEC STANDARD

Addendum No. 2 to JESD79-3 -
for 1.25 V DDR3U-800, DDR3U-1066,
DDR3U-1333, and DDR3U-1600

JESD79-3-2

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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1.25 V DDR3U-800, DDR3U-1066, DDR3U-1333, and DDR3U-1600

(From JEDEC Board Ballot, JCB-11-39, formulated under the cognizance of the JC-42.3 Subcommittee on Volatile RAM.)

1 Scope

The JESD79-3 document defines the DDR3 SDRAM, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments with the exception of what is stated within this addendum.

The purpose of this addendum is to define the DDR3U specifications that supersede the DDR3 specifications in the JESD79-3. The use of DDR3-800, DDR3-1066, DDR3-1333, and DDR3-1600 titles in JESD79-3 are to be interpreted as DDR3U-800, DDR3U-1066, DDR3U-1333, and DDR3U-1600, respectively, when applying towards DDR3U definition; unless specifically stated otherwise.

2 DDR3U VDD/VDDQ Requirements

Table 1 — Recommended DC Operating Conditions - DDR3U (1.25 V) operation

Symbol	Parameter/Condition	Min	Typ	Max	Units	Notes
VDD	Supply voltage	1.19	1.25	1.31	V	1,2,3,4
VDDQ	Supply voltage for Output	1.19	1.25	1.31	V	1,2,3,4
NOTE 1 Maximum DC value may not be greater than 1.31 V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g., 1 sec).						
NOTE 2 If maximum limit is exceeded, input levels shall be governed by DDR3L specifications depending on the value.						
NOTE 3 Under these supply voltages, the device operates to this DDR3U specification.						
NOTE 4 Once initialized for DDR3U operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation (see Figure 1).						

Table 2 — Recommended DC Operating Conditions - DDR3L (1.35 V) operation

Symbol	Parameter/Condition	Min	Typ	Max	Units	Notes
VDD	Supply voltage	1.283	1.35	1.45	V	1,2,3,4
VDDQ	Supply voltage for Output	1.283	1.35	1.45	V	1,2,3,4
NOTE 1 Maximum DC value may not be greater than 1.425 V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g., 1 sec).						
NOTE 2 If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.						
NOTE 3 Under these supply voltages, the device operates to this DDR3L specification.						
Once initialized for DDR3L operation, DDR3U operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3U operation (see Figure 1).						

DDR3U SDRAM is 1.5V endurant.

DDR3U SDRAM operation at 1.5V is not supported.

2 DDR3U VDD/VDDQ Requirements (cont'd)

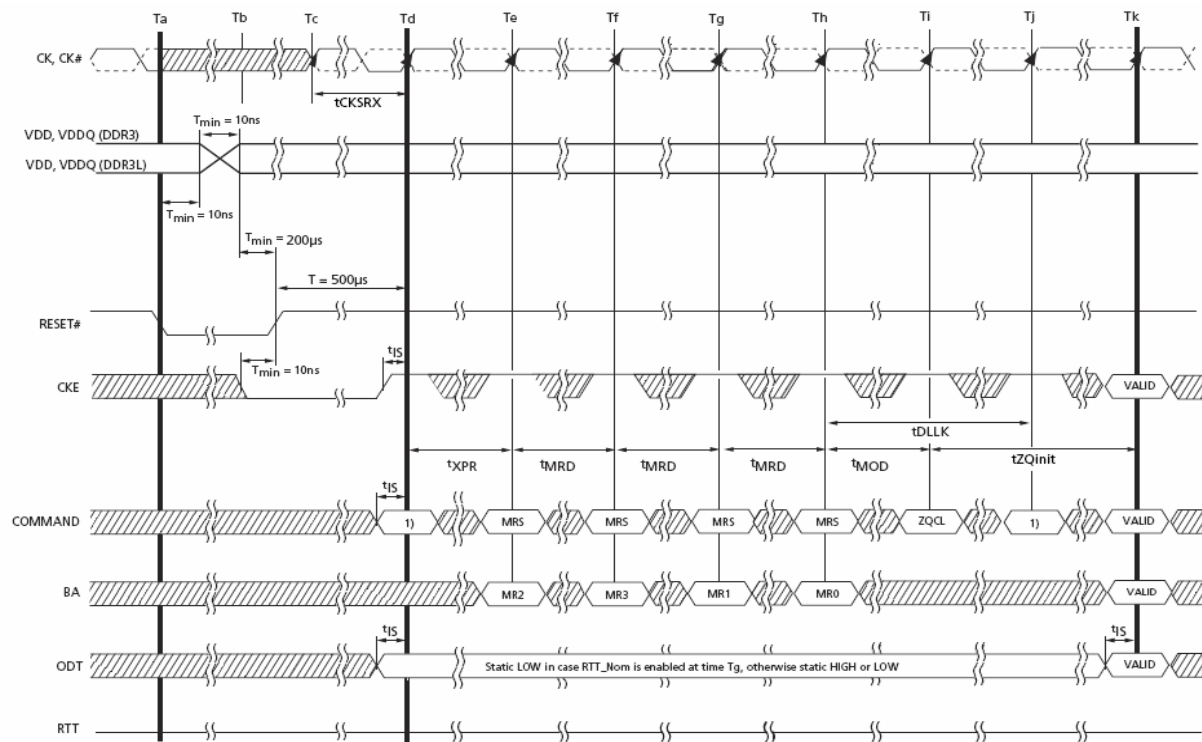
Table 3 — Absolute Maximum DC Ratings

Symbol	Parameter/Condition	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.4V ~ 1.6V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4V ~ 1.6V	V	1,3
V _{IN} , V _{OUT}	Voltage on any pin relative to Vss	-0.4V ~ 1.6V	V	1
TSTG	Storage Temperature	-55 to +100	°C	1,2

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 3 VDD and VDDQ must be within 250 mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV.



NOTE 1. From time point “Td” until “Tk” NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK DON'T CARE

Figure 1 — VDD/VDDQ Voltage Switch Between DDR3U and DDR3L

3 1.25 V DDR3U AC and DC Logic Input Levels for Single-Ended Signals

3.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Table 4 — Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3U-800, DDR3U-1066		DDR3U-1333, DDR3U-1600		Unit	Notes
		Min	Max	Min	Max		
VIH.CA(DC90)	DC input logic high	Vref + 0.090	VDD	Vref + 0.090	VDD	V	1
VIL.CA(DC90)	DC input logic low	VSS	Vref - 0.090	VSS	Vref - 0.090	V	1
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note 2	Vref + 0.150	Note 2	V	1, 2, 5
VIL.CA(AC150)	AC input logic low	Note 2	Vref - 0.150	Note 2	Vref - 0.150	V	1, 2, 5
VIH.CA(AC130)	AC input logic high	Vref + 0.130	Note 2	Vref + 0.130	Note 2	V	1, 2, 5
VIL.CA(AC130)	AC input logic low	Note 2	Vref - 0.130	Note 2	Vref - 0.130	V	1, 2, 5
V _{RefCA} (DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

NOTE 1 For input only pins except RESET#. Vref = VrefCA(DC).
NOTE 2 See JESD79-3, 9.6 "Overshoot and Undershoot Specifications" (9.6.1).
NOTE 3 The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from V_{RefDQ}(DC) by more than +/-1% VDD (for reference: approx. +/- 12.5 mV).
NOTE 4 For reference: approx. VDD/2 +/- 12.5 mV.
NOTE 5 These levels apply for 1.25 V operation only. If the device is operated at 1.35 V the appropriate levels in JESD79-3-1, VIH/L.CA(DC90), VIH/L.CA(AC160), VIH/L.CA(AC135), etc.) apply. The 1.35 V levels VIH/L.CA(DC90), VIH/L.CA(AC160), VIH/L.CA(AC135) etc.) do not apply when the device is operated in the 1.25 voltage range.

3.2 AC and DC Input Levels for Single-Ended Data Signals

Table 5 — Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3U-800, DDR3U-1066		DDR3U-1333, DDR3U-1600		Unit	Notes
		Min	Max				
VIH.DQ(DC90)	DC input logic high	Vref + 0.090	VDD	Vref + 0.090	VDD	V	1
VIL.DQ(DC90)	DC input logic low	VSS	Vref - 0.090	VSS	Vref - 0.090	V	1
VIH.DQ(AC150)	AC input logic high	Vref + 0.150	Note 2	-	-	V	1, 2, 5
VIL.DQ(AC150)	AC input logic low	Note 2	Vref - 0.150	-	-	V	1, 2, 5
VIH.DQ(AC130)	AC input logic high	Vref + 0.130	Note 2	Vref + 0.130	Note 2	V	1, 2, 5
VIL.DQ(AC130)	AC input logic low	Note 2	Vref - 0.130	Note 2	Vref - 0.130	V	1, 2, 5
V _{RefDQ} (DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

NOTE 1 For input only pins except RESET#. Vref = VrefDQ(DC).
NOTE 2 See JESD79-3, 9.6 "Overshoot and Undershoot Specifications" (9.6.1).
NOTE 3 The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from V_{RefDQ}(DC) by more than +/-1% VDD (for reference: approx. +/- 12.5 mV).
NOTE 4 For reference: approx. VDD/2 +/- 12.5 mV.
NOTE 5 These levels apply for 1.25 V operation only. If the device is operated at 1.35 V, the appropriate levels in JESD79-3-1 VIH/L.DQ(DC90), VIH/L.DQ (AC160), VIH/L.DQ(AC135), etc.) apply. The 1.35 V levels VIH/L.DQ(DC90), VIH/L.DQ(AC160), VIH/L.DQ(AC135), etc.) do not apply when the device is operated in the 1.25 voltage range.