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Addendum No. 3 to JESD79-3: 3D Stacked SDRAM

JESD79-3-3

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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TABLE OF CONTENTS

1 Scope	1
1.1 Definition of Terms	1
2 3DS SDRAM Package Pinout and Addressing	3
2.1 Overview	3
2.2 3D Stacked / DDR3 SDRAM x4 Ballout using MO-207	4
2.3 3D Stacked / DDR3 SDRAM x8 Ballout using MO-207	5
2.4 Logical Rank Addressing	6
2.5 3D Stack Organizations	6
2.6 3DS SDRAM System Addressing	7
2.7 DDR3 3DS Stack Addressing Table	7
2.8 Bank Selection	11
3 Functional Description	13
3.1 Simplified State Diagram	13
3.2 Basic Functionality	13
3.3 Reset Signal and Initialization Procedure	13
3.4 Mode Register Definition	14
4 SDRAM Command Description and Operation	17
4.1 Write Leveling	17
4.2 ACTIVE Command	17
4.3 Precharge and Precharge All Commands	18
4.4 Read and Write Commands	21
4.5 Refresh Command	21
4.6 Self-Refresh Operation and Power-Down Modes	22
4.7 ZQ Calibration Commands	23
5 On Die Termination	25
6 Absolute Maximum Ratings	27
7 AC & DC Operating Conditions	29
8 AC & DC Input Measurement Levels	31
9 AC & DC Output Measurement Levels	33
10 IDD Current Specification	35
10.1 IDD and IDDQ Measurement Conditions	35
10.2 IDD Specifications	51
11 Input/Output Capacitance	53
12 Electrical Characteristics & AC Timings for DDR3-3DS-800 to DDR3-3DS-1866	55
12.1 Clock Specification	55
12.2 Refresh parameters by logical rank density	55
12.3 Standard 3DS Speed Bins	56
12.3.1 Speed Bin Table Notes	61
13 Electrical Characteristics and AC Timings	63

LIST OF TABLES

Table 1 —Supported 3D Stack Organizations.....	6
Table 2 —DDR3 Address table: 2H Stacked SDRAM	7
Table 3 —DDR3 Address table: 4H Stacked SDRAM	8
Table 4 —DDR3 Address table: 8H Stacked SDRAM	10
Table 5 —Simplified Truth Table for MRS Command.....	14
Table 6 —Truth Table for ACTIVE Command	18
Table 7 —Truth Table for Precharge Command	19
Table 8 —Truth Table for Precharge All Command.....	20
Table 9 —Logical Rank to Logical Rank CMD-to-CMD Timings.....	21
Table 10 —Truth Table for Refresh Command.....	22
Table 11 —Truth Table for SRE and PDE	23
Table 12 —Absolute Maximum DC Ratings	27
Table 13 —Recommended DC Operating Conditions	29
Table 14 —Timings used for IDD and IDDQ measurements loop patterns.....	37
Table 14 —Timings used for IDD and IDDQ measurements loop patterns (Continued)	38
Table 15 —Basic IDD and IDDQ Measurement Conditions	39
Table 16 —IDD0 measurement - Loop pattern, 4H Stacking as Example.....	42
Table 17 —IDD1 measurement - Loop pattern, 4H Stacking as Example.....	43
Table 18 —IDD2N and IDD3N measurement - Loop pattern	44
Table 19 —IDD2N and IDDQ2NT measurement-Loop pattern	44
Table 20 —IDD4R and IDDQ4R measurement-Loop pattern, 4H Stacking as Example.....	45
Table 21 —IDD4W measurement-Loop pattern, 4H Stacking as Example.....	46
Table 22 —IDD5B1 measurement-Loop pattern, 4H Stacking as Example.....	47
Table 23 —IDD5B2 measurement-Loop pattern, 4H Stacking as Example.....	48
Table 24 —IDD7 measurement – Loop pattern	49
Table 25 —Specification Example 4Gbit DDR3-3DS	51
Table 26 —IDD6 Specification	52
Table 27 —Refresh parameters by logical rank density.....	55
Table 28 —DDR3-800 3D Stacked Speed Bins and Operating Conditions.....	56
Table 29 —DDR3-1066 3D Stacked Speed Bins and Operating Conditions.....	57
Table 30 —DDR3-1333 3D Stacked Speed Bins and Operating Conditions.....	58
Table 31 —DDR3-1600 3DS Speed Bins and Operating Conditions	59
Table 32 —DDR3-1866 3DS Speed Bins and Operating Conditions	60
Table 33 —Timing Parameters by Speed Bin	63
Table 33 —Timing Parameters by Speed Bin (Continued).....	64

LIST OF FIGURES

Figure 1 3D Stacked DDR3 SDRAM x4 Ballout	4
Figure 2 3D Stacked DDR3 SDRAM x8 Ballout	5
Figure 3 2-2-1-1 Device (2H)	7
Figure 4 4-4-1-1 Device (4H)	8
Figure 5 8-4-1-1 Device (8H)	9
Figure 6 Bank Selection.....	11
Figure 7 Mode Register 0 Definition	15
Figure 8 Mode Register 1 Definition	15
Figure 9 Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements.....	36
Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.....	36

ADDENDUM NO. 3 TO JESD79-3: 3D STACKED SDRAM

(From JEDEC BoD ballot JCB-12-12, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

1 Scope

This addendum to JESD79-3 defines the 3DS DDR3 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for compliant 8Gbit through 64Gbit x4 and x8 3DS DDR3 SDRAM devices. This document was created based on the E revision of the DDR standard (JESD79). Each aspect of the changes for 3DS DDR3 SDRAM operation was considered.

The requirement for 3DS devices compliant to this spec addendum is to have a single electrical load for the stacked devices no matter if the stack is comprised of 2, 4 or 8 devices. The I/O buffer circuitry can be built into the base SDRAM of the stack or into a separate logic buffer device. In either case (built in native DRAM circuitry or separate logic die), the assumption is that the I/O buffers are located at the bottom of the stack closest to the package substrate. All pictures and diagrams in the spec depict a master die at the bottom of the stack.

1.1 Definition of Terms

3DS: 3D Stacked SDRAM devices with a single electrical load. In the remainder of this document both the long form as well as the abbreviation are used interchangeably.

Logical Rank: 3DS devices are divided into 2, 4 or 8 logical ranks. Devices with 2 or 4 logical ranks use 2 or 4 chip select pins to select the logical ranks. Devices with 8 logical ranks use 4 chip select pins and a single ID pin to select the logical ranks. There is not necessarily a 1-to-1 relationship between a physical die and a logical rank.

Package Rank: A package rank on a 3D stacked module consists of all 3DS packages that together span the whole data width of the module. For example with a 72-bit ECC module using x4 3DS devices, a package rank consists of 18 packages.

Master Logical Rank: The master logical rank in the 3DS device is the device in the stack that buffers external signals between the controller and the SDRAM stack. Other logical ranks in the stack only communicate to the master logical rank and are not visible as loads on the DDR bus to the controller. By convention, the master logical rank is controlled by CS0_n.

2 3DS SDRAM Package Pinout and Addressing

2.1 Overview

These ballouts have been derived from JEDEC DDR3 Standard JESD79-3. The ballout comprehends x4 and x8 data widths, where x4 is a subset of the x8 ballout. Address mirroring option for existing A[15:0] is preserved without change, e.g. as allowed by DDR3 UDIMM and LRDIMM specifications.

2.2 3D Stacked / DDR3 SDRAM x4 Ballout using MO-207

Ball locations highlighted in red in Figure 1, “3D Stacked DDR3 SDRAM x4 Ballout” indicate deviations from JESD 79-3 Quad-stacked/Quad-die SDRAM x4 ballout.

[X-ray view from package top surface]

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC		NC				NC		NC	NC
B											
C	NC	NC		NC				NC		NC	NC
D											
E											
F	NC	VSS	VDD	NC				NU	VSS	VDD	NC
G		VSS	VSSQ	DQ0				DM	VSSQ	VDDQ	
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	
J		VSSQ	NC	DQS_n				VDD	VSS	VSSQ	
K		VREFDQ	VDDQ	NC				NC	NC	VDDQ	
L		NC	VSS	RAS_n				CK_t	VSS	CID, NC ¹	
M		ODT	VDD	CAS_n				CK_c	VDD	CKE	
N		CS1_n	CS0_n	WE_n				A10/AP	ZQ	NC	
P		VSS	BA0	BA2				A15, NC ²	VREFCA	VSS	
R		CS2_n, NC ³	A3	A0				A12/Bacon	BA1	VDD	
T		CS3_n, NC ³	A5	A2				A1	A4	VSS	
U		VDD	A7	A9				A11	A6	VDD	
V	NC	VSS	RESET_n	A13				A14	A8	VSS	NC
W											
Y											
AA	NC	NC		NC				NC		NC	NC
AB											
AC	NC	NC		NC				NC		NC	NC

1. Not used for 3DS devices with two or four logical ranks
2. Not used for 3DS devices with 2Gb logical rank densities
3. Not used for 3DS devices with two logical ranks

Figure 1 — 3D Stacked DDR3 SDRAM x4 Ballout

2.3 3D Stacked / DDR3 SDRAM x8 Ballout using MO-207

Ball locations highlighted in red in Figure 2, “3D Stacked DDR3 SDRAM x8 Ballout” indicate deviations from JESD 79-3 Quad-stacked/Quad-die SDRAM x8 ballout.

[X-ray view from package top surface]

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC		NC				NC		NC	NC
B											
C	NC	NC		NC				NC		NC	NC
D											
E											
F	NC	VSS	VDD	NC				TDQS _n	VSS	VDD	NC
G		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ	
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	
J		VSSQ	DQ6	DQS _n				VDD	VSS	VSSQ	
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ	
L		NC	VSS	RAS _n				CK _t	VSS	CID, NC ¹	
M		ODT	VDD	CAS _n				CK _c	VDD	CKE	
N		CS1 _n	CS0 _n	WE _n				A10/AP	ZQ	NC	
P		VSS	BA0	BA2				A15, NC ²	VREFCA	VSS	
R		CS2 _n , NC ³	A3	A0				A12/BC _n	BA1	VDD	
T		CS3 _n , NC ³	A5	A2				A1	A4	VSS	
U		VDD	A7	A9				A11	A6	VDD	
V	NC	VSS	RESET _n	A13				A14	A8	VSS	NC
W											
Y											
AA	NC	NC		NC				NC		NC	NC
AB											
AC	NC	NC		NC				NC		NC	NC

1. Not used for 3DS devices with two or four logical ranks
2. Not used for 3DS devices with 2Gb logical rank densities
3. Not used for 3DS devices with two logical ranks

Figure 2 — 3D Stacked DDR3 SDRAM x8 Ballout

2.4 Logical Rank Addressing

The 3DS package is organized into two, four or eight logical ranks.

For 3DS devices with 2 and 4 logical ranks, the logical ranks are selected by dedicated CS_n inputs. For 3DS devices with eight logical ranks, an additional select input CID (Chip ID) is used together with the four CS_n inputs to decode eight internal select signals. Figure 5, “8-4-1-1 Device (8H)” and Table 4, “DDR3 Address table: 8H Stacked SDRAM” define the behavior of the CID input.

The functional behavior of logical rank(s) should not deviate from DDR3 JEDEC standard SDRAMs, except when noted in this document. Each logical rank may be implemented as a single slice but the DDR3 3DS specification doesn't require this to be the case. For example a 3DS device with four logical ranks may be implemented as eight slices, i.e. two 4Gb slices with 1 KB page size may be combined into an 8Gb logical rank with 2KB page size. Such an implementation has the advantage of not requiring a CID pin, making it more compatible with existing hosts and module support chips than regular 8H 3DS devices with eight 4Gb logical ranks (with 1KB page size).

2.5 3D Stack Organizations

Table 1, “Supported 3D Stack Organizations,” indicates valid configurations supported by the 3DS specification.

Table 1 — Supported 3D Stack Organizations

# of Logical Ranks	# of CS _n	# of CKE	# of ODT
2	2	1	1
4	4	1	1
8	4	1	1

Figure 3, Figure 4, and Figure 5 show one architectural diagram per row of Table 1. For the names of the these figures the standard *3DS configuration notation* LR-CS-CKE-ODT is used where LR indicates the number of logical ranks, CS_n indicates the number of chip select inputs, CKE indicates the number of CKE inputs and ODT indicates the number of ODT inputs. Since there is only one valid configuration for each number of logical ranks, this document will typically use the abbreviations 2H, 4H and 8H to describe 3DS devices with two, four or eight logical ranks. Table 1 shows all valid CKE and ODT configurations.

2.6 3DS SDRAM System Addressing

3DS addressing scheme for 3DS devices is explained in section 2.7. This document comprehends using these 3DS devices in RDIMM and LRDIMM applications with x4 or x8 3DS SDRAMs.

2.7 DDR3 3DS Stack Addressing Table

3DS devices with two and four logical ranks use dedicated CS_n inputs to select these logical ranks. 3DS SDRAMs with eight logical ranks require the additional address input CID (Chip ID) to select logical ranks 4 to 7. Figure 5 and Table 4 define the behavior of the CID pin.

Table 2, Table 3, and Table 4 indicate the address and select pins that are used for different configurations of 3DS stacks.

The 3DS DDR3 devices may be derived from monolithic DDR3 devices. Therefore the address signals used within a logical rank are identical to the address signals used by a monolithic DRAM of the same density.

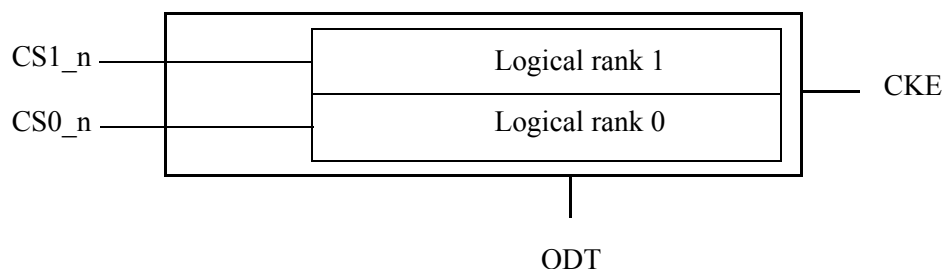


Figure 3 — 2-2-1-1 Device (2H)

Table 2 — DDR3 Address table: 2H Stacked SDRAM

DDR3 3DS address table : 2H 3D Stacked SDRAM								
3DS Logical Rank Organization					3DS Package Organization			
Density	Page Size	MSB Address			Capacity	Page Size	Logical Rank	Logical Rank selected by
		Row	Col					
			x4 Die	x8 Die				
2Gb	1KB	A14	A11	A9	4Gb	1KB	0	CS0_n
							1	CS1_n
4Gb	1KB	A15	A11	A9	8Gb	1KB	0	CS0_n
							1	CS1_n
8Gb	2KB	A15	A13	A11	16Gb	2KB	0	CS0_n
							1	CS1_n

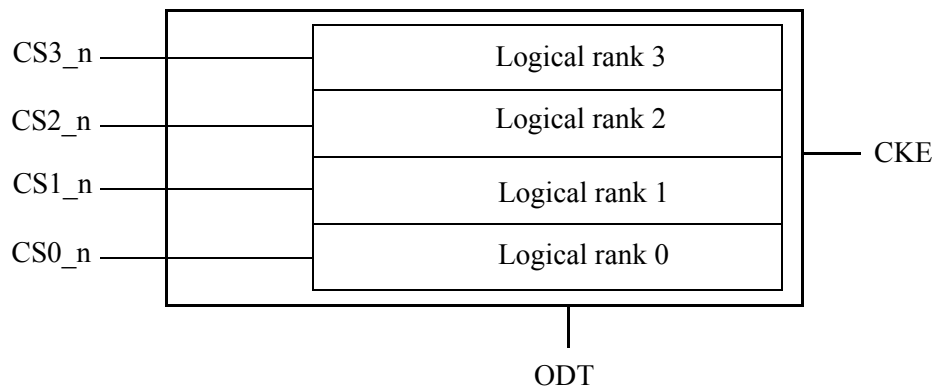


Figure 4 — 4-4-1-1 Device (4H)

Table 3 — DDR3 Address table: 4H Stacked SDRAM

DDR3 3DS address table : 4H Stacked SDRAM								
3DS Logical Rank Organization					3DS Package Organization			
Density	Page Size	MSB Address			Capacity	Page Size	Logical Rank	Logical Rank selected by
		Row	Col					
			x4 Die	x8 Die				
2Gb	1KB	A14	A11	A9	8Gb	1KB	0	CS0_n
							1	CS1_n
							2	CS2_n
							3	CS3_n
4Gb	1KB	A15	A11	A9	16Gb	1KB	0	CS0_n
							1	CS1_n
							2	CS2_n
							3	CS3_n
8Gb	2KB	A15	A13	A11	32Gb	2KB	0	CS0_n
							1	CS1_n
							2	CS2_n
							3	CS3_n

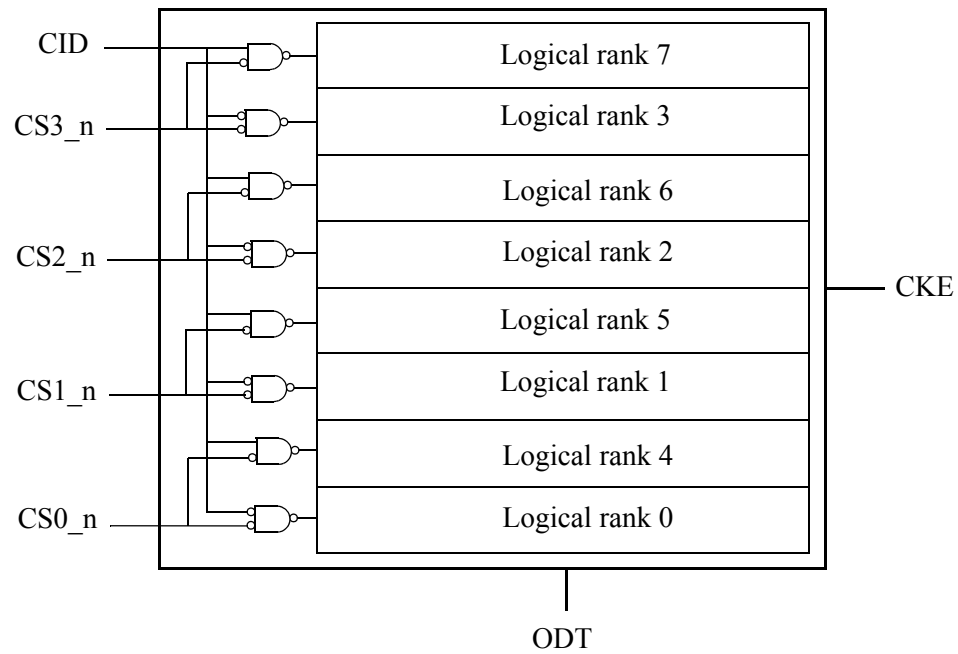


Figure 5 — 8-4-1-1 Device (8H)

Table 4 — DDR3 Address table: 8H Stacked SDRAM

DDR3 3DS address table : 8H Stacked SDRAM									
3DS Logical Rank Organization					3DS Package Organization				
Density	Page Size	MSB Address			Capacity	Page Size	Logical Rank	Logical Rank selected by	
		Row	Col						
			x4 Die	x8 Die					
2Gb	1KB	A14	A11	A9	16Gb	1KB	0	CS0_n	CID=L
							1	CS1_n	CID=L
							2	CS2_n	CID=L
							3	CS3_n	CID=L
							4	CS0_n	CID=H
							5	CS1_n	CID=H
							6	CS2_n	CID=H
							7	CS3_n	CID=H
4Gb	1KB	A15	A11	A9	32Gb	1KB	0	CS0_n	CID=L
							1	CS1_n	CID=L
							2	CS2_n	CID=L
							3	CS3_n	CID=L
							4	CS0_n	CID=H
							5	CS1_n	CID=H
							6	CS2_n	CID=H
							7	CS3_n	CID=H
8Gb	2KB	A15	A13	A11	64Gb	2KB	0	CS0_n	CID=L
							1	CS1_n	CID=L
							2	CS2_n	CID=L
							3	CS3_n	CID=L
							4	CS0_n	CID=H
							5	CS1_n	CID=H
							6	CS2_n	CID=H
							7	CS3_n	CID=H

Note that these diagrams show only the logical organizations of these devices. No 1:1 relationship to physical organizations is implied.

2.8 Bank Selection

3DS devices can accommodate up to 64 independent banks. Figure 6, “Bank Selection” shows how these banks are selected.

	Bank 63	Bank 62	Bank 61	Bank 60	Bank 59	Bank 58	Bank 57	Bank 56	CS3_n	CS2_n	CS1_n	CS0_n	CID
Logical Rank 7	Bank 63	Bank 62	Bank 61	Bank 60	Bank 59	Bank 58	Bank 57	Bank 56	0	1	1	1	1
Logical Rank 6	Bank 55	Bank 54	Bank 53	Bank 52	Bank 51	Bank 50	Bank 49	Bank 48	1	0	1	1	1
Logical Rank 5	Bank 47	Bank 46	Bank 45	Bank 44	Bank 43	Bank 42	Bank 41	Bank 40	1	1	0	1	1
Logical Rank 4	Bank 39	Bank 38	Bank 37	Bank 36	Bank 35	Bank 34	Bank 33	Bank 32	1	1	1	0	1
Logical Rank 3	Bank 31	Bank 30	Bank 29	Bank 28	Bank 27	Bank 26	Bank 25	Bank 24	0	1	1	1	0
Logical Rank 2	Bank 23	Bank 22	Bank 21	Bank 20	Bank 19	Bank 18	Bank 17	Bank 16	1	0	1	1	0
Logical Rank 1	Bank 15	Bank 14	Bank 13	Bank 12	Bank 11	Bank 10	Bank 9	Bank 8	1	1	0	1	0
Logical Rank 0	Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0	1	1	1	0	0

Addressed by BA[2:0] =

111	110	101	100	011	010	001	000
-----	-----	-----	-----	-----	-----	-----	-----

Figure 6 — Bank Selection

3 Functional Description

3.1 Simplified State Diagram

DDR3 3D Stacked SDRAMs use the same simplified state diagram documented in JESD79-3. Situations involving more than one bank, and multiple logical ranks are not reflected in the simple state diagram.

3.2 Basic Functionality

The 3DS DDR3 SDRAM is a 2H, 4H or 8H stacked high-speed dynamic random-access memory with each logical rank configured as an eight-logical bank SDRAM. The 3DS SDRAM has 16, 32 or 64 physical banks available internally, depending on the number of logical ranks. The 3DS DDR3 SDRAM retains the use of an 8n pre-fetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the 3DS DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal SDRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

3.3 Reset Signal and Initialization Procedure

Prior to normal operation, the 3DS DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

A single reset pin with a single load is available per 3DS device. It is expected that the entire stack of SDRAMs within the package reset as per DDR3 specification. After RESET_n is de-asserted, the SDRAM will start internal state initialization; this will be done independently of external clocks. All steps in the JESD79-3 initialization sequence must be followed. No additional steps are required for 3DS DDR3 devices but the unique nature of 3DS devices (which have a single external I/O structure shared by all logical ranks of the entire device) has to be considered when programming the SDRAM mode register bits (see next section for details).

3.4 Mode Register Definition

Like planar DDR3 SDRAMs, DDR3 3D Stacked SDRAMs have four Mode Registers. One set of registers controls the entire stack regardless if the 3DS stack has two, four or eight logical ranks, and they must be programmed via a Mode Register Set (MRS) command.

For 3DS DDR3 stacks configured as n logical ranks, the single set of MRS registers is addressed by CS0_n as shown in Table 5.

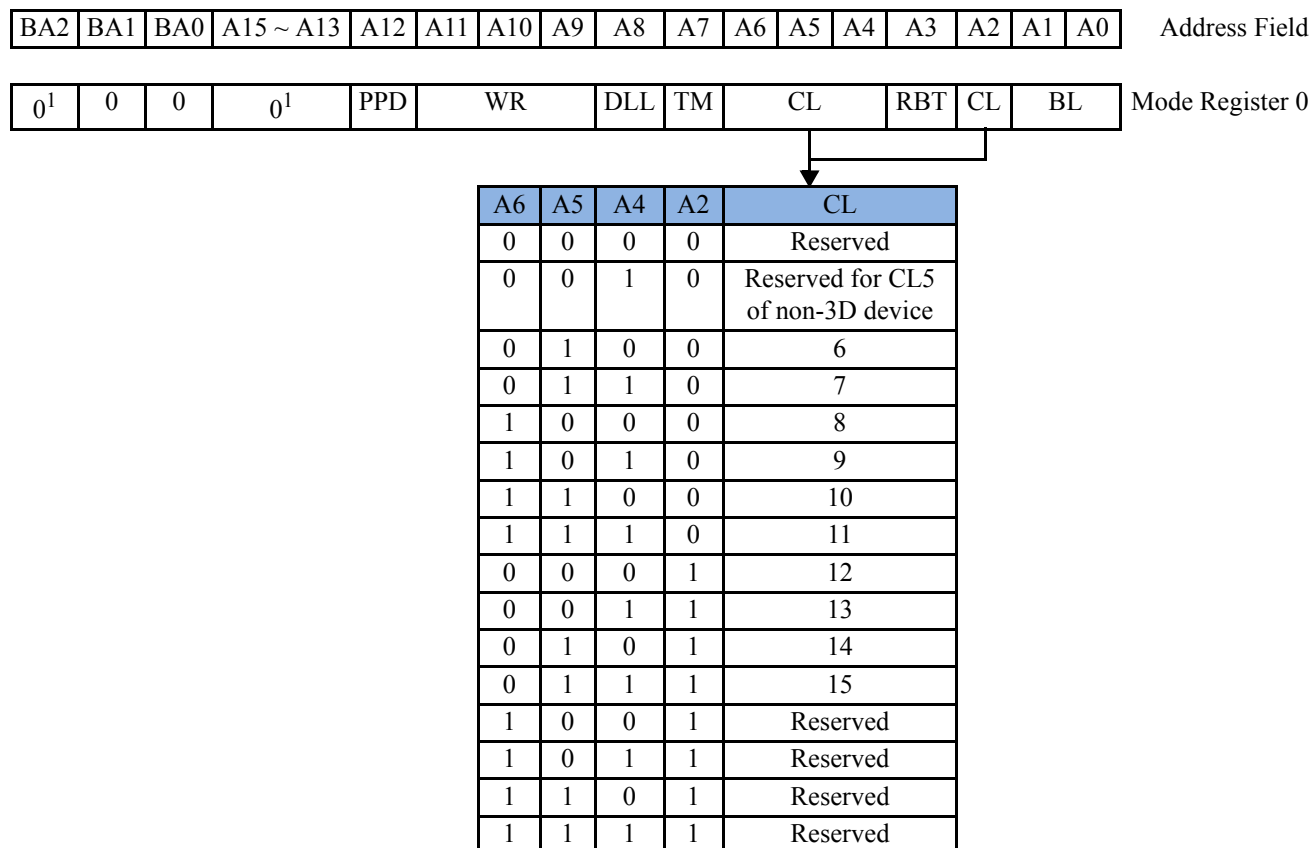
Table 5 — Simplified Truth Table for MRS Command

DRAM Command	CS0_n	CS1_n	CS2_n	CS3_n	CID	Logical rank 0	Logical rank 1	Logical rank 2	Logical rank 3	Logical rank 4	Logical rank 5	Logical rank 6	Logical rank 7	Notes
Mode Register Set	L	V	V	V	V	MRS	MRS	MRS	MRS	MRS	MRS	MRS	MRS	1 2
Mode Register Set	H	V	V	V	V	DES or NOP	DES or NOP	DES or NOP	DES or NOP	DES or NOP	DES or NOP	DES or NOP	DES or NOP	2
Any Command	H	H	H	H	V	DES	DES	DES	DES	DES	DES	DES	DES	2

1. Mode Register Set to all logical ranks
2. "V" means H or L (but a defined logic level)

Programming the register fields for a stacked device has some special considerations. Waiting for the timing parameter tMRD is required between two MRS commands issued to any logical rank in a stacked device. After an MRS command is given, waiting for tMOD is required before a non-MRS command can be given to any logical rank in the stack.

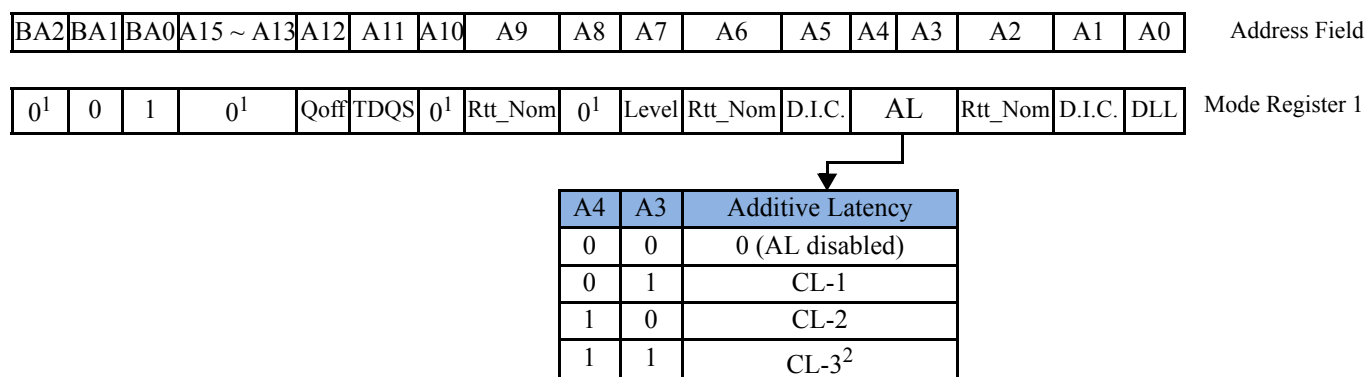
The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. Due to the additional latency caused by stacking multiple memory dies, one additional CAS Latency setting (CL-15), which was not used in the JESD79-3 base specification, has been added to the MR0 bits A[6:4], as shown in Figure 7.



1. Must be programmed to 0

Figure 7 — Mode Register 0 Definition

In MR1, Additive Latency (AL) of CL-3 is supported for the case that tAA is larger than tRCD (optional if tAA=tRCD), as shown in Figure 8.



1. Must be programmed to 0
2. For devices supporting the DDR3-1066F-3DS1B, DDR3-1333H-3DS1B, DDR3-1600K-3DS1B and DDR3-1866M-3DS1B speed bins, support for AL=CL-3 is optional

Figure 8 — Mode Register 1 Definition