

JEDEC STANDARD

DDR3 SDRAM Standard

JESD79-3F

(Revision of JESD79-3E, July 2010)

JULY 2012

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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1 Scope

This document defines the DDR3 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 512 Mb through 8 Gb for x4, x8, and x16 DDR3 SDRAM devices. This specification was created based on the DDR2 specification (JESD79-2) and some aspects of the DDR specification (JESD79). Each aspect of the changes for DDR3 SDRAM operation were considered and approved by committee ballot(s). The accumulation of these ballots were then incorporated to prepare this JESD79-3 specification, replacing whole sections and incorporating the changes into Functional Description and Operation.

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2 DDR3 SDRAM Package Pinout and Addressing

2.1 DDR3 SDRAM x4 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	A
B												B
C	NC	NC		NC				NC		NC	NC	C
D												D
E												E
F	NC	VSS	VDD	NC				NC	VSS	VDD	NC	F
G		VSS	VSSQ	DQ0				DM	VSSQ	VDDQ		G
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		H
J		VSSQ	NC	DQS#				VDD	VSS	VSSQ		J
K		VREFDQ	VDDQ	NC				NC	NC	VDDQ		K
L		NC	VSS	RAS#				CK	VSS	NC		L
M		ODT	VDD	CAS#				CK#	VDD	CKE		M
N		NC	CS#	WE#				A10/AP	ZQ	NC		N
P		VSS	BA0	BA2				A15	VREFCA	VSS		P
R		VDD	A3	A0				A12/BC#	BA1	VDD		R
T		VSS	A5	A2				A1	A4	VSS		T
U		VDD	A7	A9				A11	A6	VDD		U
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	V
W												W
Y												Y
AA	NC	NC		NC				NC		NC	NC	AA
AB												AB
AC	NC	NC		NC				NC		NC	NC	AC
	1	2	3	4	5	6	7	8	9			

NOTE: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

MO-207 Variation DT-z (x4)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○

○ Populated ball
+ Ball not populated

MO-207 Variation DW-z (x4)
with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	○	+	+	+	○	+	○	○
B	+	+	+	+	+	+	+	+	+	+	+
C	○	○	+	○	+	+	+	○	+	○	○
D	+	+	+	+	+	+	+	+	+	+	+
E	○	○	+	○	+	+	+	○	+	○	○
F	+	+	+	+	+	+	+	+	+	+	+
G	+	○	○	○	+	+	+	○	+	○	+
H	+	○	○	○	+	+	+	○	+	○	+
J	+	○	○	○	+	+	+	○	+	○	+
K	+	○	○	○	+	+	+	○	+	○	+
L	+	○	○	○	+	+	+	○	+	○	+
M	+	○	○	○	+	+	+	○	+	○	+
N	+	○	○	○	+	+	+	○	+	○	+
P	+	○	○	○	+	+	+	○	+	○	+
R	+	○	○	○	+	+	+	○	+	○	+
T	+	○	○	○	+	+	+	○	+	○	+
U	+	○	○	○	+	+	+	○	+	○	+
V	○	○	○	○	+	+	+	○	+	○	○
W	+	+	+	+	+	+	+	+	+	+	+
Y	+	+	+	+	+	+	+	+	+	+	+
AA	+	○	○	○	+	+	+	○	+	○	+
AB	+	+	+	+	+	+	+	+	+	+	+
AC	○	○	+	○	+	+	+	○	+	○	○

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.2 DDR3 SDRAM x8 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC		NC				NC		NC	NC
B											
C	NC	NC		NC				NC		NC	NC
D											
E											
F	NC	VSS	VDD	NC				NU/TDQS#	VSS	VDD	NC
G		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ	
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	
J		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ	
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ	
L		NC	VSS	RAS#				CK	VSS	NC	
M		ODT	VDD	CAS#				CK#	VDD	CKE	
N		NC	CS#	WE#				A10/AP	ZQ	NC	
P		VSS	BA0	BA2				A15	VREFCA	VSS	
R		VDD	A3	A0				A12/BC#	BA1	VDD	
T		VSS	A5	A2				A1	A4	VSS	
U		VDD	A7	A9				A11	A6	VDD	
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC
W											
Y											
AA	NC	NC		NC				NC		NC	NC
AB											
AC	NC	NC		NC				NC		NC	NC
	1	2	3	4	5	6	7	8	9		

NOTE: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

MO-207 Variation DT-z (x8)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○

○ Populated ball
+ Ball not populated

MO-207 Variation DW-z (x8)
with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	○	+	+	+	○	+	○	○
B	+	+	+	+	+	+	+	+	+	+	+
C	○	○	+	○	+	+	+	○	+	○	○
D	+	+	+	+	+	+	+	+	+	+	+
E	+	+	+	+	+	+	+	+	+	+	+
F	○	○	○	○	+	+	+	○	○	○	○
G	+	○	○	○	+	+	+	○	○	○	+
H	+	○	○	○	+	+	+	○	○	○	+
J	+	○	○	○	+	+	+	○	○	○	+
K	+	○	○	○	+	+	+	○	○	○	+
L	+	○	○	○	+	+	+	○	○	○	+
M	+	○	○	○	+	+	+	○	○	○	+
N	+	○	○	○	+	+	+	○	○	○	+
P	+	○	○	○	+	+	+	○	○	○	+
R	+	○	○	○	+	+	+	○	○	○	+
T	+	○	○	○	+	+	+	○	○	○	+
U	+	○	○	○	+	+	+	○	○	○	+
V	○	○	○	○	+	+	+	○	○	○	○
W	+	+	+	+	+	+	+	+	+	+	+
Y	+	○	+	○	+	+	+	○	+	○	○
AA	○	○	+	○	+	+	+	○	+	○	○
AB	+	+	+	+	+	+	+	+	+	+	+
AC	○	○	+	○	+	+	+	○	+	○	○



Documents

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2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.3 DDR3 SDRAM x16 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C												
D	NC	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	NC	A
E		VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ		B
F		VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ		C
G		VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD		D
H		VSS	VSSQ	DQL0				DML	VSSQ	VDDQ		E
J		VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ		F
K		VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ		G
L		VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ		H
M		NC	VSS	RAS#				CK	VSS	NC		J
N		ODT	VDD	CAS#				CK#	VDD	CKE		K
P		NC	CS#	WE#				A10/AP	ZQ	NC		L
R		VSS	BA0	BA2				A15	VREFCA	VSS		M
T		VDD	A3	A0				A12/BC#	BA1	VDD		N
U		VSS	A5	A2				A1	A4	VSS		P
V		VDD	A7	A9				A11	A6	VDD		R
W	NC	VSS	RESET#	A13				A14	A8	VSS	NC	T
Y												
AA												
AB	NC	NC		NC				NC		NC	NC	
	1	2	3	4	5	6	7	8	9			

NOTE: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

MO - 207 Variation DU-z (x16)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	+	○	○
B	○	○	○	+	+	+	+	○	○
C	○	○	○	+	+	+	+	○	○
D	○	○	○	+	+	+	+	○	○
E	○	○	○	+	+	+	+	○	○
F	○	○	○	+	+	+	+	○	○
G	○	○	○	+	+	+	+	○	○
H	○	○	○	+	+	+	+	○	○
J	○	○	○	+	+	+	+	○	○
K	○	○	○	+	+	+	+	○	○
L	○	○	○	+	+	+	+	○	○
M	○	○	○	+	+	+	+	○	○
N	○	○	○	+	+	+	+	○	○
P	○	○	○	+	+	+	+	○	○
R	○	○	○	+	+	+	+	○	○
T	○	○	○	+	+	+	+	○	○

○ Populated ball
+ Ball not populated

MO-207 Variation DY-z (x16)
with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	○	+	+	+	○	+	○	○
B	+	+	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+	+	+
D	○	○	○	○	+	+	+	○	○	○	○
E	+	○	○	○	+	+	+	○	○	○	+
F	+	○	○	○	+	+	+	○	○	○	+
G	+	○	○	○	+	+	+	○	○	○	+
H	+	○	○	○	+	+	+	○	○	○	+
J	+	○	○	○	+	+	+	○	○	○	+
K	+	○	○	○	+	+	+	○	○	○	+
L	+	○	○	○	+	+	+	○	○	○	+
M	+	○	○	○	+	+	+	○	○	○	+
N	+	○	○	○	+	+	+	○	○	○	+
P	+	○	○	○	+	+	+	○	○	○	+
R	+	○	○	○	+	+	+	○	○	○	+
T	+	○	○	○	+	+	+	○	○	○	+
U	+	○	○	○	+	+	+	○	○	○	+
V	+	○	○	○	+	+	+	○	○	○	+
W	○	○	○	○	+	+	+	○	○	○	○
Y	+	+	+	+	+	+	+	+	+	+	+
AA	+	+	+	+	+	+	+	+	+	+	+
AB	○	○	+	○	+	+	+	○	+	○	○

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.4 Stacked / dual-die DDR3 SDRAM x4 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C	NC	NC		NC				NC		NC	NC	
D												
E												
F	NC	VSS	VDD	NC				NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0				DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS#				VDD	VSS	VSSQ		D
K		VREFDQ	VDDQ	NC				NC	NC	VDDQ		E
L		ODT1	VSS	RAS#				CK	VSS	CKE1		F
M		ODT0	VDD	CAS#				CK#	VDD	CKE0		G
N		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2				A15	VREFCA	VSS		J
R		VDD	A3	A0				A12/BC#	BA1	VDD		K
T		VSS	A5	A2				A1	A4	VSS		L
U		VDD	A7	A9				A11	A6	VDD		M
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	N
W												
Y												
AA	NC	NC		NC				NC		NC	NC	
AB												
AC	NC	NC		NC				NC		NC	NC	
	1	2	3	4	5	6	7	8	9			

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

NOTE 2: This stacked ballout is intended for use only with stacked/dual-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

MO-207 Variation DT-z (x4)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○

○ Populated ball
+ Ball not populated

MO-207 Variation DW-z (x4)
with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	○	+	+	+	○	+	○	○
B	+	+	+	+	+	+	+	+	+	+	+
C	○	○	+	○	+	+	+	○	+	○	○
D	+	+	+	+	+	+	+	+	+	+	+
E	+	+	+	+	+	+	+	+	+	+	+
F	○	○	○	○	+	+	+	○	○	○	○
G	+	○	○	○	+	+	+	○	○	○	+
H	+	○	○	○	+	+	+	○	○	○	+
J	+	○	○	○	+	+	+	○	○	○	+
K	+	○	○	○	+	+	+	○	○	○	+
L	+	○	○	○	+	+	+	○	○	○	+
M	+	○	○	○	+	+	+	○	○	○	+
N	+	○	○	○	+	+	+	○	○	○	+
P	+	○	○	○	+	+	+	○	○	○	+
R	+	○	○	○	+	+	+	○	○	○	+
T	+	○	○	○	+	+	+	○	○	○	+
U	+	○	○	○	+	+	+	○	○	○	+
V	○	○	○	○	+	+	+	○	○	○	○
W	+	+	+	+	+	+	+	+	+	+	+
Y	+	+	+	+	+	+	+	+	+	+	+
AA	○	○	+	○	+	+	+	○	+	○	○
AB	+	+	+	+	+	+	+	+	+	+	+
AC	○	○	+	○	+	+	+	○	+	○	○



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.5 Stacked / dual-die DDR3 SDRAM x8 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC		NC				NC		NC	NC
B											
C	NC	NC		NC				NC		NC	NC
D											
E											
F	NC	VSS	VDD	NC				NU/TDQS#	VSS	VDD	NC
G		VSSQ	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ	
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	
J		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ	
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ	
L		ODT1	VSS	RAS#				CK	VSS	CKE1	
M		ODT0	VDD	CAS#				CK#	VDD	CKE0	
N		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1	
P		VSS	BA0	BA2				A15	VREFCA	VSS	
R		VDD	A3	A0				A12/BC#	BA1	VDD	
T		VSS	A5	A2				A1	A4	VSS	
U		VDD	A7	A9				A11	A6	VDD	
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC
W											
Y											
AA	NC	NC		NC				NC		NC	NC
AB											
AC	NC	NC		NC				NC		NC	NC
	1	2	3	4	5	6	7	8	9		

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

NOTE 2: This stacked ballout is intended for use only with stacked/dual-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

MO-207 Variation DT-z (x8)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○

○ Populated ball
+ Ball not populated

MO - 207 Variation DW-z (x8) with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	○	+	+	+	○	+	○	○
B	+	+	+	+	+	+	+	+	+	+	+
C	○	○	+	○	+	+	+	○	+	○	○
D	+	+	+	+	+	+	+	+	+	+	+
E	+	+	+	+	+	+	+	+	+	+	+
F	○	○	○	○	+	+	+	○	○	○	○
G	+	○	○	○	+	+	+	○	○	○	+
H	+	○	○	○	+	+	+	○	○	○	+
J	+	○	○	○	+	+	+	○	○	○	+
K	+	○	○	○	+	+	+	○	○	○	+
L	+	○	○	○	+	+	+	○	○	○	+
M	+	○	○	○	+	+	+	○	○	○	+
N	+	○	○	○	+	+	+	○	○	○	+
P	+	○	○	○	+	+	+	○	○	○	+
R	+	○	○	○	+	+	+	○	○	○	+
T	+	○	○	○	+	+	+	○	○	○	+
U	+	○	○	○	+	+	+	○	○	○	+
V	○	○	○	○	+	+	+	○	○	○	○
W	+	+	+	+	+	+	+	+	+	+	+
Y	+	+	+	+	+	+	+	+	+	+	+
AA	○	○	+	○	+	+	+	○	+	○	○
AB	+	+	+	+	+	+	+	+	+	+	+
AC	○	○	+	○	+	+	+	○	+	○	○



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.6 Stacked / dual-die DDR3 SDRAM x16 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC		NC				NC		NC	NC
B											
C											
D	NC	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	NC
E		VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ	
F		VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	
G		VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	
H		VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	
J		VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	
K		VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ	
L		VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	
M		ODT1	VSS	RAS#				CK	VSS	CKE1	
N		ODT0	VDD	CAS#				CK#	VDD	CKE0	
P		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1	
R		VSS	BA0	BA2				A15	VREFCA	VSS	
T		VDD	A3	A0				A12/BC#	BA1	VDD	
U		VSS	A5	A2				A1	A4	VSS	
V		VDD	A7	A9				A11	A6	VDD	
W	NC	VSS	RESET#	A13				A14	A8	VSS	NC
Y											
AA											
AB	NC	NC		NC				NC		NC	NC
	1	2	3	4	5	6	7	8	9		

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

NOTE 2: This stacked ballout is intended for use only with stacked/dual-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

MO - 207 Variation DU-z (x16)

1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○
B	○	○	○	+	+	+	○	○
C	○	○	○	+	+	+	○	○
D	○	○	○	+	+	+	○	○
E	○	○	○	+	+	+	○	○
F	○	○	○	+	+	+	○	○
G	○	○	○	+	+	+	○	○
H	○	○	○	+	+	+	○	○
J	○	○	○	+	+	+	○	○
K	○	○	○	+	+	+	○	○
L	○	○	○	+	+	+	○	○
M	○	○	○	+	+	+	○	○
N	○	○	○	+	+	+	○	○
P	○	○	○	+	+	+	○	○
R	○	○	○	+	+	+	○	○
T	○	○	○	+	+	+	○	○

○ Populated ball
+ Ball not populated

MO - 207 Variation DY-z
(x16) with support balls

1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	○	+	+	+	○	+	○
B	+	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+	+
D	+	+	+	+	+	+	+	+	+	+
E	+	○	○	○	+	+	+	○	○	+
F	+	○	○	○	+	+	+	○	○	+
G	+	○	○	○	+	+	+	○	○	+
H	+	○	○	○	+	+	+	○	○	+
J	+	○	○	○	+	+	+	○	○	+
K	+	○	○	○	+	+	+	○	○	+
L	+	○	○	○	+	+	+	○	○	+
M	+	○	○	○	+	+	+	○	○	+
N	+	○	○	○	+	+	+	○	○	+
P	+	○	○	○	+	+	+	○	○	+
R	+	○	○	○	+	+	+	○	○	+
T	+	○	○	○	+	+	+	○	○	+
U	+	○	○	○	+	+	+	○	○	+
V	+	○	○	○	+	+	+	○	○	+
W	○	○	○	○	+	+	+	○	○	○
Y	+	+	+	+	+	+	+	+	+	+
AA	+	+	+	+	+	+	+	+	+	+
AB	○	○	+	○	+	+	+	○	+	○

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.7 Quad-stacked / Quad-die DDR3 SDRAM x4 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC		NC				NC		NC	NC
B											
C	NC	NC		NC				NC		NC	NC
D											
E											
F	NC	VSS	VDD	NC				NC	VSS	VDD	NC
G		VSSQ	VSSQ	DQ0				DM	VSSQ	VDDQ	
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	
J		VSSQ	NC	DQS#				VDD	VSS	VSSQ	
K		VREFDQ	VDDQ	NC				NC	NC	VDDQ	
L		ODT1	VSS	RAS#				CK	VSS	CKE1	
M		ODT0	VDD	CAS#				CK#	VDD	CKE0	
N		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1	
P		VSS	BA0	BA2				A15	VREFCA	VSS	
R		CS2#	A3	A0				A12/BC#	BA1	ZQ2	
T		CS3#	A5	A2				A1	A4	ZQ3	
U		VDD	A7	A9				A11	A6	VDD	
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC
W											
Y											
AA	NC	NC		NC				NC		NC	NC
AB											
AC	NC	NC		NC				NC		NC	NC
	1	2	3	4	5	6	7	8	9		

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

NOTE 2: This stacked ballout is intended for use only with quad-stacked/quad-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

MO-207 Variation DT-z (x4)

	1	2	3	4	5	6	7	8	9
A	●	●	●	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○

○ Populated ball
+ Ball not populated

MO-207 Variation DW-z (x4) with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	+	+	+	+	○	+	○	○
B	+	+	+	+	+	+	+	+	+	+	+
C	○	○	+	+	+	+	+	○	+	○	○
D	+	+	+	+	+	+	+	+	+	+	+
E	+	+	+	+	+	+	+	+	+	+	+
F	○	○	○	+	+	+	+	○	○	○	○
G	+	○	○	○	+	+	+	○	○	○	+
H	+	○	○	○	+	+	+	○	○	○	+
J	+	○	○	○	+	+	+	○	○	○	+
K	+	○	○	○	+	+	+	○	○	○	+
L	+	○	○	○	+	+	+	○	○	○	+
M	+	○	○	○	+	+	+	○	○	○	+
N	+	○	○	○	+	+	+	○	○	○	+
P	+	○	○	○	+	+	+	○	○	○	+
R	+	○	○	○	+	+	+	○	○	○	+
T	+	○	○	○	+	+	+	○	○	○	+
U	+	○	○	○	+	+	+	○	○	○	+
V	○	○	○	+	+	+	+	○	○	○	○
W	+	+	+	+	+	+	+	+	+	+	+
Y	+	+	+	+	+	+	+	+	+	+	+
AA	○	○	+	+	+	+	+	○	+	○	○
AB	+	+	+	+	+	+	+	+	+	+	+
AC	○	○	+	+	+	+	+	○	+	○	○



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.8 Quad-stacked / Quad-die DDR3 SDRAM x8 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC		NC				NC		NC	NC
B											
C	NC	NC		NC				NC		NC	NC
D											
E											
F	NC	VSS	VDD	NC				NU/TDQS#	VSS	VDD	NC
G		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ	
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	
J		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ	
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ	
L		ODT1	VSS	RAS#				CK	VSS	CKE1	
M		ODT0	VDD	CAS#				CK#	VDD	CKE0	
N		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1	
P		VSS	BA0	BA2				A15	VREFCA	VSS	
R		CS2#	A3	A0				A12/BC#	BA1	ZQ2	
T		CS3#	A5	A2				A1	A4	ZQ3	
U		VDD	A7	A9				A11	A6	VDD	
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC
W											
Y											
AA	NC	NC		NC				NC		NC	NC
AB											
AC	NC	NC		NC				NC		NC	NC
	1	2	3	4	5	6	7	8	9		

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

NOTE 2: This stacked ballout is intended for use only with quad-stacked/quad-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

MO-207 Variation DT-z (x8)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○

○ Populated ball
+ Ball not populated

MO - 207 Variation DW-z (x8)
with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	○	+	+	+	○	+	○	○
B	+	+	+	+	+	+	+	+	+	+	+
C	○	○	+	○	+	+	+	○	+	○	○
D	+	+	+	+	+	+	+	+	+	+	+
E	+	+	+	+	+	+	+	+	+	+	+
F	○	○	○	○	+	+	+	○	+	○	○
G	+	○	○	○	+	+	+	○	○	○	+
H	+	○	○	○	+	+	+	○	○	○	+
J	+	○	○	○	+	+	+	○	○	○	+
K	+	○	○	○	+	+	+	○	○	○	+
L	+	○	○	○	+	+	+	○	○	○	+
M	+	○	○	○	+	+	+	○	○	○	+
N	+	○	○	○	+	+	+	○	○	○	+
P	+	○	○	○	+	+	+	○	○	○	+
R	+	○	○	○	+	+	+	○	○	○	+
T	+	○	○	○	+	+	+	○	○	○	+
U	+	○	○	○	+	+	+	○	○	○	+
V	○	○	○	○	+	+	+	○	+	○	○
W	+	+	+	+	+	+	+	+	+	+	+
Y	+	+	+	+	+	+	+	+	+	+	+
AA	○	○	+	○	+	+	+	○	+	○	○
AB	+	+	+	+	+	+	+	+	+	+	+
AC	○	○	+	○	+	+	+	○	+	○	○



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.9 Quad-stacked / Quad-die DDR3 SDRAM x16 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C												
D	NC	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	NC	A
E		VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ		B
F		VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ		C
G		VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD		D
H		VSS	VSSQ	DQL0				DML	VSSQ	VDDQ		E
J		VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ		F
K		VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ		G
L		VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ		H
M		ODT1	VSS	RAS#				CK	VSS	CKE1		J
N		ODT0	VDD	CAS#				CK#	VDD	CKE0		K
P		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		L
R		VSS	BA0	BA2				A15	VREFCA	VSS		M
T		CS2#	A3	A0				A12/BC#	BA1	ZQ2		N
U		CS3#	A5	A2				A1	A4	ZQ3		P
V		VDD	A7	A9				A11	A6	VDD		R
W	NC	VSS	RESET#	A13				A14	A8	VSS	NC	T
Y												
AA												
AB	NC	NC		NC				NC		NC	NC	
	1	2	3	4	5	6	7	8	9			

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

NOTE 2: This stacked ballout is intended for use only with quad-stacked/quad-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

MO - 207 Variation DU-z (x16)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○
P	○	○	○	+	+	+	○	○	○
R	○	○	○	+	+	+	○	○	○
T	○	○	○	+	+	+	○	○	○

○ Populated ball
+ Ball not populated

MO - 207 Variation DY-z (x16) with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	○	+	+	+	○	+	○	○
B	+	+	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+	+	+
D	+	+	+	+	+	+	+	+	+	+	+
E	+	○	○	○	+	+	+	○	○	○	+
F	+	○	○	○	+	+	+	○	○	○	+
G	+	○	○	○	+	+	+	○	○	○	+
H	+	○	○	○	+	+	+	○	○	○	+
J	+	○	○	○	+	+	+	○	○	○	+
K	+	○	○	○	+	+	+	○	○	○	+
L	+	○	○	○	+	+	+	○	○	○	+
M	+	○	○	○	+	+	+	○	○	○	+
N	+	○	○	○	+	+	+	○	○	○	+
P	+	○	○	○	+	+	+	○	○	○	+
R	+	○	○	○	+	+	+	○	○	○	+
T	+	○	○	○	+	+	+	○	○	○	+
U	+	○	○	○	+	+	+	○	○	○	+
V	+	○	○	○	+	+	+	○	○	○	+
W	○	○	○	○	+	+	+	○	○	○	○
Y	+	+	+	+	+	+	+	+	+	+	+
AA	+	+	+	+	+	+	+	+	+	+	+
AB	○	○	+	○	+	+	+	○	+	○	○

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.9 Quad-stacked / Quad-die DDR3 SDRAM x16 Ballout using MO-207 (Cont'd)

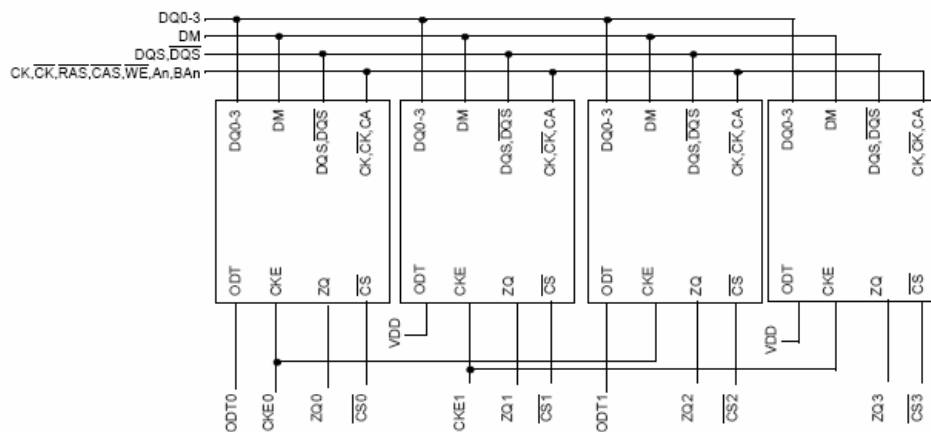


Figure 1 — Qual-stacked / Quad-die DDR3 SDRAM x4 rank association

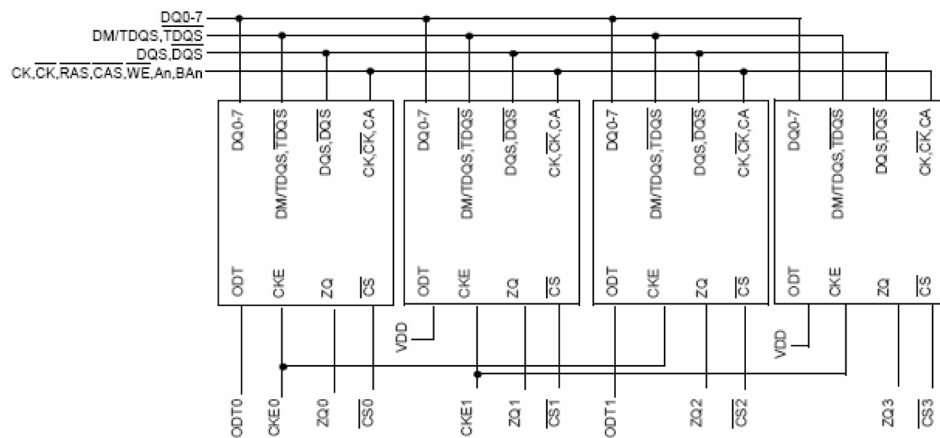


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

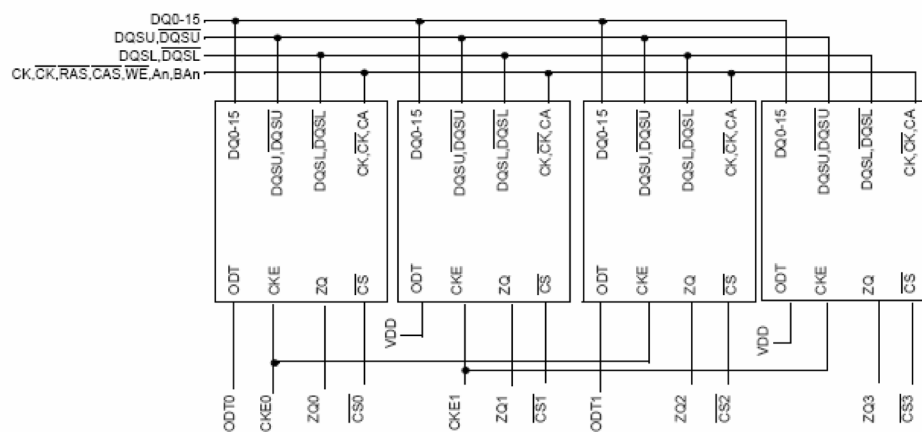


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.10 Pinout Description

Table 1 — Input/output functional description

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC#	Input	Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET#	Input	Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of V _{DD} , i.e., 1.20V for DC high and 0.30V for DC low.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, DQS#, DQSU, DQSU#, DQSL, DQSL#	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)**2.10 Pinout Description (Cont'd)****Table 1 — Input/output functional description (Cont'd)**

Symbol	Type	Function
TDQS, TDQS#	Output	Termination Data Strobe: TDQS/TDQS# is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS# that is applied to DQS/DQS#. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS# is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
V _{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V _{SSQ}	Supply	DQ Ground
V _{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V
V _{SS}	Supply	Ground
V _{REFDQ}	Supply	Reference voltage for DQ
V _{REFCA}	Supply	Reference voltage for CA
ZQ, (ZQ0), (ZQ1), (ZQ2), (ZQ3)	Supply	Reference Pin for ZQ calibration
NOTE: Input only pins (BA0-BA2, A0-A15, RAS#, CAS#, WE#, CS#, CKE, ODT, and RESET#) do not supply termination.		

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.11 DDR3 SDRAM Addressing

2.11.1 512Mb

Configuration	128Mb x 4	64Mb x 8	32Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BC switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A12	A0 - A12	A0 - A11
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size ¹	1 KB	1 KB	2 KB

2.11.2 1Gb

Configuration	256Mb x 4	128Mb x 8	64Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BC switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A13	A0 - A13	A0 - A12
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size ¹	1 KB	1 KB	2 KB

2.11.3 2Gb

Configuration	512Mb x 4	256Mb x 8	128Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BC switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A14	A0 - A14	A0 - A13
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size ¹	1 KB	1 KB	2 KB

2.11.4 4Gb

Configuration	1Gb x 4	512Mb x 8	256Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BC switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A15	A0 - A15	A0 - A14
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size ¹	1 KB	1 KB	2 KB

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.11 DDR3 SDRAM Addressing (Cont'd)

2.11.5 8Gb

Configuration	2Gb x 4	1Gb x 8	512Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BC switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A15	A0 - A15	A0 - A15
Column Address	A0 - A9, A11, A13	A0 - A9, A11	A0 - A9
Page size ¹	2 KB	2 KB	2 KB

NOTE 1. Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

$$\text{page size} = 2^{\text{COLBITS}} * \text{ORG} \div 8$$

where

COLBITS = the number of column address bits

ORG = the number of I/O (DQ) bits

3 Functional Description

3.1 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

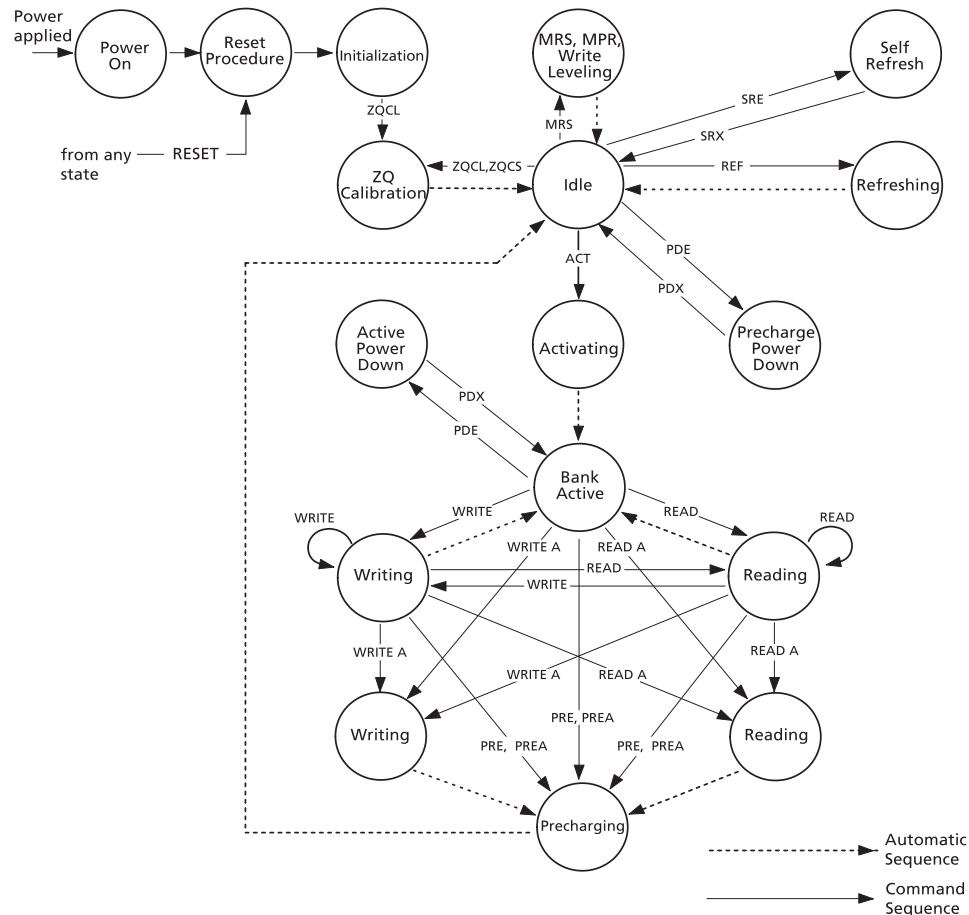


Figure 4 — Simplified State Diagram

Table 2 — State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-

NOTE: See "Command Truth Table" on page 33 for more details.

3 Functional Description (Cont'd)

3.2 Basic Functionality

The DDR3 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses a $8n$ prefetch architecture to achieve high-speed operation. The $8n$ prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single $8n$ -bit wide, four clock data transfer at the internal DRAM core and eight corresponding n -bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A15 select the row; refer to "DDR3 SDRAM Addressing" on page 15 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

3 Functional Description (Cont'd)

3.3 RESET and Initialization Procedure

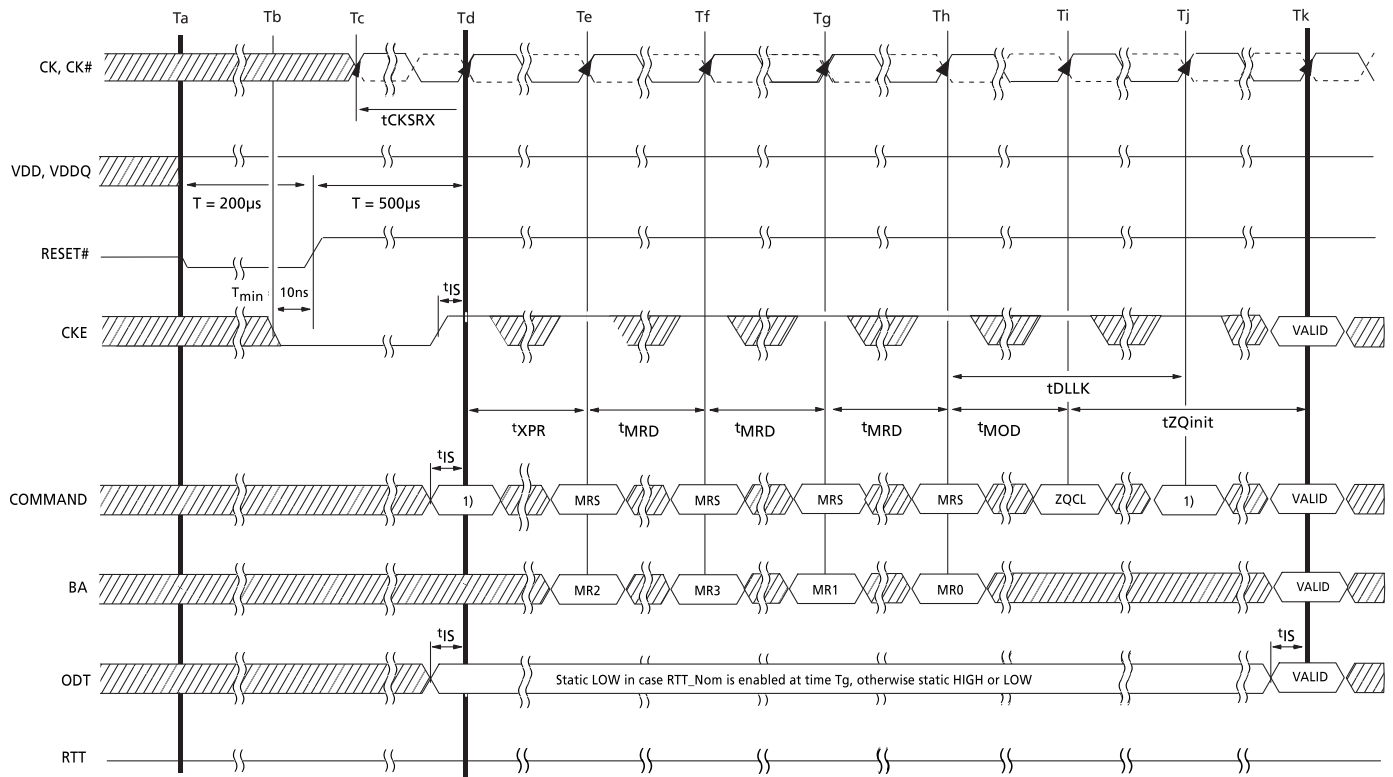
3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below $0.2 \times VDD$; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 μ s with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mV to VDDmin must be no greater than 200 ms; and during the ramp, $VDD > VDDQ$ and $(VDD - VDDQ) < 0.3$ volts.
 - VDD and VDDQ are driven from a single power converter output, AND
 - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
 - Vref tracks VDDQ/2.

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
 - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
 - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After RESET# is de-asserted, wait for another 500 μ s until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
 3. Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
 4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
 5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. ($tXPR = \max(tXS; 5 \times tCK)$)
 6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
 7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
 8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).
 9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
 10. Issue ZQCL command to starting ZQ calibration.
 11. Wait for both tDLLK and tZQinit completed.
 12. The DDR3 SDRAM is now ready for normal operation.

3.3 RESET and Initialization Procedure (Cont'd)**3.3.1 Power-up Initialization Sequence (Cont'd)**

NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK DON'T CARE

Figure 5 — Reset and Initialization Sequence at Power-on Ramping

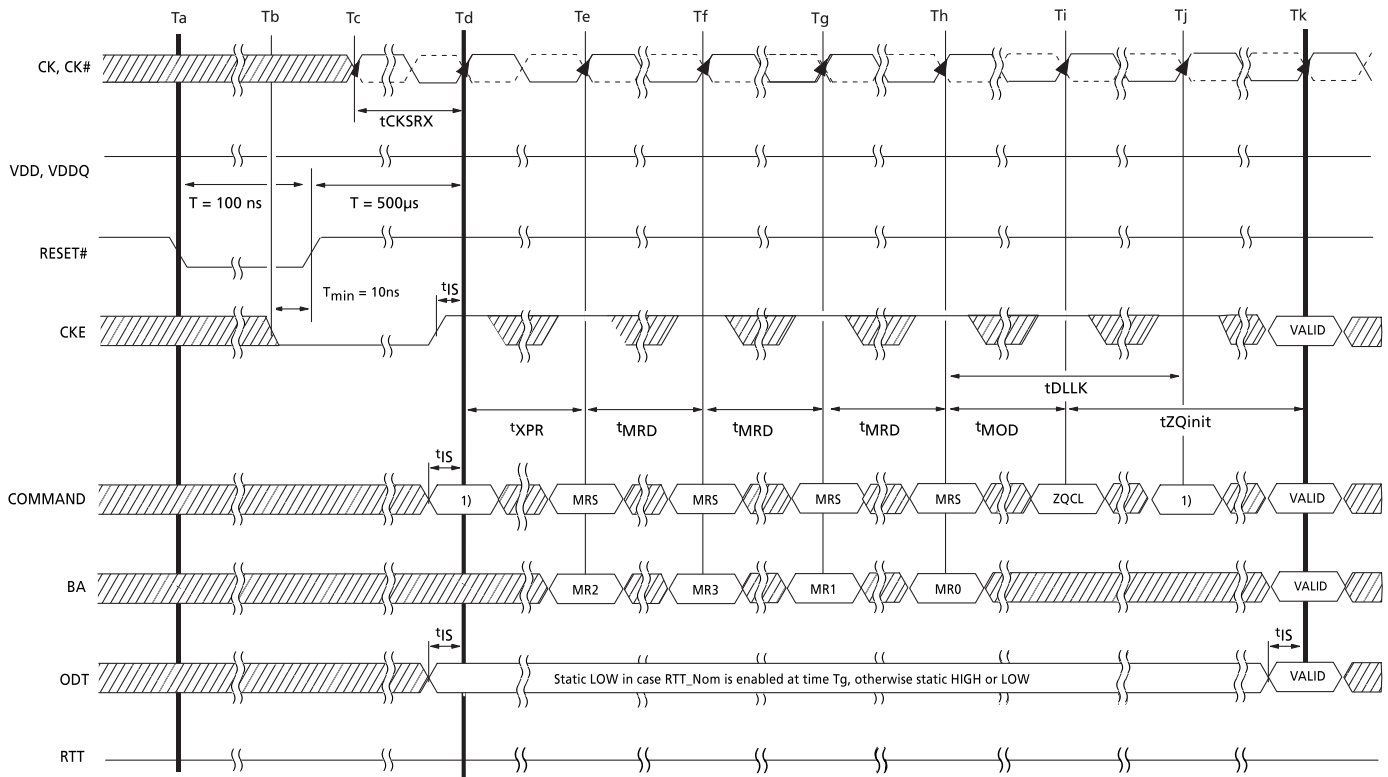
3 Functional Description (Cont'd)

3.3 RESET and Initialization Procedure (Cont'd)

3.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below $0.2 * VDD$ anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled "LOW" before RESET being de-asserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence steps 2 to 11.
3. The Reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK
DON'T CARE

Figure 6 — Reset Procedure at Power Stable Condition

3 Functional Description (Cont'd)

3.4 Register Definition

3.4.1 Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, t_{MRD} is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 7.

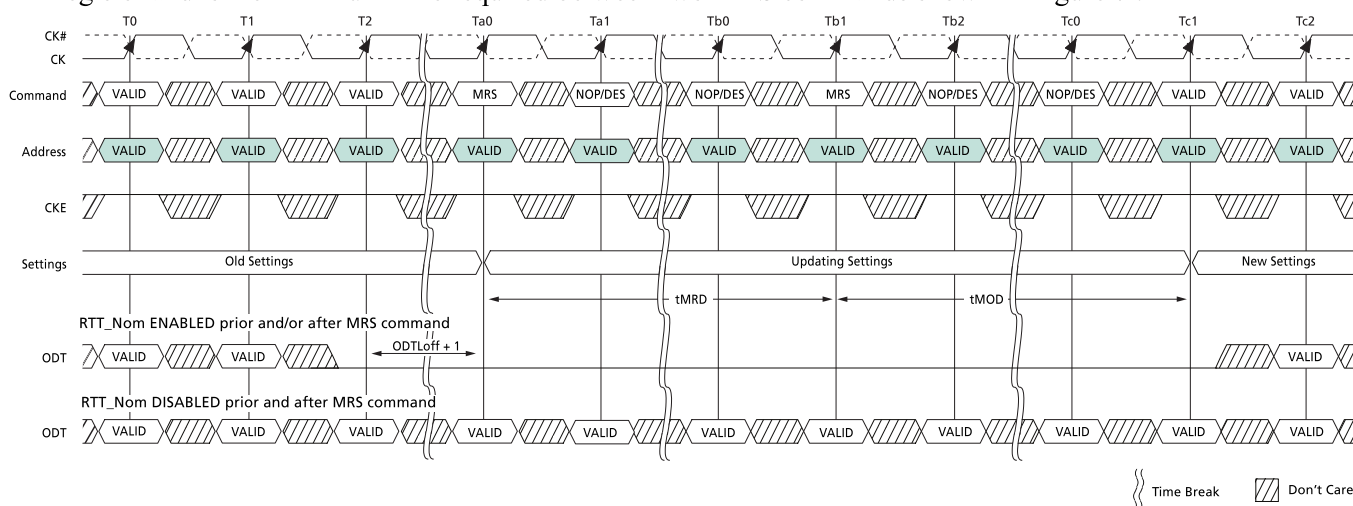


Figure 7 — t_{MRD} Timing

The MRS command to Non-MRS command delay, t_{MOD} , is required for the DRAM to update the features, except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure 8.

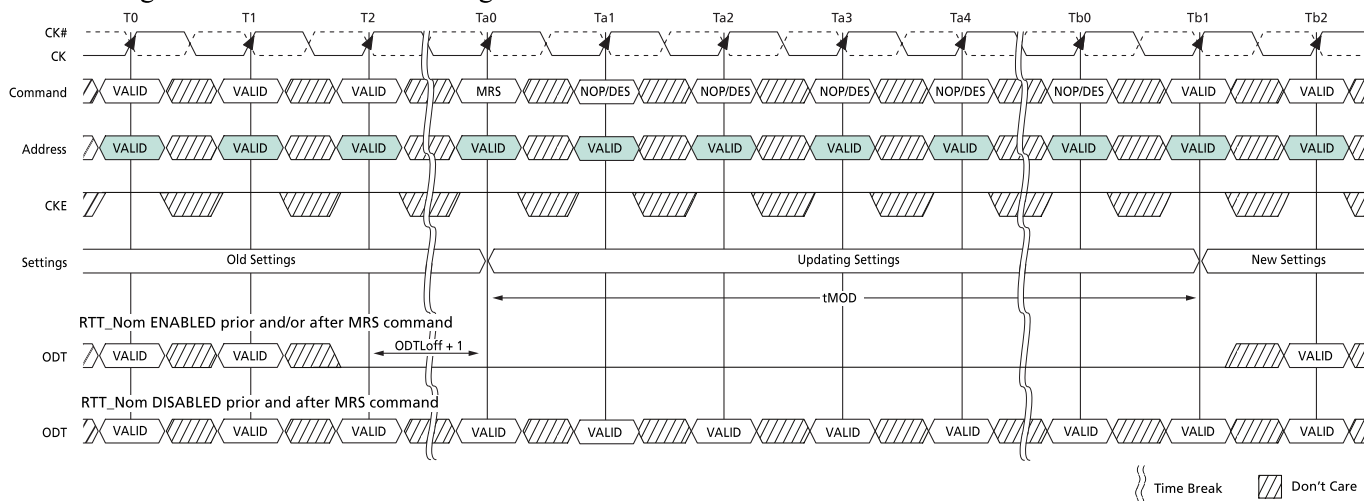


Figure 8 — t_{MOD} Timing

3.4 Register Definition (Cont'd)

3.4.1 Programming the Mode Registers (Cont'd)

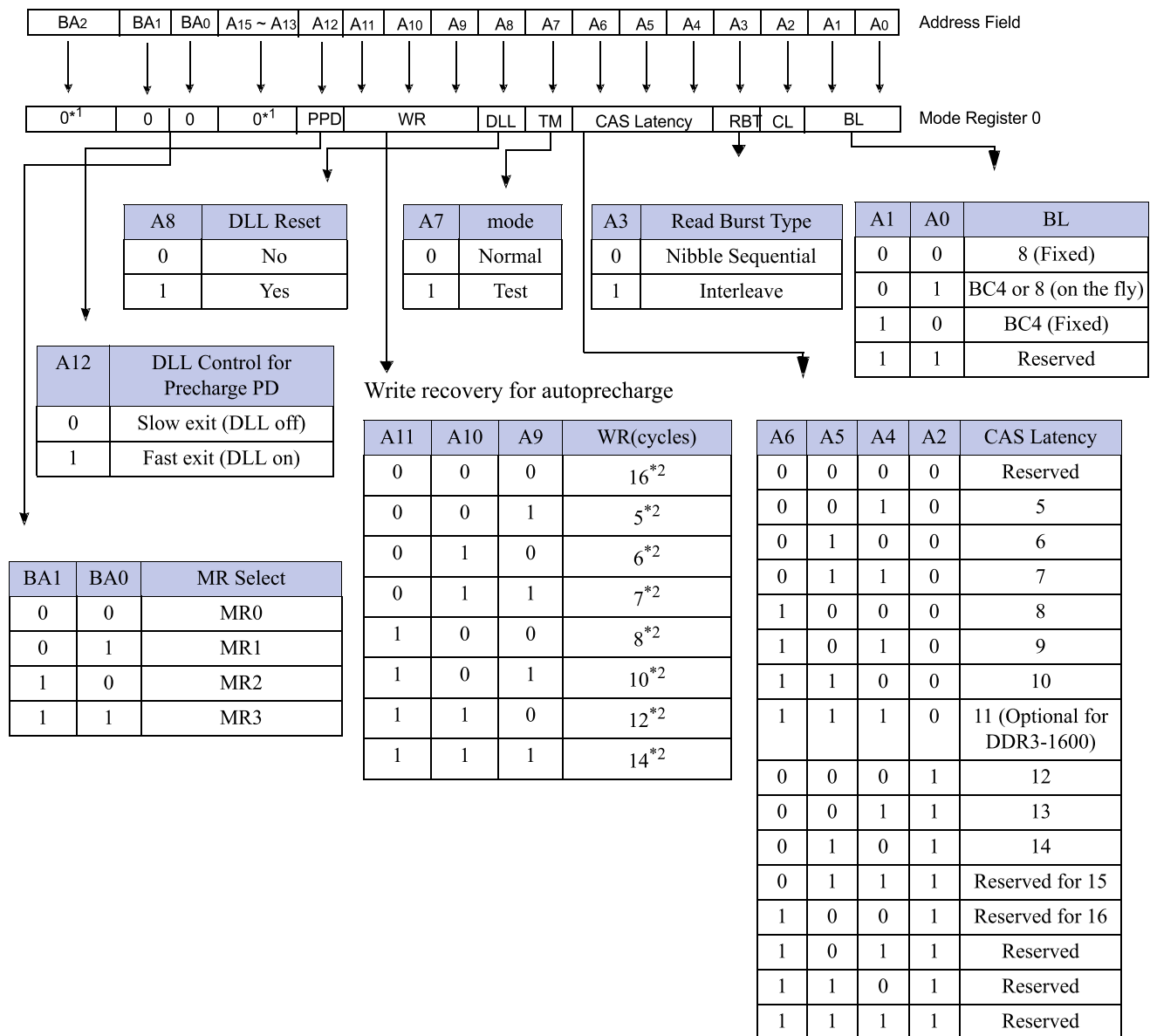
The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the RTT_NOM Feature is enabled in the Mode Register prior and/or after an MRS Command, the ODT Signal must continuously be registered LOW ensuring RTT is in an off State prior to the MRS command. The ODT Signal may be registered high after tMOD has expired. If the RTT_NOM Feature is disabled in the Mode Register prior and after an MRS command, the ODT Signal can be registered either LOW or HIGH before, during and after the MRS command. The mode registers are divided into various fields depending on the functionality and/or modes.

3.4.2 Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2,

3.4 Register Definition (Cont'd)**3.4.2 Mode Register MR0 (Cont'd)**

while controlling the states of address pins according to Figure 9.



*1: BA2 and A13~A15 are RFU and must be programmed to 0 during MRS.

*2: WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: $WR_{min}[\text{cycles}] = \text{Roundup}(tWR[\text{ns}] / tCK[\text{ns}])$. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

*3: The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency

*4: The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timingtable.

Figure 9 — MR0 Definition

3.4 Register Definition (Cont'd)**3.4.2 Mode Register MR0 (Cont'd)****3.4.2.1 Burst Length, Type and Order**

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 9. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 3. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and ‘on the fly’ which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

Table 3 — Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column ADDRESS (A2,A1,A0)	burst type = Sequential (decimal) A3 = 0	burst type = Interleaved (decimal) A3 = 1	Notes
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1, 2, 3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1, 2, 3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1, 2, 3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1, 2, 3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1, 2, 3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1, 2, 3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1, 2, 3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1, 2, 3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1, 2, 4, 5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1, 2, 4, 5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2, 4
NOTE 1 In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks. NOTE 2 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst. NOTE 3 T: Output driver for data and strobes are in high impedance. NOTE 4 V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins. NOTE 5 X: Don't Care.					

3.4.2.2 CAS Latency

The CAS Latency is defined by MR0 (bits A9-A11) as shown in Figure 9. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); $RL = AL + CL$. For more information on the supported CL and AL settings based on the operating clock frequency, refer to “Standard Speed Bins” on page 157. For detailed Read operation, refer to “READ Operation” on page 56.

3.4 Register Definition (Cont'd)

3.4.2 Mode Register MR0 (Cont'd)

3.4.2.3 Test Mode

The normal operating mode is selected by MR0 (bit A7 = 0) and all other bits set to the desired values shown in Figure 9. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is specified if A7 = 1.

3.4.2.4 DLL Reset

The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

3.4.2.5 Write Recovery

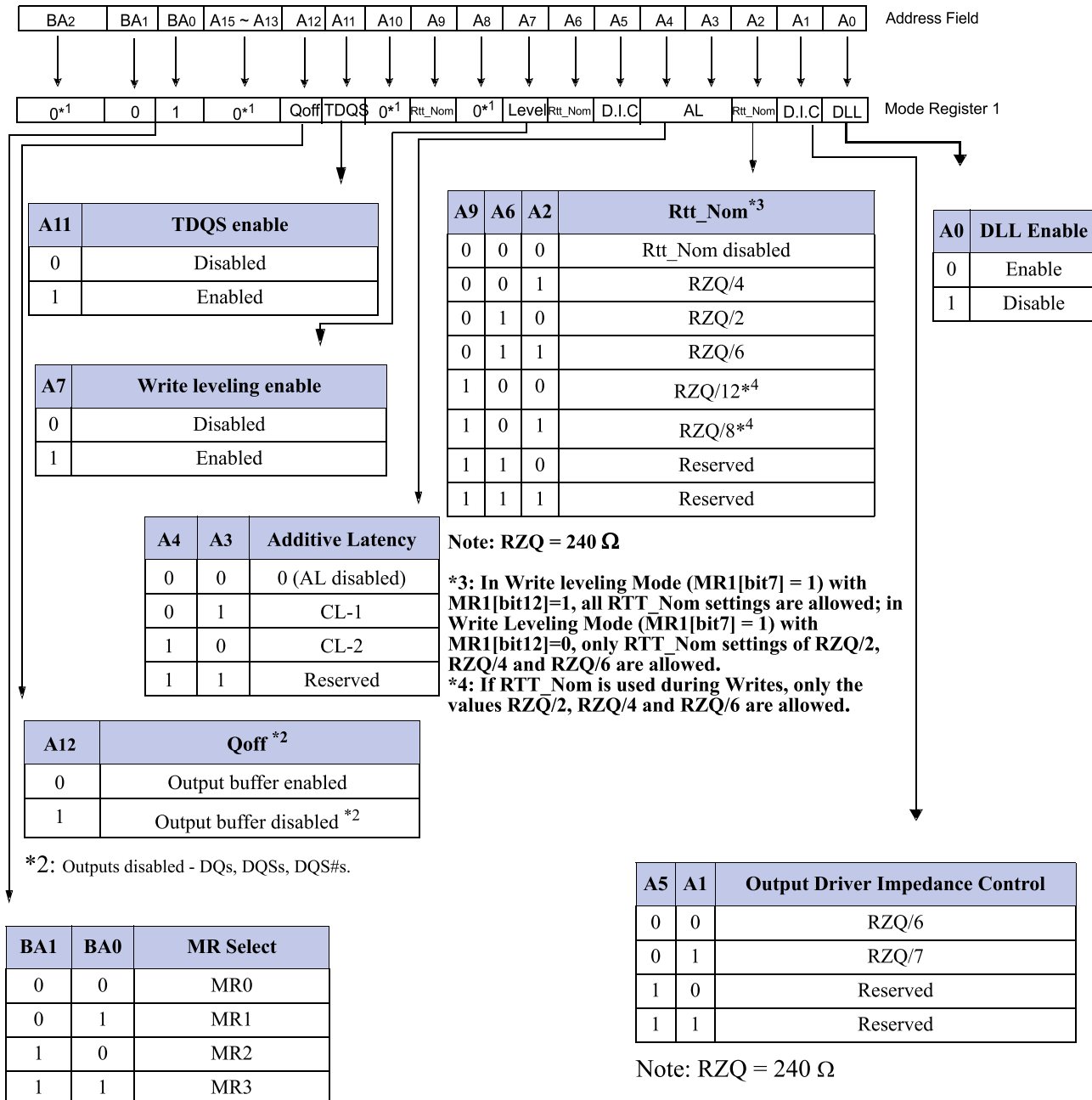
The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: $WR_{min}[\text{cycles}] = \text{Roundup}(tWR[\text{ns}] / tCK[\text{ns}])$. The WR must be programmed to be equal to or larger than tWR(min).

3.4.2.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

3 Functional Description (Cont'd)**3.4 Register Definition (Cont'd)****3.4.3 Mode Register MR1**

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to Figure 10.



^{*1} : BA2 and A8, A10, and A13 ~ A15 are RFU and must be programmed to 0 during MRS.

Figure 10 — MR1 Definition

3.4.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with

3.4 Register Definition (Cont'd)

3.4.3 Mode Register MR1 (Cont'd)

MR1 (A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to “DLL-off Mode” on page 37.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1 {A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

3.4.3.2 Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bits A1 and A5) as shown in Figure 10.

3.4.3.3 ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

3.4.3.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table 4.

Table 4 — Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL Disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

NOTE: AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register.

3.4.3.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a ‘write leveling’ feature to allow the controller to compensate for skew. See 4.8 “Write Leveling” on page 42 for more details.

3.4 Register Definition (Cont'd)

3.4.3 Mode Register MR1 (Cont'd)

3.4.3.6 Output Disable

The DDR3 SDRAM outputs may be enabled/disabled by MR1 (bit A12) as shown in Figure 10. When this feature is enabled ($A12 = 1$), all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device, thus removing any loading of the output drivers. This feature may be useful when measuring module power, for example. For normal operation, A12 should be set to '0'.

3.4.3.7 TDQS, TDQS#

TDQS (Termination Data Strobe) is a feature of X8 DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

TDQS is not supported in X4 or X16 configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS/TDQS# pins that is applied to the DQS/DQS# pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the TDQS# pin is not used. See Table 5 for details.

The TDQS function is available in X8 DDR3 SDRAM only and must be disabled via the mode register $A11=0$ in MR1 for X4 and X16 configurations.

Table 5 — TDQS, TDQS# Function Matrix

MR1 (A11)	DM / TDQS	NU / TDQS
0 (TDQS Disabled)	DM	Hi-Z
1 (TDQS Enabled)	TDQS	TDQS#

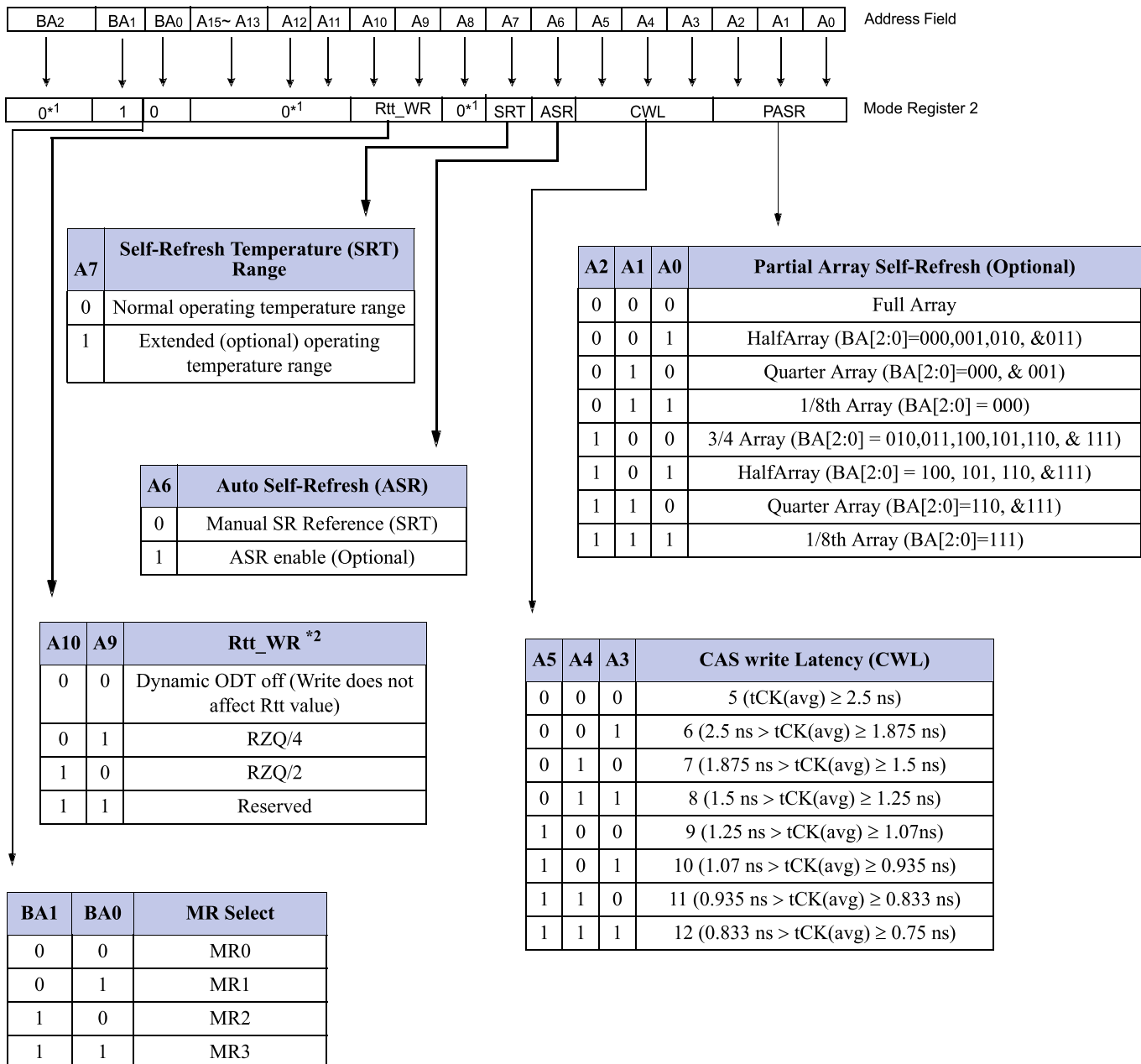
NOTE 1 If TDQS is enabled, the DM function is disabled.

NOTE 2 When not used, TDQS function can be disabled to save termination power.

NOTE 3 TDQS function is only available for X8 DRAM and must be disabled for X4 and X16.

3 Functional Description (Cont'd)**3.4 Register Definition (Cont'd)****3.4.4 Mode Register MR2**

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

MR2 Programming

* 1 : BA2, A5, A8, A11 ~ A15 are RFU and must be programmed to 0 during MRS.

* 2 : The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.
During write leveling, Dynamic ODT is not available.

Figure 11 — MR2 Definition

3.4 Register Definition (Cont'd)

3.4.4 Mode Register MR2 (Cont'd)

3.4.4.1 Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 11 will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

3.4.4.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 11. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); $WL = AL + CWL$. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to “Standard Speed Bins” on page 157. For detailed Write operation refer to “WRITE Operation” on page 68.

3.4.4.3 Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to “Extended Temperature Usage” on page 46. DDR3 SDRAMs must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

3.4.4.4 Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to “Dynamic ODT” on page 94.

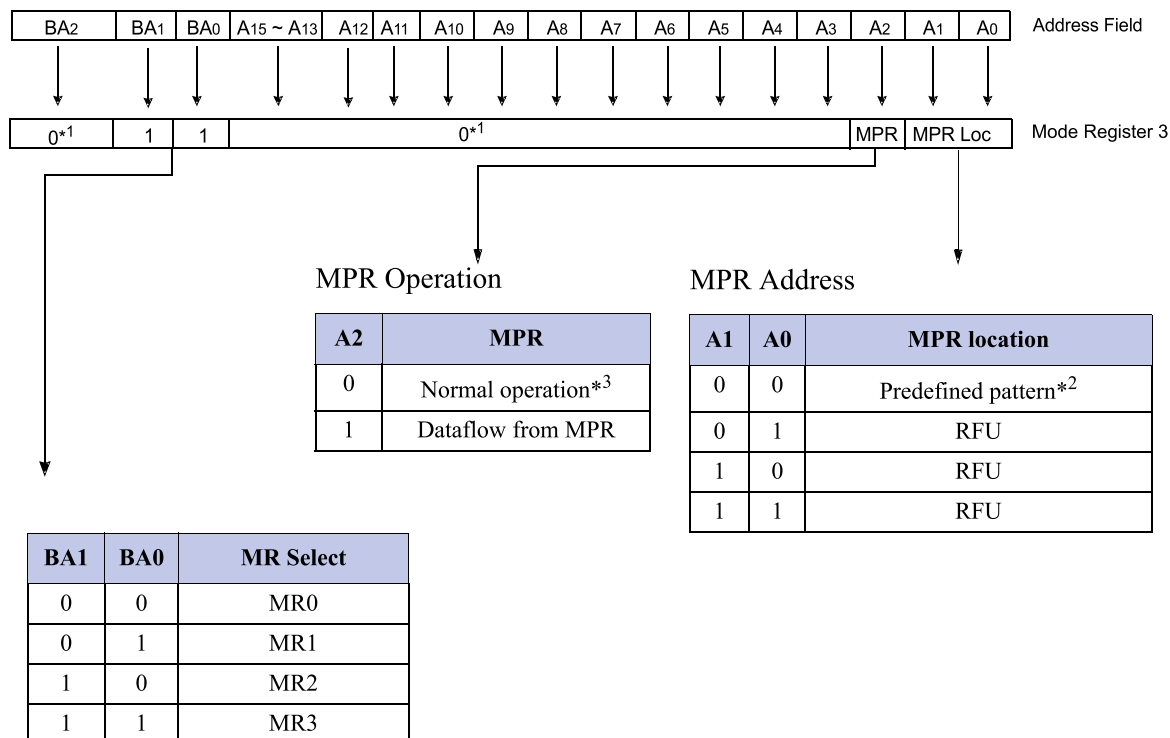
3 Functional Description (Cont'd)

3.4 Register Definition (Cont'd)

3.4.5 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

MR3 Programming



* 1 : BA2, A3 - A15 are RFU and must be programmed to 0 during MRS.

* 2 : The predefined pattern will be used for read synchronization.

* 3 : When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

Figure 12 — MR3 Definition

3.4.5.1 Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to “Multi Purpose Register” on page 48.

4 DDR3 SDRAM Command Description and Operation

4.1 Command Truth Table

Notes 1, 2, 3, and 4 apply to the entire Command Truth Table

Note 5 applies to all Read/Write commands

[BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid]

Table 6 — Command Truth Table

Function	Abbrevia tion	CKE		CS#	RAS#	CAS#	WE#	BA0- BA2	A13- A15	A12- BC#	A10- AP	A0- A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9, 12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

4 DDR3 SDRAM Command Description and Operation (Cont'd)

4.1 Command Truth Table (Cont'd)

Table 6 — Command Truth Table (Cont'd)

Function	Abbrevia tion	CKE		CS#	RAS#	CAS#	WE#	BA0- BA2	A13- A15	A12- BC#	A10- AP	A0- A9, A11	Notes
		Previous Cycle	Current Cycle										
NOTE 1 All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.													
NOTE 2 RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.													
NOTE 3 Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.													
NOTE 4 “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.													
NOTE 5 Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.													
NOTE 6 The Power Down Mode does not perform any refresh operation.													
NOTE 7 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.													
NOTE 8 Self Refresh Exit is asynchronous.													
NOTE 9 VREF(Both VrefDQ and VrefCA) must be maintained during Self Refresh operation. VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.													
NOTE 10 The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.													
NOTE 11 The Deselect command performs the same function as No Operation command.													
NOTE 12 Refer to the CKE Truth Table for more detail with CKE transition.													

4 DDR3 SDRAM Command Description and Operation (Cont'd)**4.2 CKE Truth Table**

Notes 1-7 apply to the entire CKE Truth Table.

For Power-down entry and exit parameters See 4.17 “Power-Down Modes” on page 81.

CKE low is allowed only if tMRD and tMOD are satisfied.

Table 7 — CKE Truth Table

Current State ²	CKE		Command (N) ³ RAS#, CAS#, WE#, CS#	Action (N) ³	Notes
	Previous Cycle ¹ (N-1)	Current Cycle ¹ (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT or NOP	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	11,13,14,18
	H	L	REFRESH	Self-Refresh	9,13,18
For more details with all signals See 4.1 “Command Truth Table” on page 33.					10
NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge. NOTE 2 Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N. NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here. NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document. NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh. NOTE 6 During any CKE transition (registration of CKE H->L or CKE L->H) the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again). NOTE 7 DESELECT and NOP are defined in the Command Truth Table. NOTE 8 On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied. NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state. NOTE 10 Must be a legal command as defined in the Command Truth Table. NOTE 11 Valid commands for Power-Down Entry and Exit are NOP and DESELECT only. NOTE 12 Valid commands for Self-Refresh Exit are NOP and DESELECT only. NOTE 13 Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See 4.16 “Self-Refresh Operation” on page 79 and See 4.17 “Power-Down Modes” on page 81.					

4 DDR3 SDRAM Command Description and Operation (Cont'd)

4.2 CKE Truth Table (Cont'd)

Table 7 — CKE Truth Table (Cont'd)

Current State ²	CKE		Command (N) ³ RAS#, CAS#, WE#, CS#	Action (N) ³	Notes
	Previous Cycle ¹ (N-1)	Current Cycle ¹ (N)			
NOTE 14 The Power-Down does not perform any refresh operations.					
NOTE 15 “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.					
NOTE 16 VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.					
NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.					
NOTE 18 ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).					

4.3 No OPeration (NOP) Command

The No OPeration (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# LOW and RAS#, CAS#, and WE# HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

4.4 Deselect Command

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.