

JEDEC STANDARD

Addendum No. 1 to JESD79-4, 3D Stacked DRAM

JESD79-4-1B

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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ADDENDUM No. 1 to JESD79-4, 3D STACKED SDRAM

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ADDENDUM No. 1 to JESD79-4, 3D STACKED SDRAM

(From JEDEC Board Ballots JCB-16-29, JCB-19-34, and JCB-21-08 formulated under the cognizance of the JC-42.3C Subcommittee on DRAM Parametrics.)

1 Scope

This document defines the 3DS DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a compliant 8 Gbit through 128 Gbit for x4, x8 3DS DDR4 SDRAM devices. This addendum was created based on the JESD79-4 DDR4 SDRAM specification. Each aspect of the changes for 3DS DDR4 SDRAM operation was considered. Any TBD's, as of the publication of this document, are under discussion by the formulating committee.

The requirement for 3DS devices compliant to this spec addendum is to have a single electrical load for the stacked devices no matter if the stack is comprised of 2, 4 or 8 devices. The I/O buffer circuitry can be built into the base SDRAM of the stack or into a separate logic buffer device. In either case (built in native circuitry or separate logic die), the assumption is that the I/O buffers are located at the bottom of the stack closest to the package substrate. All pictures and diagrams in the spec depict a primary die at the bottom of the stack; it is associated with logical rank 0.

2 3DS SDRAM Package Pinout and Addressing

2.1 Overview

These ballouts have been derived from JESD79-4. The ballout comprehends x4 and x8 data widths, where x4 is a subset of the x8 ballout, and the addressing described in this section.

2.2 Pinout Description

The following table only documents differences of DDR4 3DS SDRAMs relative to the pinout description in JESD79-4.

Symbol	Type	Function
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0 and C0, C1, C2. Input parity should maintain at the rising edge of the clock and at the same time with command and address with CS_n LOW

NOTE 1 Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, C0, C1, C2 and RESET_n) do not supply termination.

2.3 3D Stacked / DDR4 SDRAM x4 Ballout using MO-207

Ball locations in Figure 1, “3D Stacked DDR4 SDRAM x4 Ballout” show the proposed DDR4 3D Stacked SDRAM x4 ballout.

[X-ray view from package top surface]

		1	2	3	4	5	6	7	8	9	
		NC	NC	NC				NC		NC	NC
		NC	NC	NC				NC		NC	NC
A		NC	VDD	VSSQ	NC			NC	VSSQ	VSS	NC
B			VPP	VDDQ	DQS_c			DQ1	VDDQ	ZQ	
C			VDDQ	DQ0	DQS_t			VDD	VSS	VDDQ	
D			VSSQ	NC	DQ2			DQ3	NC	VSSQ	
E			VSS	VDDQ	NC			NC	VDDQ	VSS	
F			VDD	C2, NC ¹	ODT			CK_t	CK_c	VDD	
G			VSS	C0	CKE			CS_n	C1, NC ²	RFU	
H			VDD	WE_n, A14	ACT_n			CAS_n, A15	RAS_n, A16	VSS	
J			VREFCA	BG0	A10, AP			A12, BC_n	BG1	VDD	
K			VSS	BA0	A4			A3	BA1	VSS	
L			RESET_n	A6	A0			A1	A5	ALERT_n	
M			VDD	A8	A2			A9	A7	VPP	
N		NC	VSS	A11	PAR			A17, NC ³	A13	VDD	NC
		NC	NC	NC				NC		NC	NC
		NC	NC	NC				NC		NC	NC

1.This pin is not connected for 3DS devices with two or four logical ranks.

2.This pin is not connected for 3DS devices with two logical ranks.

3.This pin is not connected for 4Gb and 8Gb devices.

Figure 1 — 3D Stacked DDR4 SDRAM x4 Ballout

2.4 3D Stacked / DDR4 SDRAM x8 Ballout using MO-207

Ball locations in Figure 2, “3D Stacked DDR4 SDRAM x8 Ballout” show the proposed DDR4 3D Stacked SDRAM x8 ballout.

[X-ray view from package top surface]

	1	2	3	4	5	6	7	8	9	
	NC	NC	NC				NC		NC	NC
	NC	NC	NC				NC		NC	NC
A	NC	VDD	VSSQ	TDQS_c			DBI_n, TDQS_t	VSSQ	VSS	NC
B		VPP	VDDQ	DQS_c			DQ1	VDDQ	ZQ	
C		VDDQ	DQ0	DQS_t			VDD	VSS	VDDQ	
D		VSSQ	DQ4	DQ2			DQ3	DQ5	VSSQ	
E		VSS	VDDQ	DQ6			DQ7	VDDQ	VSS	
F		VDD	C2, NC ¹	ODT			CK_t	CK_c	VDD	
G		VSS	C0	CKE			CS_n	C1, NC ²	RFU	
H		VDD	WE_n, A14	ACT_n			CAS_n, A15	RAS_n, A16	VSS	
J		VREFCA	BG0	A10, AP			A12, BC_n	BG1	VDD	
K		VSS	BA0	A4			A3	BA1	VSS	
L		RESET_n	A6	A0			A1	A5	ALERT_n	
M		VDD	A8	A2			A9	A7	VPP	
N	NC	VSS	A11	PAR			NC	A13	VDD	NC
	NC	NC	NC				NC		NC	NC
	NC	NC	NC				NC		NC	NC

1.This pin is not connected for 3DS devices with two or four logical ranks.

2.This pin is not connected for 3DS devices with two logical ranks.

Figure 2 — 3D Stacked DDR4 SDRAM x8 Ballout

2.5 Logical Rank Addressing

The 3DS package is organized into two, four or eight logical ranks.

For DDR4 3DS devices, the logical ranks are selected by the Chip ID bus C[2:0].

The functional behavior of logical rank(s) should not deviate from monolithic DDR4 SDRAMs (specified in JESD79-4A), except when noted in this document. Each logical rank may be implemented as a single slice but the DDR4 3DS addendum doesn't require this to be the case.

2.6 3D Stack Organizations

Table 1, "Supported 3D Stack Organizations," indicates valid configurations supported by the DDR4 3DS addendum.

Table 1 — Supported 3D Stack Organizations

Logical Ranks	# of CS_n	Chip ID	# of CKE	# of ODT
2	1	C0	1	1
4	1	C0, C1	1	1
8	1	C0, C1, C2	1	1

Figure 3, Figure 4, and Figure 5 show one architectural diagram per row of Table 1. For the names of the these figures the standard *3DS configuration notation* LR-CS-CKE-ODT is used where LR indicates the number of logical ranks, CS_n indicates the number of chip select inputs, CKE indicates the number of CKE inputs and ODT indicates the number of ODT inputs. Since there is only one valid configuration for each number of logical ranks, this document will typical use the abbreviations 2H, 4H and 8H to describe 3DS devices with two, four or eight logical ranks.

2.7 3DS SDRAM System Addressing

3DS addressing scheme for DDR4 3DS devices is explained in section 2.8. This document comprehends using these 3DS devices in RDIMM and LRDIMM applications with x4 or x8 3DS SDRAMs.

2.8 **DDR4 3DS Stack Addressing Table**

Table 2, Table 3 and Table 4 indicate the address and select pins that are used for different configurations of 3DS stacks.

The DDR4 3DS devices may be derived from monolithic DDR4 devices. Therefore the address signals used within a logical rank are identical to the address signals used by a monolithic DRAM of the same density. Logical Rank 0 is considered to be associated with the primary die.

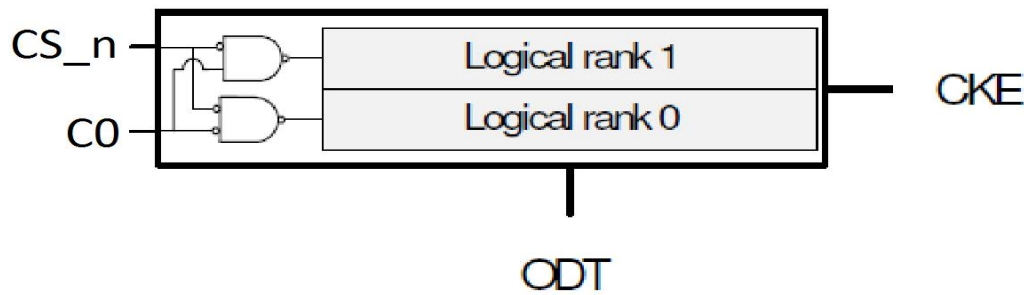


Figure 3 — 2-1-1-1 Device (2H)

Table 2 — DDR4 Address Table: 2H Stacked SDRAM

DDR4 3DS Address Table: 2H 3D Stacked SDRAM									
3DS Logical Rank Organization						3DS Package Organization			
Density	x4 Page Size	x8 Page Size	MSB Address			Capacity	Logical Rank	CS_n	C0
			Col	Row					
				x4 Die	x8 Die				
4 Gb	512 B	1 KB	A9	A15	A14	8 Gb	0	L	L
							1	L	H
8 Gb	512 B	1 KB	A9	A16	A15	16 Gb	0	L	L
							1	L	H
16 Gb	512 B	1 KB	A9	A17	A16	32 Gb	0	L	L
							1	L	H

2.8 DDR4 3DS Stack Addressing Table (cont'd)

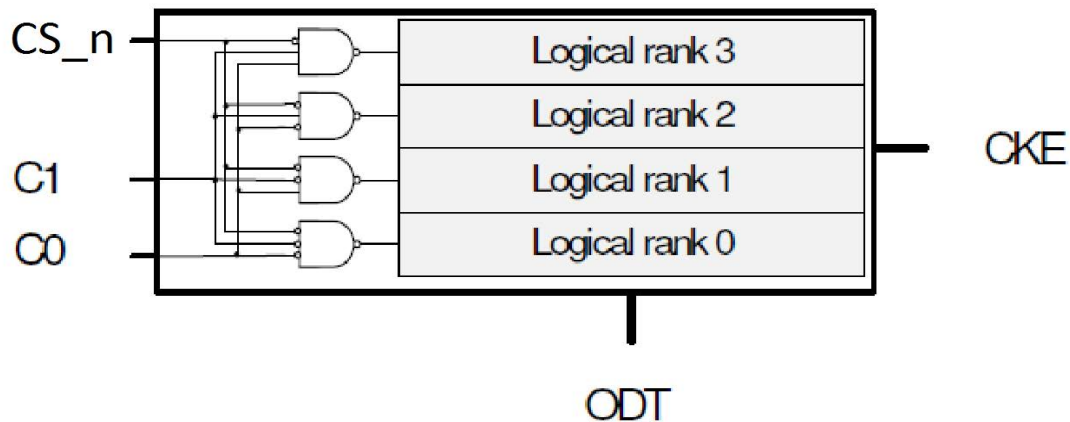


Figure 4 — 4-1-1-1 Device (4H)

Table 3 — DDR4 Address Table: 4H Stacked SDRAM

DDR4 3DS Address Table: 4H 3D Stacked SDRAM										
3DS Logical Rank Organization						3DS Package Organization				
Density	x4 Page Size	x8 Page Size	MSB Address			Capacity	Logical Rank	CS_n	C1	C0
			Col	Row						
				x4 Die	x8 Die					
4 Gb	512 B	1 KB	A9	A15	A14	16 Gb	0	L	L	L
							1	L	L	H
							2	L	H	L
							3	L	H	H
8 Gb	512 B	1 KB	A9	A16	A15	32 Gb	0	L	L	L
							1	L	L	H
							2	L	H	L
							3	L	H	H
16 Gb	512 B	1 KB	A9	A17	A16	64 Gb	0	L	L	L
							1	L	L	H
							2	L	H	L
							3	L	H	H

2.8 DDR4 3DS Stack Addressing Table (cont'd)

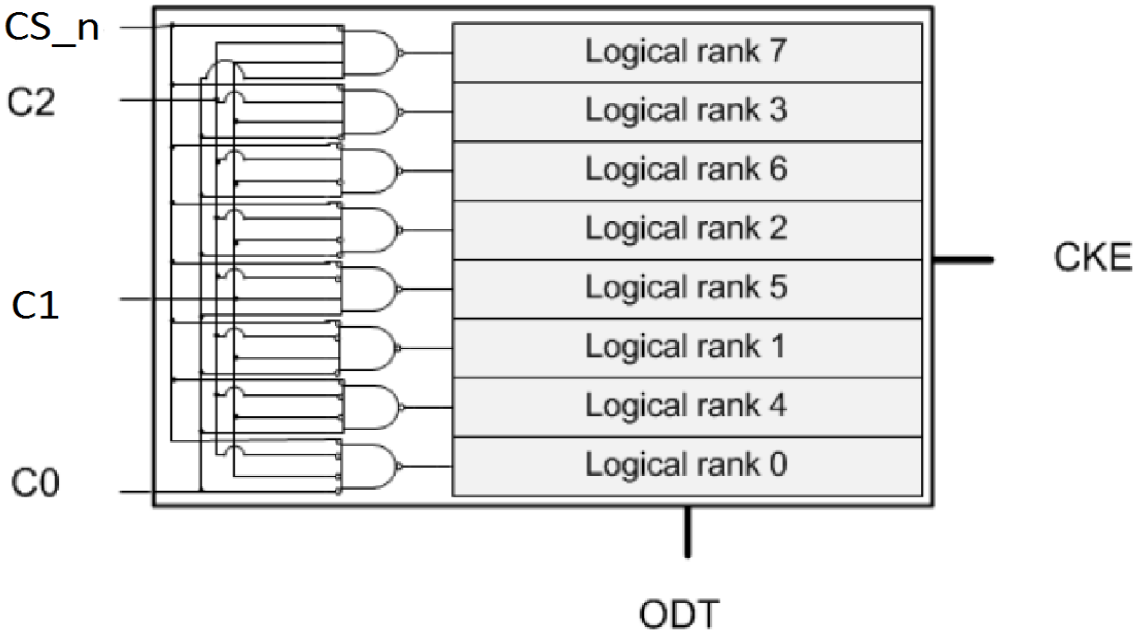


Figure 5 — 8-1-1-1 Device (8H)

2.8 DDR4 3DS Stack Addressing Table (cont'd)

Table 4 — DDR4 Address Table: 8H Stacked SDRAM

DDR4 3DS Address Table: 8H 3D Stacked SDRAM											
3DS Logical Rank Organization						3DS Package Organization					
Density	x4 Page Size	x8 Page Size	MSB Address			Capacity	Logical Rank	CS_n	C2	C1	C0
			Col	Row							
				x4 Die	x8 Die						
4 Gb	512 B	1 KB	A9	A15	A14	32 Gb	0	L	L	L	L
							1	L	L	L	H
							2	L	L	H	L
							3	L	L	H	H
							4	L	H	L	L
							5	L	H	L	H
							6	L	H	H	L
							7	L	H	H	H
8 Gb	512 B	1 KB	A9	A16	A15	64 Gb	0	L	L	L	L
							1	L	L	L	H
							2	L	L	H	L
							3	L	L	H	H
							4	L	H	L	L
							5	L	H	L	H
							6	L	H	H	L
							7	L	H	H	H
16 Gb	512 B	1 KB	A9	A17	A16	128 Gb	0	L	L	L	L
							1	L	L	L	H
							2	L	L	H	L
							3	L	L	H	H
							4	L	H	L	L
							5	L	H	L	H
							6	L	H	H	L
							7	L	H	H	H

NOTE These diagrams show only the logical organizations of these devices. No 1:1 relationship to physical organizations is implied. The Logical Rank 0 is considered the “primary die”, regardless of its physical arrangement.

2.9 Logical Rank, Bank Group and Bank Selection

DDR4 3DS devices can accommodate up to 128 banks, organized into 32 independent bank groups of 4 dependent banks each. The 128 banks are distributed among 8 logical ranks, each of which has 16 banks, organized into 4 independent bank groups of 4 dependent banks each. Table 5 shows how the logical ranks and bank groups in a DDR4 3DS device are selected. Table 6 shows how the individual banks are selected.

Table 5 — Logical rank and Bank Group Selection

Logical Rank 7	31	30	29	28
Logical Rank 6	27	26	25	24
Logical Rank 5	23	22	21	20
Logical Rank 4	19	18	17	16
Logical Rank 3	15	14	13	12
Logical Rank 2	11	10	9	8
Logical Rank 1	7	6	5	4
Logical Rank 0	3	2	1	0

Address by BG[1:0] =

11	10	01	00
----	----	----	----

C2	C1	C0	CS_n
1	1	1	0
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

Table 6 — Bank Selection

Logical Rank 7	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Logical Rank 6	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Logical Rank 5	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Logical Rank 4	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Logical Rank 3	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Logical Rank 2	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Logical Rank 1	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Logical Rank 0	15	14	13	12	11	10	9	8	7	6	5	4	Bank Group 0			

Addressed by BA[1:0] =

11	10	01	00
----	----	----	----

Addressed by BG[1:0] =

11	10	01	00
----	----	----	----

3 Functional Description

3.1 Simplified State Diagram

There is no difference between the simplified state diagrams for DDR4 and 3DS DDR4. Situations involving more than one bank, and multiple logical ranks are not reflected in the simple state diagram for DDR4 and are not captured in full detail.

3.2 Basic Functionality

The 3DS DDR4 SDRAM is a 2H, 4H or 8H stacked high-speed dynamic random-access memory with each logical rank configured as a 16-bank SDRAM (organized into four bank groups of four banks each). The 3DS SDRAM has 32, 64 or 128 physical banks available internally, depending on the number of logical ranks. The 3DS DDR4 SDRAM retains the use of an 8n pre-fetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the 3DS DDR4 SDRAM consists of a single 8n-bit wide, one clock data transfer at the internal SDRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

3.3 Reset Signal and Initialization Procedure

Prior to normal operation, the 3DS DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

A single reset pin with a single load is available per 3DS device. It is expected that the entire stack of SDRAMs within the package reset as per DDR4 specification. After RESET_n is de-asserted, the SDRAM will start internal state initialization; this will be done independently of external clocks. All steps in the DDR4 initialization sequence must be followed. No additional steps are required for 3DS DDR4 devices but the unique nature of 3DS devices (which have a single external I/O structure shared by all logical ranks of the entire device) has to be considered when programming the SDRAM mode register bits (see next section for details).

3.4 Mode Register Definition

For application flexibility, various functions, features and modes are programmable in seven Mode Registers. One set of registers controls the entire stack regardless if the 3DS stack has two, four or eight logical ranks, and they must be programmed via a Mode Register Set (MRS) command.

For 3DS DDR4 stacks configured as n logical ranks, a single set of MRS registers is addressed by the Chip Select signal (CS_n) as shown in Table 7.

3.4 Mode Register Definition (cont'd)

Table 7 — Simplified Truth Table for MRS Command

DRAM Command	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	Notes
Mode Register Set	L	V	V	V	MRS	MRS	MRS	MRS	MRS	MRS	MRS	MRS	1
Mode Register Set	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	1
Any other command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	1

NOTE 1 "V" means H or L (but a defined logic level).

Programming the register fields for a stacked device has some special considerations. Waiting for tMRD is required between two MRS commands issued to a 3DS SDRAM. After an MRS command is given, waiting for tMOD is required before a non-MRS command can be issued to any of the logical ranks in the stack.

Due to the difference between CAS Latency and nRCD, DDR4 3DS devices require a different Additive Latency definition than mono DDR4 SDRAMs. The changes to MR1 are shown in Table 10.

Table 8 — MR0 Definition for DDR4 3DS

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A11:A9	WR and RTP	Write Recovery and Read to Precharge for auto precharge see respective table in JESD79-4)
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A12, A6:A4, A2	CAS Latency ²	(see Table 9)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency which device supports. A12 is an additional bit to encode for Cas Latency. Hence availability of A12=1 could depend on Device.

3.4 Mode Register Definition (cont'd)

Table 9 — CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25
1	0	0	0	1	26
1	0	0	1	0	27
1	0	0	1	1	28
1	0	1	0	0	Reserved for 29
1	0	1	0	1	30
1	0	1	1	0	Reserved for 31
1	0	1	1	1	32
1	1	0	0	0	Reserved

3.4 Mode Register Definition (cont'd)

Table 10 — MR1 Definition for DDR4 3DS

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ³
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff ¹	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see respective table in JESD79-4)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6, A5	RFU	0 = must be programmed to 0 during MRS
A4, A3	Additive Latency ⁴	00 = 0(AL disabled) 10 = CL-2 01 = Reserved 11 = CL-3
A2, A1	Output Driver Impedance Control	(see respective table in JESD79-4)
A0	DLL Enable	0 = Disable ² 1 = Enable

NOTE 1 Outputs disabled - DQs, DQS_ts, DQS_cs.

NOTE 2 States reversed to "0 as Disable" with respect to DDR3.

NOTE 3 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 4 When the gap between tAA and tRCD is bigger than 2 clock cycles, host should increment tRCD accordingly to use AL, knowing that DDR4 3DS only supports AL of CL-2 and CL-3.

3.4 Mode Register Definition (cont'd)

Table 11 — MR2 Definition for DDR4 3DS

Address	Operating Mode	Description	
BG1	RFU	0 = must be programmed to 0 during MRS	No change from JESD79-4
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹	
A17	RFU	0 = must be programmed to 0 during MRS	
A13	RFU	0 = must be programmed to 0 during MRS	
A12	Write CRC	0 = Disable 1 = Enable	
A11	RFU	0 = must be programmed to 0 during MRS	
A10:A9	RTT_WR	(see respective table in JESD79-4)	
A8	RFU	0 = must be programmed to 0 during MRS	
A7:A6	Low Power Array Self Refresh (LP ASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)	
A5:A3	CAS Write Latency (CWL)	(see respective table in JESD79-4)	
A2:A0	RFU	0 = must be programmed to 0 during MRS	

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

4 SDRAM Command Description and Operation

4.1 ACTIVATE Command

In a 3D Stacked DDR4 SDRAM the single chip select pin and the C[2:0] pins select the logical rank - see Table 12.

The value on the BA0 - BA1 and BG0 - BG1 inputs selects the bank, the chip ID inputs select the logical ranks and the address provided on inputs A0-A17 selects the row. This row remains open (or active) for accesses until a precharge command is issued to that bank in that logical rank. A PRECHARGE command must be issued (to that bank in that logical rank) before opening a different row in the same bank in the same logical rank.

The minimum time interval between successive ACTIVATE commands to the same bank of a DDR SDRAM is defined by tRC. The minimum time interval between successive ACTIVATE commands to different banks within the same bank group of a DDR4 SDRAM is defined by tRRD_L (Min). The minimum time interval between successive ACTIVATE commands to different banks within different bank groups of a DDR4 SDRAM is defined by tRRD_S (Min). For a DDR4 3DS device, the timing parameters that applies to successive ACTIVATE commands to different banks in the same logical rank are defined as tRRD_S_slr (Min) and tRRD_L_slr (Min). The timing parameter that applies to successive ACTIVATE commands to different logical ranks is defined as tRRD_dlr (Min).

No more than four bank ACTIVATE commands may be issued in a given tFAW_slr (Min) period to the same logical rank. For all logical ranks in a 3DS device, the tFAW_dlr timing constraint applies, i.e., no more than four bank ACTIVATE commands to the whole 3DS SDRAM may be issued in a given tFAW_dlr (Min) period.

The timing restrictions covering ACTIVATE commands are documented in Table 47.

Table 12 — Truth Table for ACTIVATE Command

Symbol	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7
ACTIVATE (ACT)	L	L	L	L	ACT	DES	DES	DES	DES	DES	DES	DES
ACTIVATE (ACT)	L	L	L	H	DES	ACT	DES	DES	DES	DES	DES	DES
ACTIVATE (ACT)	L	L	H	L	DES	DES	ACT	DES	DES	DES	DES	DES
ACTIVATE (ACT)	L	L	H	H	DES	DES	DES	ACT	DES	DES	DES	DES
ACTIVATE (ACT)	L	H	L	L	DES	DES	DES	DES	ACT	DES	DES	DES
ACTIVATE (ACT)	L	H	L	H	DES	DES	DES	DES	DES	ACT	DES	DES
ACTIVATE (ACT)	L	H	H	L	DES	DES	DES	DES	DES	DES	ACT	DES
ACTIVATE (ACT)	L	H	H	H	DES	DES	DES	DES	DES	DES	DES	ACT
Any command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES

NOTE "V" means H or L (but a defined logic level).