

JEDEC STANDARD

DDR4 SDRAM

JESD79-4D

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DDR4 SDRAM STANDARD

(From JEDEC Board Ballot JCB-21-07, formulated under the cognizance of the JC-42.3C Subcommittee on DRAM Memories.)

1 Scope

This document defines the DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 2 Gb through 16 Gb for x4, x8, and x16 DDR4 SDRAM devices. This standard was created based on the DDR3 standards (JESD79-3) and some aspects of the DDR and DDR2 standards (JESD79, JESD79-2).

Each aspect of the changes for DDR4 SDRAM operation were considered and approved by committee ballot(s). The accumulation of these ballots were then incorporated to prepare this JESD79-4 specifications, replacing whole sections and incorporating the changes into Functional Description and Operation.

2 DDR4 SDRAM Package Pinout and Addressing

2.1 DDR4 SDRAM Row for X4, X8 and X16

The DDR4 SDRAM x4/x8 component will have 13 electrical rows of balls. Electrical is defined as rows that contain signal ball or power/ground balls. There may be additional rows of inactive balls for mechanical support.

The DDR4 SDRAM x16 component will have 16 electrical rows of balls. There may be additional rows of inactive balls for mechanical support.

2.2 DDR4 SDRAM Ball Pitch

The DDR4 SDRAM component will use a ball pitch of 0.8 mm by 0.8 mm.
The number of depopulated columns is 3.

2.3 DDR4 SDRAM Columns for X4, X8, and X16

The DDR4 SDRAM x4/x8 and x16 component will have 6 electrical columns of balls in 2 sets of 3 columns.
There will be columns between the electrical columns where there are no balls populated. The number of these columns is 3.
Electrical is defined as columns that contain signal ball or power/ground balls. There may be additional columns of inactive balls for mechanical support.

2.4 DDR4 SDRAM X4/8 Ballout using MO-207

Table 1 — DDR4 SDRAM X4/8 Ballout using MO-207

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c ³				DM_n, DBI_n TDQS_t ² , (NC) ¹	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4 (NC) ¹	DQ2				DQ3	DQ5 (NC) ¹	VSSQ	D
E	VSS	VDDQ	DQ6 (NC) ¹				DQ7 (NC) ¹	VDDQ	VSS	E
F	VDD	(C2) ⁵ ODT1 ⁶	ODT				CK_t	CK_c	VDD	F
G	VSS	(C0) ⁵ CKE1 ⁶	CKE				CS_n	(C1) ⁵ (CS1_n) ⁶	TEN (NC) ⁷	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				A17 (NC) ⁴	A13	VDD	N

NOTE 1 These pins are not connected for the X4 configuration.

NOTE 2 TDQS_t is not valid for the x4 configuration.

NOTE 3 TDQS_c is not valid for the x4 configuration.

NOTE 4 A17 is only defined for the x4 configuration.

NOTE 5 These pins are for stacked component such as 3DS. For mono package, these pins are NC.

NOTE 6 ODT1 / CKE1 / CS1_n are used together only for DDP.

NOTE 7 TEN is optional for 8Gb and above. This pin is not connected if TEN is not supported.

MO-207 Variation DT-z (x4)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○

○ Populated ball
+ Ball not populated

MO-207 Variation DW-z (x4)
with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	○	+	+	+	○	+	○	○
B	+	+	+	+	+	+	+	+	+	+	+
C	○	○	+	○	+	+	+	○	+	○	○
D	+	+	+	+	+	+	+	+	+	+	+
E	+	+	+	+	+	+	+	+	+	+	+
F	○	○	○	○	+	+	+	○	○	○	○
G	+	○	○	○	+	+	+	○	○	○	+
H	+	○	○	○	+	+	+	○	○	○	+
J	+	○	○	○	+	+	+	○	○	○	+
K	+	○	○	○	+	+	+	○	○	○	+
L	+	○	○	○	+	+	+	○	○	○	+
M	+	○	○	○	+	+	+	○	○	○	+
N	+	○	○	○	+	+	+	○	○	○	+
P	+	○	○	○	+	+	+	○	○	○	+
R	+	○	○	○	+	+	+	○	○	○	+
T	+	○	○	○	+	+	+	○	○	○	+
U	+	○	○	○	+	+	+	○	○	○	+
V	○	○	○	○	+	+	+	○	○	○	○
W	+	+	+	+	+	+	+	+	+	+	+
Y	+	+	+	+	+	+	+	+	+	+	+
AA	○	○	+	○	+	+	+	○	+	○	○
AB	+	+	+	+	+	+	+	+	+	+	+
AC	○	○	+	○	+	+	+	○	+	○	○

Figure 1 — DDR4 Ball Assignments for the x4/8 component

2.5 DDR4 SDRAM X16 Ballout using MO-207

Table 2 — DDR4 SDRAM X16 Ballout using MO-207

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n/ A16	VDD	L
M	VREFCA	BG0	A10/ AP				A12/ BC_n	CAS_n/ A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T

MO - 207 Variation DU-z (x16)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○
P	○	○	○	+	+	+	○	○	○
R	○	○	○	+	+	+	○	○	○
T	○	○	○	+	+	+	○	○	○

○ Populated ball
+ Ball not populated

MO-207 Variation DY-z (x16)
with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	+	○	+	+	+	○	+	○	○
B	+	+	+	+	+	+	+	+	+	+	+
C	+	+	+	+	+	+	+	+	+	+	+
D	○	○	○	○	+	+	+	○	○	○	○
E	+	○	○	○	+	+	+	○	○	○	+
F	+	○	○	○	+	+	+	○	○	○	+
G	+	○	○	○	+	+	+	○	○	○	+
H	+	○	○	○	+	+	+	○	○	○	+
J	+	○	○	○	+	+	+	○	○	○	+
K	+	○	○	○	+	+	+	○	○	○	+
L	+	○	○	○	+	+	+	○	○	○	+
M	+	○	○	○	+	+	+	○	○	○	+
N	+	○	○	○	+	+	+	○	○	○	+
P	+	○	○	○	+	+	+	○	○	○	+
R	+	○	○	○	+	+	+	○	○	○	+
T	+	○	○	○	+	+	+	○	○	○	+
U	+	○	○	○	+	+	+	○	○	○	+
V	+	○	○	○	+	+	+	○	○	○	+
W	○	○	○	○	+	+	+	○	○	○	○
Y	+	+	+	+	+	+	+	+	+	+	+
AA	+	+	+	+	+	+	+	+	+	+	+
AB	○	○	+	○	+	+	+	○	+	○	○

Figure 2 — DDR4 Ball Assignments for the x16 component

2.6 DDR4 SDRAM X32 Ballout using MO-XXX

The DDR4 SDRAM x32 component will have the pin assignments as defined in Figure 3. Blank cells are no ball locations.

	1	2	3	4	5	6	7	8	9	10	11	
A	VPP	VDDQ	DQS0_t	DQS0_c	VDDQ		VDDQ	DQS1_c	DQS1_t	VDDQ	VDD	1
B	VSS	VSSQ	DQ0	DM0_n, DBI0_n, NC	VSSQ		VSSQ	DQ8	DQ9	VSSQ	VSS	2
C	VDD	DQ3	DQ2	DQ1				DQ10	DQ11	DQ12	VDDQ	3
D	VDDQ	DQ4	DQ5	VSSQ				VSSQ	DQ13	DQ15	VSSQ	4
E	VSSQ	DQ6	DQ7	VDDQ				VDDQ	DQ14	DM1_n, DBI1_n, NC	ZQ	5
F	VDD	ODT1	VDDQ	ODT				CK_t	VDDQ	CS1_n	VDD	6
G	VDD	CKE1	VSS	CKE				CK_c	VSS	TEN	VDD	7
H	VREFCA	BA0	ACT_n	WE_n/ A14				CS_n	RAS_n/ A16	BA1	RFU	8
J	VSS	A4	VSS	BG0				CAS_n/ A15	VSS	A3	VSS	9
K	RESET_n	A6	A0	A10/AP				A12/ BC_n	RFU	A5	ALERT_n	10
L	VDD	A8	VSS	A2				A1	VSS	A7	VDD	11
M	VDD	A11	VDDQ	PAR				A9	VDDQ	A13	VDD	12
N	ZQ1	DM3_n, DBI3_n, NC	DQ30	VDDQ				VDDQ	DQ23	DQ22	VSSQ	13
P	VSSQ	DQ31	DQ29	VSSQ				VSSQ	DQ21	DQ20	VDDQ	14
R	VDDQ	DQ28	DQ27	DQ26				DQ17	DQ18	DQ19	VDD	15
T	VSS	VSSQ	DQ25	DQ24	VSSQ		VSSQ	DM2_n, DBI2_n, NC	DQ16	VSSQ	VSS	16
U	VDD	VDDQ	DQS3_t	DQS3_c	VDDQ		VDDQ	DQS2_c	DQS2_t	VDDQ	VPP	17

NOTE ODT1, CKE1, CS1_n and ZQ1 are for packages containing two x32 die stacked. These pins are NC for all other configurations.

Figure 3 — DDR4 Ball Assignments for the x32 component

2.7 Pinout Description

Table 3 — Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQS_u_t, DQS_u_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DD} .

Table 3 — Pinout Description (Cont'd)

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0, and C0-C2 (3DS devices). Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is low.
ALERT_n	Input/Output	Alert: It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

NOTE Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

2.8 DDR4 SDRAM Addressing

Table 4 — 2 Gb Addressing Table

Configuration		512 Mb x4	256 Mb x8	128 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A14	A0~A13	A0~A13
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

Table 5 — 4 Gb Addressing Table

Configuration		1 Gb x4	512 Mb x8	256 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A15	A0~A14	A0~A14
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

Table 6 — 8 Gb Addressing Table

Configuration		2 Gb x4	1 Gb x8	512 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A16	A0~A15	A0~A15
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

Table 7 — 16 Gb Addressing Table

Configuration		4 Gb x4	2 Gb x8	1 Gb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A17	A0~A16	A0~A16
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

2.9 DDP Single Rank (SR) x16 from two x8

The Single Rank (SR) x16 DDP (Dual Die Package) is comprised of two x8 devices connected in parallel. The intent is to place two x8 devices in the physical footprint space of a x16. Unless noted otherwise, the functionality, operation, and timings of the SRx16 DDP are to be the same as the mono x8 device.

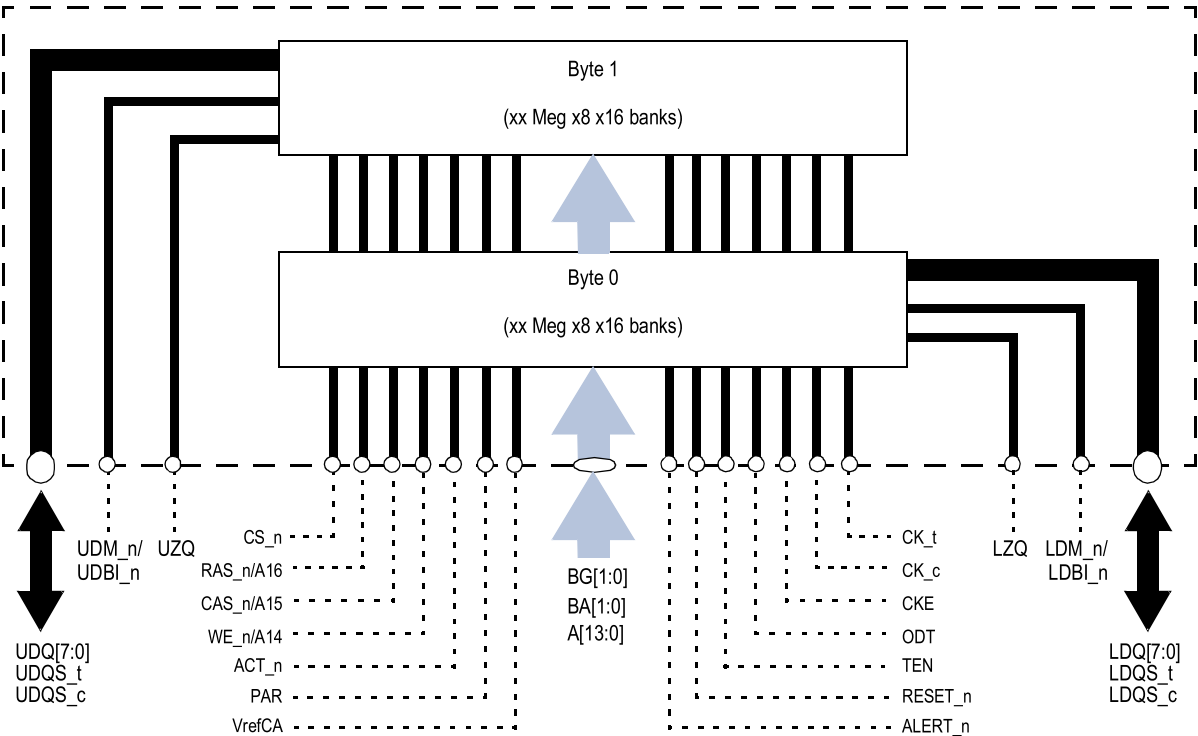


Figure 4 — Functional Block Diagram of SR x16 DDP

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n/ DBIL_n	VSSQ	UZQ	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	LZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n/ A16	VDD	L
M	VREFCA	BG0	A10/ AP				A12/ BC_n	CAS_n/ A15	BG1	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				VSS	A13	VDD	T

Figure 5 — Ballout of SR x16 DDP using MO-207

2.9 DDP Single Rank (SR) x16 from two x8 (cont'd)

Table 8 — 8Gb Addressing Table (SR x16 DDP)

Configuration		512Mb x 16
Bank Address	# of Bank Groups	4
	BG Address	BG0~BG1
	Bank Address in a BG	BA0~BA1
Row Address		A0~A14
Column Address		A0~A9
Page size - per array		1KB
Page size - package		2KB

Table 9 — 16Gb Addressing Table (SR x16 DDP)

Configuration		1Gb x 16
Bank Address	# of Bank Groups	4
	BG Address	BG0~BG1
	Bank Address in a BG	BA0~BA1
Row Address		A0~A15
Column Address		A0~A9
Page size - per array		1KB
Page size - package		2KB

Table 10 — 32Gb Addressing Table (SR x16 DDP)

Configuration		2Gb x 16
Bank Address	# of Bank Groups	4
	BG Address	BG0~BG1
	Bank Address in a BG	BA0~BA1
Row Address		A0~A16
Column Address		A0~A9
Page size - per array		1KB
Page size - package		2KB

3 Functional Description

3.1 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

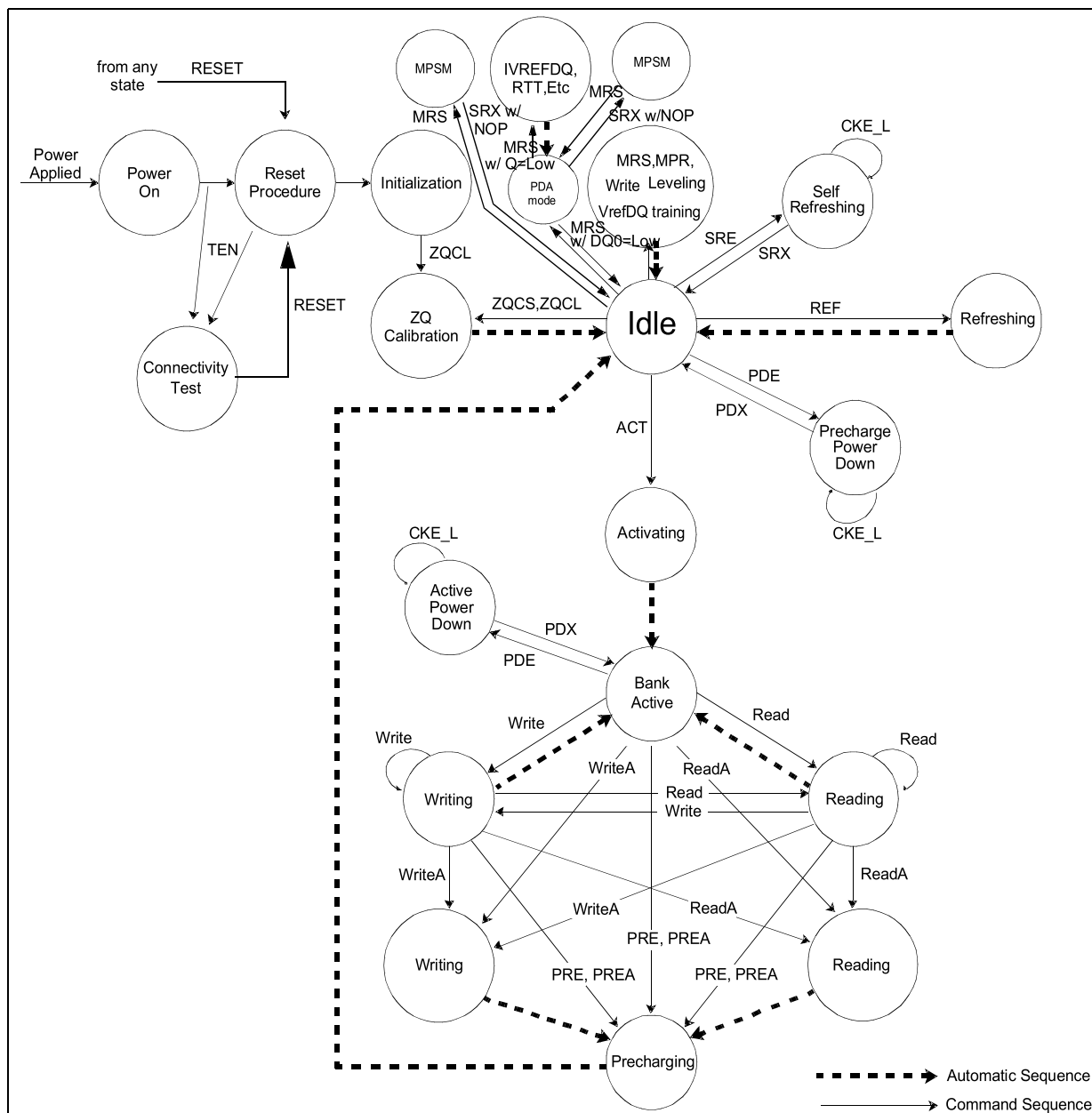


Figure 6 — Simplified State Diagram

3.1 Simplified State Diagram (cont'd)

Table 11 — Simplified State Diagram Functions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	PRECHARGE All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
REF	Refresh, Fine granularity Refresh	RESET_n	Start RESET procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

3.2 Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM.

The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.8 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

3.3 RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly default values for the following MR settings need to be defined.

Gear down mode (MR3 A[3]): 0 = 1/2 Rate

Per DRAM Addressability (MR3 A[4]): 0 = Disable

Max Power Saving Mode (MR4 A[1]): 0 = Disable

CS to Command/Address Latency (MR4 A[8:6]): 000 = Disable

CA Parity Latency Mode (MR5 A[2:0]): 000 = Disable

Hard Post Package Repair mode (MR4 A[13]): 0 = Disable

Soft Post Package Repair mode (MR4 A[5]): 0 = Disable

3.3.1 Power-up Initialization Sequence

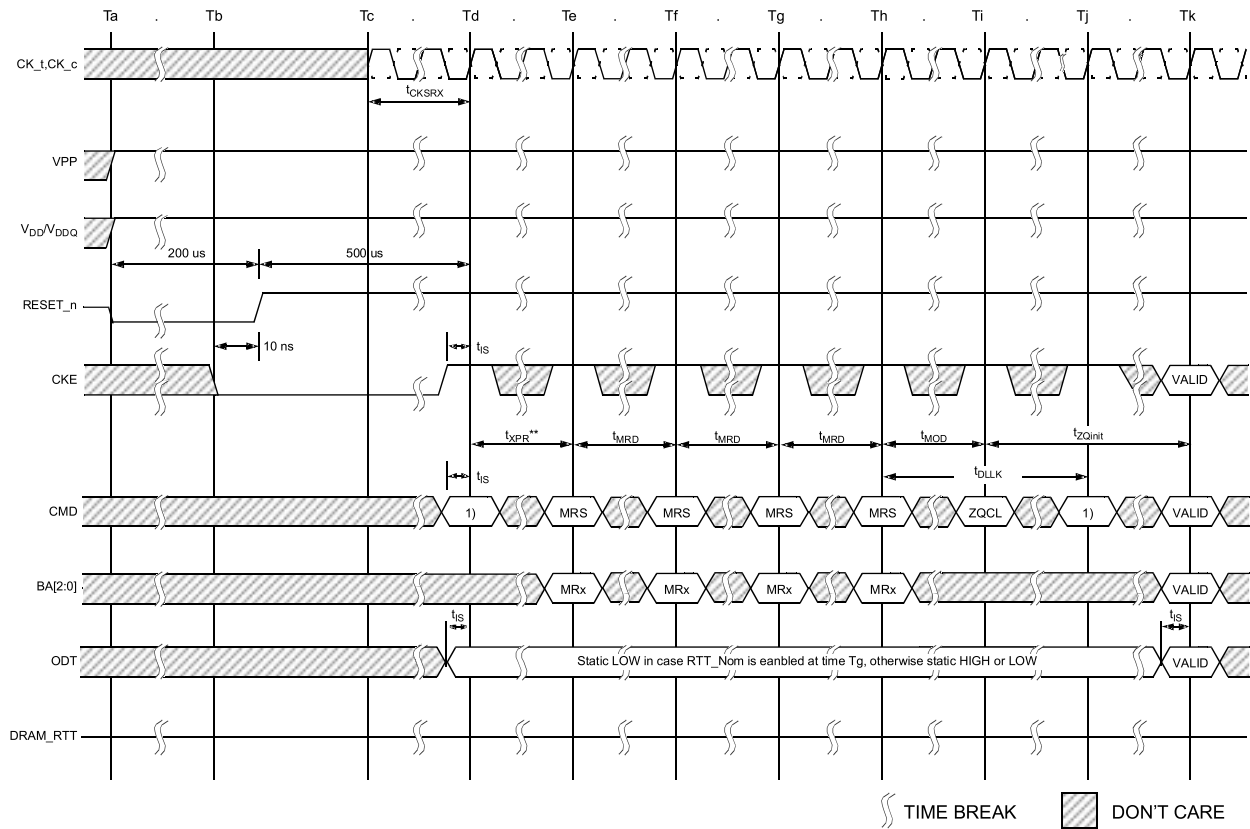
The following sequence is required for POWER UP and Initialization and is shown in Figure 7.

1. Apply power (RESET_n and TEN are recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained below 0.2 x VDD for minimum 200us with stable power and TEN needs to be maintained below 0.2 x VDD for minimum 700us with stable power. CKE is pulled "Low" anytime before RESET_n being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, V_{DD} ≥ V_{DDQ} and (V_{DD}-V_{DDQ}) < 0.3volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.
 - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
 - The voltage levels on all pins other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.76V max once power ramp is finished, AND
 - VrefCA tracks VDD/2.
 - or
 - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}

3.3.1 Power-up Initialization Sequence (cont'd)

- Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & V_{refCA} .
 - Apply V_{PP} without any slope reversal before or at the same time as V_{DD} .
 - The voltage levels on all pins other than V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After $RESET_n$ is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
 3. Clocks (CK_t , CK_c) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also, a Deselect command must be registered (with tIS set up time to clock) at clock edge Td. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit
 4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as $RESET_n$ is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after $RESET_n$ deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
 5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=Max(tXS, 5nCK))
 6. Issue MRS Command to load MR3 with all application settings(To issue MRS command to MR3, provide "Low" to BG0, "High" to BA1, BA0)
 7. Issue MRS command to load MR6 with all application settings (To issue MRS command to MR6, provide "Low" to BA0, "High" to BG0, BA1)
 8. Issue MRS command to load MR5 with all application settings (To issue MRS command to MR5, provide "Low" to BA1, "High" to BG0, BA0)
 9. Issue MRS command to load MR4 with all application settings (To issue MRS command to MR4, provide "Low" to BA1, BA0, "High" to BG0)
 10. Issue MRS command to load MR2 with all application settings (To issue MRS command to MR2, provide "Low" to BG0, BA0, "High" to BA1)
 11. Issue MRS command to load MR1 with all application settings (To issue MRS command to MR1, provide "Low" to BG0, BA1, "High" to BA0)
 12. Issue MRS command to load MR0 with all application settings (To issue MRS command to MR0, provide "Low" to BG0, BA1, BA0)
 13. Issue ZQCL command to starting ZQ calibration
 14. Wait for both tDLLK and tZQ init to be completed
 15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).
 16. Optional MBIST PPR mode can be entered by setting MR4:A0 to a "1", followed by subsequent MR0 guard key sequences, then DRAM will drive ALERT_n to LOW. DRAM will drive ALERT_n to HIGH to indicate that this operation is completed. MBIST PPR mode can take place anytime after Tk. Note that no exit sequence or re-initialization is needed after MBIST completes; as soon as ALERT_N goes HIGH and tIS is satisfied, MR0 must be re-written to the pre guard key state, then the DRAM is immediately ready to receive valid commands. Please refer to Ch 4.34 MBIST PPR for more detailed operation procedures.

3.3.1 Power-up Initialization Sequence (cont'd)



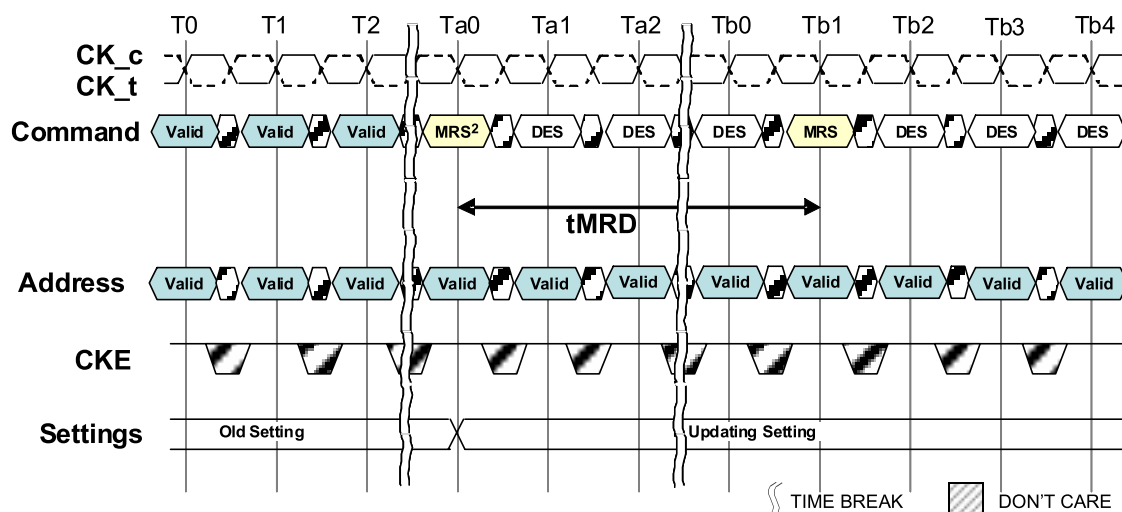
- NOTE 1 From time point 'Td' until 'Tk', DES commands must be applied between MRS and ZQCL commands.
NOTE 2 MRS Commands must be issued to all Mode Registers that have defined settings.
NOTE 3 Optional MBIST PPR should be entered anytime after Tk.

Figure 7 — RESET_n and Initialization Sequence at Power-on Ramping

3.4 Register Definition

3.4.1 Programming the mode registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also, the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. MRS Commands can be issued only when DRAM is at idle state. The mode register set command cycle time, t_{MRD} is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 9.



NOTE 1 This timing diagram shows C/A Parity Latency mode is "Disable" case.

NOTE 2 List of MRS commands exception that do not apply to t_{MRD}

- Gear down mode
- C/A Parity Latency mode
- CS to Command/Address Latency mode
- Per DRAM Addressability mode
- VrefDQ training Value, VrefDQ Training mode and VrefDQ training Range

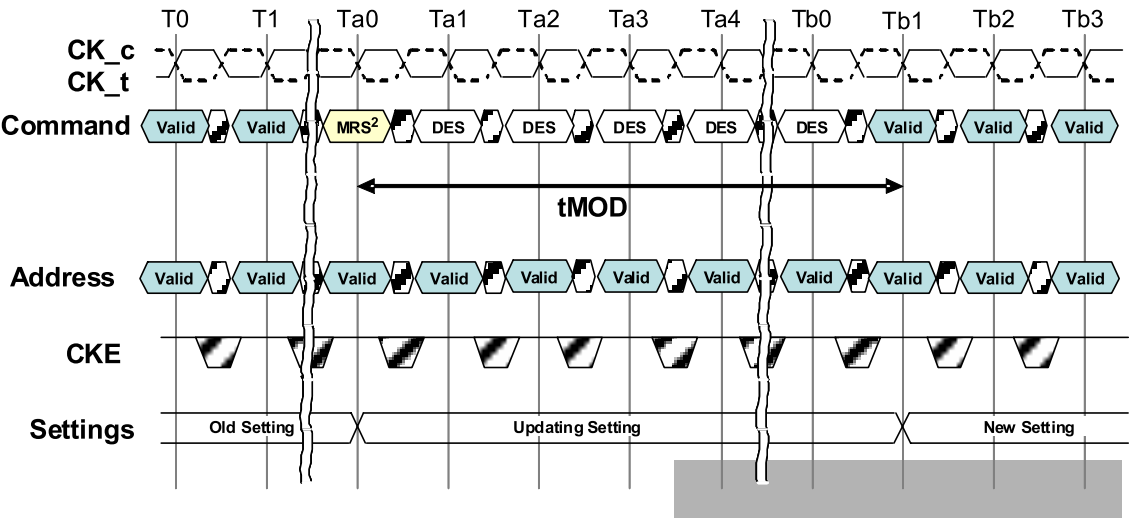
Figure 9 — t_{MRD} Timing

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.

The MRS commands which do not apply t_{MRD} timing to next MRS command are listed in Note 2 of Figure 9. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

The most MRS command to Non-MRS command delay, t_{MOD} , is required for the DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding DES shown in Figure 10.

3.4.1 Programming the mode registers (cont'd)

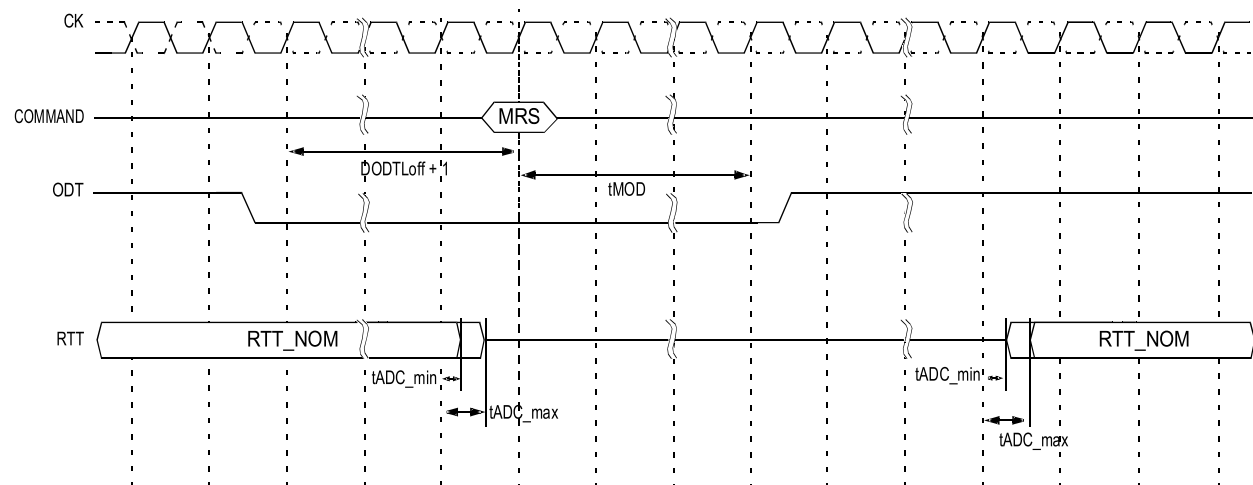


- NOTE 1 This timing diagram shows CA Parity Latency mode is "Disable" case.
- NOTE 2 List of MRS commands exception that do not apply to tMOD
- DLL Enable, DLL Reset
 - VrefDQ training Value, internal Vref Monitor, VrefDQ Training mode and VrefDQ training Range
 - Gear down mode
 - Per DRAM addressability mode
 - Maximum power saving mode
 - CA Parity mode

Figure 10 — tMOD Timing

Some of the mode register setting cases, function updating takes longer than tMOD. The MRS commands which do not apply tMOD timing to next valid command excluding DES is listed in note 2 of Figure 10. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

3.4.1 Programming the mode registers (cont'd)



NOTE 1 This timing diagram shows CA Parity Latency mode is "Disable" case.

NOTE 2 When an MRS command mentioned in this note affects RTT_NOM turn on timings, RTT_NOM turn off timings and RTT_NOM value, this means the MR register value changes. The ODT signal should set to be low for at least DODTLoft + 1 clock before their affecting MRS command is issued and remain low until tMOD expires. The following MR registers affects RTT_NOM turn on timings, RTT_NOM turn off timings and RTT_NOM value and it requires ODT to be low when an MRS command change the MR register value. If there are no changes the MR register value that corresponds to commands mentioned in this note, then the ODT signal is not required to be low.

- DLL control for precharge power down
- Additive latency and CAS read latency
- DLL enable and disable
- CAS write latency
- CA Parity mode
- Gear Down mode
- RTT_NOM

Figure 11 — ODT Status at MRS affecting ODT turn-on/off timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. For MRS command, If RTT_Nom function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring RTT_NOM is in an off state prior to MRS command affecting RTT_NOM turn-on and off timing. Refer to note2 of Figure 11 for this type of MRS. The ODT signal may be registered high after tMOD has expired. ODT signal is a don't care during MRS command if DRAM RTT_Nom function is disabled in the mode register prior to and after an MRS command.

3.5 Mode Register

MR0

Table 13 — Mode Register 0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13 ⁵ , A11:A9	WR and RTP ^{2, 3}	Write Recovery and Read to Precharge for auto precharge(see Table 14)
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A12, A6:A4,A2	CAS Latency ⁴	(see Table 15)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) Abbreviated BL8MRS 01 = BC4 or 8 (on the fly) Abbreviated BC4OTF or BL8OTF 10 = BC4 (Fixed) Abbreviated BC4MRS 11 = Reserved

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 WR (write recovery for autoprecharge)min in clock cycles is calculated following rounding algorithm defined in Section 13.5. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

NOTE 3 The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.

NOTE 4 The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency. Cas Latency controlled by A12 is optional for 4Gb device.

NOTE 5 A13 for WR and RTP setting is optional for 4Gb.

Table 14 — Write Recovery and Read to Precharge (cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

3.5 Mode Register (cont'd)

Table 15 — CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25
1	0	0	0	1	26
1	0	0	1	0	27 (only 3DS available)
1	0	0	1	1	28
1	0	1	0	0	reserved for 29
1	0	1	0	1	30
1	0	1	1	0	reserved for 31
1	0	1	1	1	32
1	1	0	0	0	reserved

3.5 Mode Register (cont'd)

MR1

Table 16 — Mode Register 1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ³
A17	RFU	0 = must be programmed to 0 during MRS
A13, A6, A5	Rx CTLE control	000 = Vendor Optimized Setting (default) 001 = vendor defined 010 = vendor defined 011 = vendor defined 100 = vendor defined 101 = vendor defined 110 = vendor defined 111 = vendor defined
A12	Qoff ¹	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see Table 17)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A4, A3	Additive Latency	00 = 0(AL disabled) 10 = CL-2 01 = CL-1 11 = Reserved
A2, A1	Output Driver Impedance Control	(see Table 18)
A0	DLL Enable	0 = Disable ² 1 = Enable

NOTE 1 Outputs disabled - DQs, DQS_ts, DQS_cs.

NOTE 2 States reversed to "0 as Disable" with respect to DDR4.

NOTE 3 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Table 17 — RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Table 18 — Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

3.5 Mode Register (cont'd)

MR2**Table 19 — Mode Register 2**

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Write CRC	0 = Disable 1 = Enable
A11, A10:A9	RTT_WR	(see Table 20)
A8, A2	RFU	0 = must be programmed to 0 during MRS
A7:A6	Low Power Auto Self Refresh (LP ASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A5:A3	CAS Write Latency (CWL)	(see Table 21)
A1:A0	RFU	0 = must be programmed to 0 during MRS

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Table 20 — RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT Off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Table 21 — CWL (CAS Write Latency)

A5	A4	A3	CWL	Operating Data Rate in MT/s for 1 tCK Write Preamble		Operating Data Rate in MT/s for 2 tCK Write Preamble ¹	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	2933 / 3200	2400	2666	2400
1	1	0	18		2666	2933 / 3200	2666
1	1	1	20		2933 / 3200		2933 / 3200

NOTE 1 The 2 tCK Write Preamble is valid for DDR4-2400/2666/2933/3200 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional delay is needed.

3.5 Mode Register (cont'd)

MR3

Table 22 — Mode Register 3

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A11	MPR Read Format	00 = Serial 10 = Staggered 01 = Parallel 11 = Reserved
A10:A9	Write CMD Latency when CRC and DM are enabled	(see Table 24)
A8:A6	Fine Granularity Refresh Mode	(see Table 23)
A5	Temperature sensor readout	0 : disabled 1: enabled
A4	Per DRAM Addressability	0 = Disable 1 = Enable
A3	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A2	MPR Operation	0 = Normal 1 = Dataflow from/to MPR
A1:A0	MPR page Selection	00 = Page0 10 = Page2 01 = Page1 11 = Page3 (see Table)

NOTE 1 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Table 23 — Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

Table 24 — MR3 A<10:9> Write Command Latency when CRC and DM are both enabled

A10	A9	CRC+DM Write Command Latency	Operating Data Rate
0	0	4nCK	1600
0	1	5nCK	1866,2133,2400,2666
1	0	6nCK	2933,3200
1	1	RFU	RFU

NOTE 1 Write Command latency when CRC and DM are both enabled:

NOTE 2 At less than or equal to 1600 then 4nCK; neither 5nCK nor 6nCK

NOTE 3 At greater than 1600 and less than or equal to 2666 then 5nCK; neither 4nCK nor 6nCK

NOTE 4 At greater than 2666 and less than or equal to 3200 then 6nCK; neither 4nCK nor 5nCK



3.5 Mode Register (cont'd)

Table 25 — MPR Data Format

MPR page0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/ Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page1 (CA Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read- only
	01 = MPR1	CAS_n/ A15	WE_n/ A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	ACT_n	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	RAS_n/ A16	
	11 = MPR3	CRC Error Status	CA Par- ity Error Status	CA Parity Latency ⁴			C[2]	C[1]	C[0]	
				MR5.A[2]	MR5.A[1]	MR5.A[0]				

NOTE 1 MPR used for C/A parity error log readout is enabled by setting A[2] in MR3

NOTE 2 For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.

NOTE 3 If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

NOTE 4 MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.

Table 25 — MPR Data Format (cont'd)

MPR page2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note	
BA1:BA0	00 = MPR0	hPPR	sPPR	RTT_WR	Temperature Sensor Status		CRC Write Enable	Rtt_WR		read-only	
		-	-	MR2	-	-	MR2	MR2			
		-	-	A11	-	-	A12	A10	A9		
	01= MPR1	Vref DQ Trng range	Vref DQ training Value						Gear-down Enable		
		MR6	MR6						MR3		
		A6	A5	A4	A3	A2	A1	A0	A3		
	10 = MPR2	CAS Latency					CAS Write Latency				
		MR0					MR2				
		A6	A5	A4	A2	A12	A5	A4	A3		
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver Impedance			
		MR1			MR5			MR1			
		A10	A9	A6	A8	A7	A6	A2	A1		

MR bit for Temperature Sensor Readout

MR3 bit A5=1: DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.

MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X refresh (> tREFI)
0	1	1X refresh rate(= tREFI)
1	0	2X refresh rate(1/2* tREFI)
1	1	rsvd

MPR page3 (Vendor use only)¹

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	Read-only
	01 = MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	11 = MPR3	don't care	don't care	don't care	don't care	MAC	MAC	MAC	MAC	

NOTE 1 MPR page3 is specifically assigned to DRAM. Actual encoding method is vendor specific.

3.5 Mode Register (cont'd)

MR4

Table 26 — Mode Register 4

Address	Operating Mode	Description	
BG1	RFU	0 = must be programmed to 0 during MRS	
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS	
A13	hPPR	0 = Disable	1 = Enable
A12	Write Preamble	0 = 1 nCK	1 = 2 nCK
A11	Read Preamble	0 = 1 nCK	1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable	1 = Enable
A9	Self Refresh Abort	0 = Disable	1 = Enable
A8:A6	CS to CMD/ADDR Latency Mode (cycles)	000 = Disable 001 = 3 010 = 4 011 = 5 (See Table 27)	100 = 6 101 = 8 110 = Reserved 111 = Reserved
A5	sPPR	0 = Disable	1 = Enable
A4	Internal Vref Monitor	0 = Disable	1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable	1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal	1 = Extended
A1	Maximum Power Down Mode	0 = Disable	1 = Enable
A0	MBIST PPR	0 = Disable	1 = Enable

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Table 27 — CS to CMD / ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

3.5 Mode Register (cont'd)

MR5**Table 28 — Mode Register 5**

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	CA parity Persistent Error	0 = Disable 1 = Enable
A8:A6	RTT_PARK	(see Table 29)
A5	ODT Input Buffer during Power Down mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A4	C/A Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2:A0	C/A Parity Latency Mode	(see Table 30)

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

Table 29 — RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Table 30 — C/A Parity Latency Mode

A2	A1	A0	PL	Speed Bin
0	0	0	Disable	
0	0	1	4	1600, 1866, 2133
0	1	0	5	2400, 2666
0	1	1	6	2933, 3200
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

NOTE 1 Parity latency must be programmed according to timing parameters by speed grade table



3.5 Mode Register (cont'd)

MR6

Table 31 — Mode Register 6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13, A9, A8	RFU	
A12:A10	tCCD_L	(see Table 32)
A7	VrefDQ Training Enable	0 = Disable (Normal operation Mode) 1 = Enable (Training Mode)
A6	VrefDQ Training Range	(see Table 33)
A5:A0	VrefDQ Training Value	(see Table 34)

NOTE 1 Reserved for Register control word setting . DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond.

Table 32 — tCCD_L & tDLLK

A12	A11	A10	tCCD_L.min (nCK) ¹	tDLLKmin (nCK) ¹	Note
0	0	0	4	597	Data rate ≤ 1333Mbps
0	0	1	5		1333Mbps < Data rate ≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps < Data rate ≤ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	2400Mbps < Data rate ≤ 2666Mbps (2666Mbps)
1	0	0	8		2666Mbps < Data rate ≤ 3200Mbps (2933/3200Mbps)
1	0	1	Reserved		
1	1	0			
1	1	1			

NOTE 1 tCCD_L/tDLLK should be programmed according to the value defined in AC parameter table per operating frequency

3.5 Mode Register (cont'd)

Table 33 — VrefDQ Training : Range

A6	VrefDQ Range
0	Range 1
1	Range 2

Table 34 — VrefDQ Training: Values

A5:A0	Range1	Range2	A5:A0	Range1	Range2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111	Reserved	Reserved

DRAM MR7 Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM. Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 35 — Command Truth Table

Function	Abbreviation	CKE		CS _n	ACT _n	RAS _n /A16	CAS _n /A15	WE _n /A14	BG0-BG1	BA0-BA1	C2-C0	A12/BC _n	A17, A13, A11	A10/AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V		
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

NOTE 1 All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When ACT_n = H; pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n respectively. When ACT_n = L; pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as address pins A16, A15, and A14 respectively

NOTE 2 RESET_n is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE 3 Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.

NOTE 4 "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

NOTE 5 Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE 6 The Power Down Mode does not perform any refresh operation.

NOTE 7 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE 8 Controller guarantees self refresh exit to be synchronous.

NOTE 9 VPP and VREF (VrefCA) must be maintained during Self Refresh operation.

NOTE 10 The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit

NOTE 11 Refer to the CKE Truth Table for more detail with CKE transition.

NOTE 12 During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

4.2 CKE Truth Table

Table 36 — CKE Truth Table

Current State ²	CKE		Command (N) ³ RAS_n, CAS_n, WE_n, CS_n	Action (N) ³	NOTE
	Previous Cycle ¹ (N-1)	Current Cycle ¹ (N)			
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See "Command Truth Table".					10

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N). ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.

NOTE 13 Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See "Self-Refresh Operation" on Section 4.27 and See "Power-Down Modes" on Section 4.28.

NOTE 14 The Power-Down does not perform any refresh operations.

NOTE 15 "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

NOTE 16 VPP and VREF (VrefCA) must be maintained during Self-Refresh operation.

NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

NOTE 18 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, etc.)

4.3 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 of Mode Register MR0. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 37. The burst length is defined by bits A0-A1 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC_n.

Table 37 — Burst Type and Burst Order

Burst Length	Read/Write	Starting Column Address (A2,A1,A0)	burst type = Sequential (decimal) A3=0	burst type = Interleaved (decimal) A3=1	NOTE
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1,2,3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1,2,3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1,2,3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1,2,3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1,2,3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1,2,3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1,2,3
	WRITE	0, V, V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1, V, V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1,2,4,5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V, V, V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

NOTE 1 In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC_n, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

NOTE 2 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

NOTE 3 Output driver for data and strobes are in high impedance.

NOTE 4 V : A valid logic level (0 or 1), but respective buffer input ignores level on input pins.

NOTE 5 X : Don't Care.

4.3.1 BL8 Burst order with CRC Enabled

DDR4 SDRAM supports fixed write burst ordering [A2:A1:A0=0:0:0] when write CRC is enabled in BL8 (fixed).

4.4 DLL-off Mode & DLL on/off Switching procedure

4.4.1 DLL on/off switching procedure

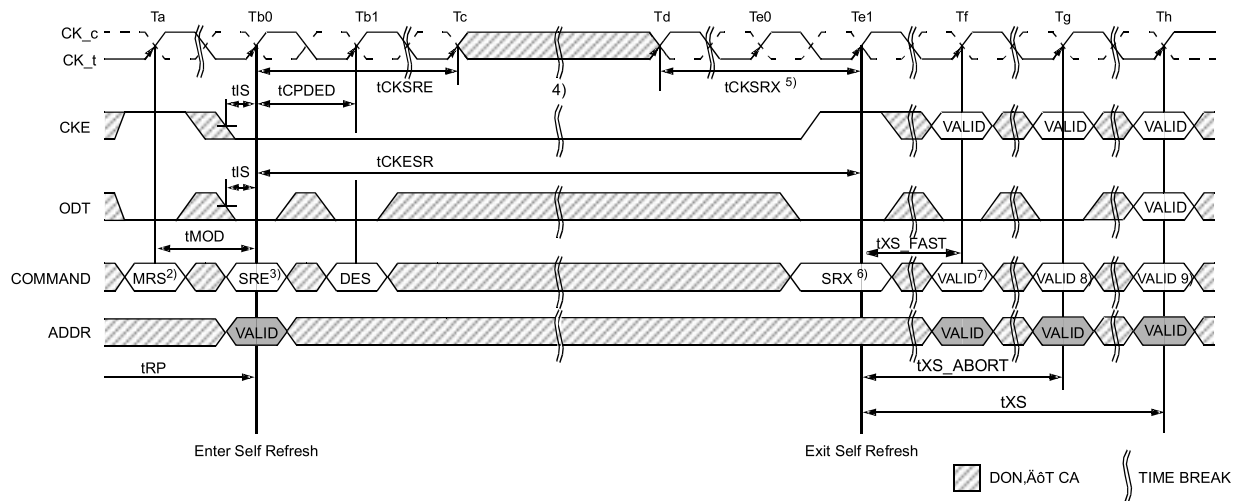
DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to "0"; this will disable the DLL for subsequent operations until A0 bit is set back to "1".

4.4.2 DLL "on" to DLL "off" Procedure

To switch from DLL "on" to DLL "off" requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT_NOM, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to "0" to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.
5. Change frequency, in guidance with "Input clock frequency change" on Section 4.6.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If RTT_NOM features were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don't Care.
8. Wait tXS_Fast or tXS_Abort or tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS_Fast).
 - tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8
 - tXS_Fast - ZQCL, ZQCS, MRS commands. For MRS command, only DRAM CL and WR/RTP register in MR0, CWL register in MR2 and gear-down mode in MR3 are allowed to be accessed provided DRAM is not in per DRAM addressability mode. Access to other DRAM mode registers must satisfy tXS timing.
 - tXS_Abort - If the MR4 bit A9 is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of tXS_abort. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.
9. Wait for tMOD, then DRAM is ready for next command.

2.4.2 DLL “on” to DLL “off” Procedure (cont’d)



- NOTE 1 Starting with Idle State, RTT in Stable
 NOTE 2 Disable DLL by setting MR1 Bit A0 to 0
 NOTE 3 Enter SR
 NOTE 4 Change Frequency
 NOTE 5 Clock must be stable tCKSRX
 NOTE 6 Exit SR
 NOTES 7.8.9 Update Mode registers allowed with DLL off parameters setting

Figure 12 — DLL Switch Sequence from DLL ON to DLL OFF

4.4.3 DLL “off” to DLL “on” Procedure

To switch from DLL “off” to DLL “on” (with required frequency change) during Self-Refresh:

- Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT_NOM) must be in high impedance state before Self-Refresh mode is entered.)
- Enter Self Refresh Mode, wait until tCKSRE satisfied.
- Change frequency, in guidance with "Input clock frequency change" on Section 4.6.
- Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
- Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If RTT_NOM were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don't care.
- Wait tXS or tXS_ABORT depending on Bit A9 in MR4, then set MR1 bit A0 to "1" to enable the DLL.
- Wait tMRD, then set MR0 bit A8 to "1" to start DLL Reset.
- Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
- Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.

4.4.3 DLL “off” to DLL “on” Procedure (cont’d)

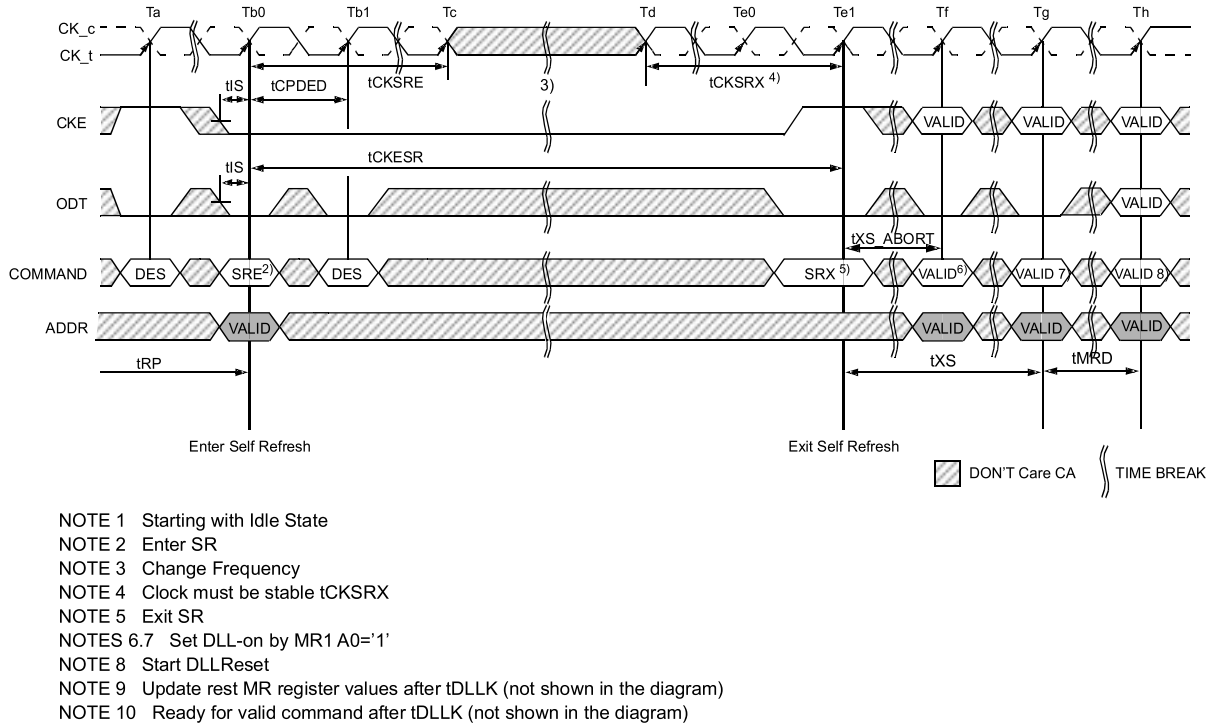


Figure 13 — DLL Switch Sequence from DLL OFF to DLL ON

4.5 DLL-off Mode

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to “Input clock frequency change” on Section 4.6.

The DLL-off Mode operations listed below are an optional feature for DDR4 SDRAM. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=10 and CWL=9. When DLL-off Mode is enabled, use of CA Parity Mode is not allowed.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command.

Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

tDQSCK(DLL_off) values are vendor specific.

The timing relations on DLL-off mode READ operation are shown in the following Timing Diagram (CL=10, BL=8, PL=0):

4.5 DLL-off Mode (cont'd)

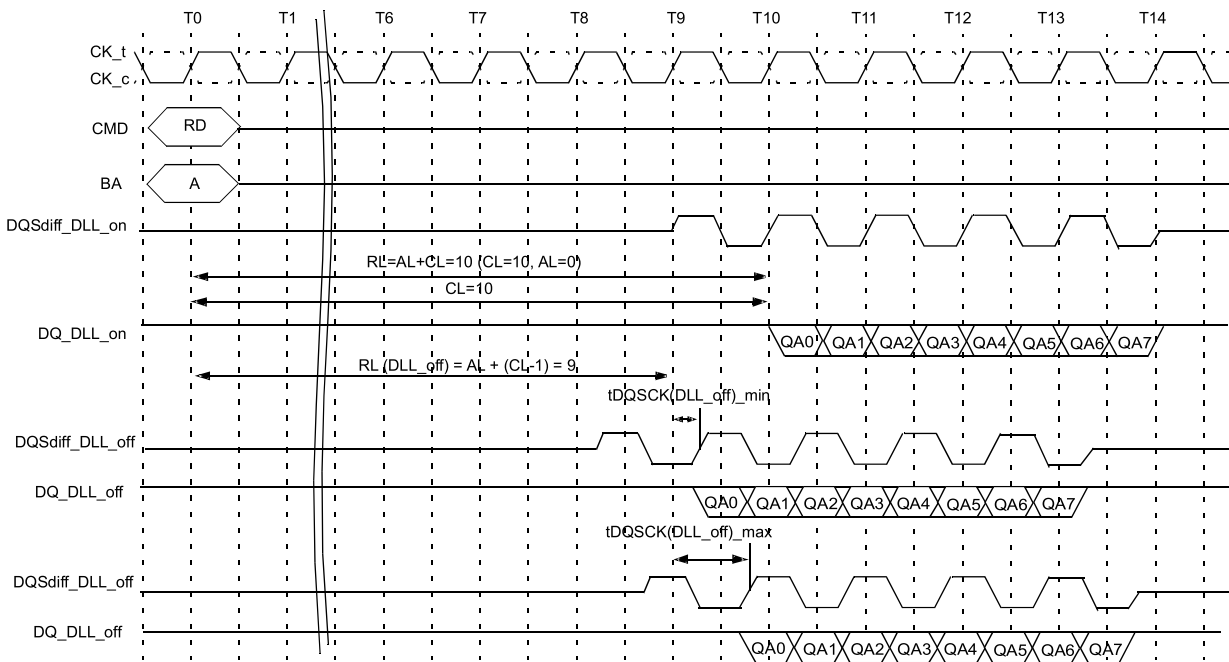


Figure 14 — READ operation at DLL-off mode

4.6 Input Clock Frequency Change

Once the DDR4 SDRAM is initialized, the DDR4 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under Self-Refresh mode. Outside Self-Refresh mode, it is illegal to change the clock frequency.

Once the DDR4 SDRAM has been successfully placed into Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in Section 4.27 “Self-Refresh Operation”.

For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, MR5, and MR6 may need to be issued to program appropriate CL, CWL, Gear-down mode, Read & Write Preamble, Command Address Latency (CAL Mode), Command Address Parity (CA Parity Mode), and tCCD_L/tDLLK value.

In particular, the Command Address Parity Latency (PL) must be disabled when the clock rate changes, i.e. while in Self Refresh Mode. For example, if changing the clock rate from DDR4-2133 to DDR4-2933 with CA Parity Mode enabled, MR5[2:0] must first change from PL = 4 to PL = disable prior to PL = 6. A correct procedure would be to (1) change PL = 4 to disable via MR5 [2:0], (2) enter Self Refresh Mode, (3) change clock rate from DDR4-2133 to DDR4-2933, (4) exit Self Refresh Mode, (5) Enable CA Parity Mode setting PL = 6 via MR5 [2:0].

If the MR settings that require additional clocks are updated after the clock rate has been increased, i.e., after exiting self refresh mode, the required MR settings must be updated prior to removing the DRAM from the IDLE state, unless the DRAM is RESET. If the DRAM leaves the idle state to enter self refresh mode or ZQ Calibration, the updating of the required MR settings may be deferred to after the next time the DRAM enters the IDLE state.

If MR6 is issued prior to Self Refresh Entry for new tDLLK value, then DLL will relock automatically at Self Refresh Exit. However, if MR6 is issued after Self Refresh Entry, then MR0 must be issued to reset the DLL. The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off- mode transition sequence, refer to Section 4.4, DLL on/off switching procedure

4.7 Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR4 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. This feature may not be required under some system conditions provided the host can maintain the tDQSS, tDSS and tDSH specifications.

The memory controller can use the 'write leveling' feature and feedback from the DDR4 SDRAM to adjust the DQS_t - DQS_c to CK_t - CK_c relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS_t - DQS_c to align the rising edge of DQS_t - DQS_c with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK_t - CK_c, sampled with the rising edge of DQS_t - DQS_c, through the DQ bus. The controller repeatedly delays DQS_t - DQS_c until a transition from 0 to 1 is detected. The DQS_t - DQS_c delay established through this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS_t - DQS_c signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 15.

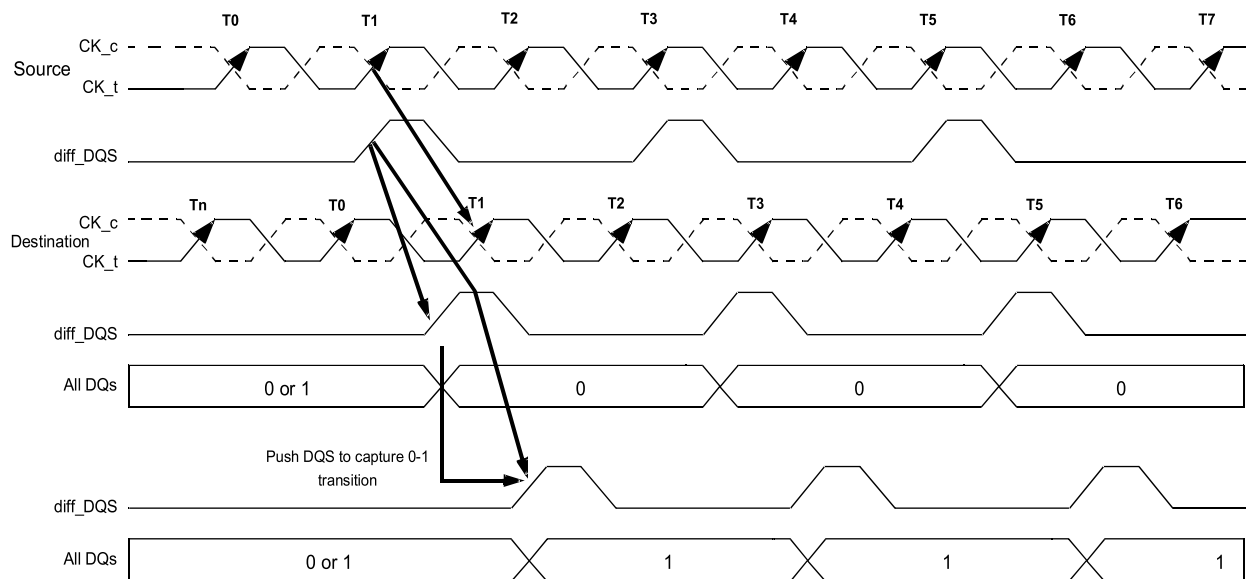


Figure 15 — Write Leveling Concept

DQS_t - DQS_c driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

4.7.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (Table 38). Note that in write leveling mode, only DQS_t/DQS_c terminations are activated and deactivated via ODT pin, unlike normal operation (Table 39).

Table 38 — MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

Table 39 — DRAM termination function in the leveling mode

ODT pin @DRAM if RTT_NOM/PARK Value is set via MRS	DQS_t/DQS_c termination	DQs termination
RTT_NOM with ODT High	On	Off
RTT_PARK with ODT LOW	On	Off

NOTE 1 In Write Leveling Mode with its output buffer disabled (MR1[bit A7] = 1 with MR1[bit A12] = 1) all RTT_NOM and RTT_PARK settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit A7] = 1 with MR1[bit A12] = 0) all RTT_NOM and RTT_PARK settings are allowed.

NOTE 2 Dynamic ODT function is not available in Write Leveling Mode. DRAM MR2 bits A[11:9] must be '000' prior to entering Write Leveling Mode.

4.7.2 Procedure Description

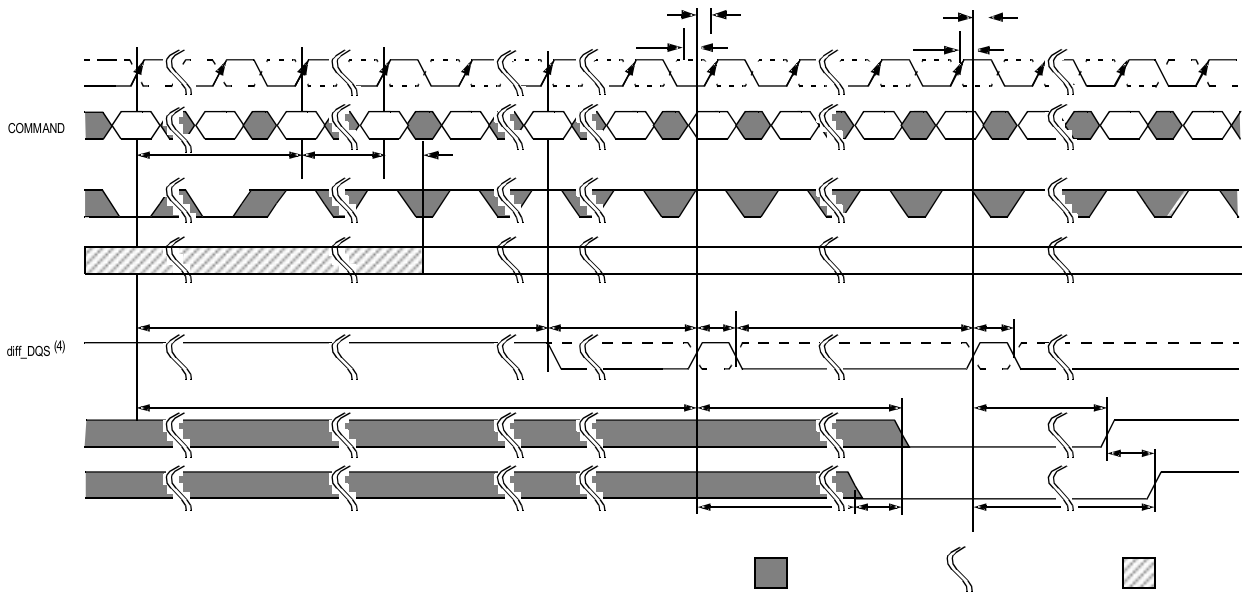
The Memory controller initiates Leveling mode of all DRAMs by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A8 ,A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS_t low and DQS_c high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS_t, DQS_c edge which is used by the DRAM to sample CK_t - CK_c driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK_t - CK_c status with rising edge of DQS_t - DQS_c and provides feedback on all the DQ bits asynchronously after tWLOE timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS_t/ DQS_c) needed for these DQs. Controller samples incoming DQs and decides to increment or decrement DQS_t - DQS_c delay setting and launches the next DQS_t/DQS_c pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS_t - DQS_c delay setting and write leveling is achieved for the device. Figure 16 describes the timing diagram and parameters for the overall Write Leveling procedure.

Table 40 — Write Leveling Mode

Parameter	Symbol	DDR4-1600,1866,2133,2400		DDR4-2666,3200		Units	NOTE
		Min	Max	Min	Max		
Write leveling output error	tWLOE	0	2	0	2	ns	



- NOTE 1 DDR4 SDRAM drives leveling feedback on all DQs
- NOTE 2 MRS : Load MR1 to enter write leveling mode
- NOTE 3 DES : Deselect
- NOTE 4 diff_DQS is the differential data strobe (DQS_t-DQS_c). Timing reference points are the zero crossings. DQS_t is shown with solid line, DQS_c is shown with dotted line
- NOTE 5 CK_t/CK_c : CK_t is shown with solid dark line, where as CK_c is drawn with dotted line.
- NOTE 6 DQS_t, DQS_c needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent
- NOTE 7 tMOD(Min) = max(24nCK, 15ns), WL = 9 (CWL = 9, AL = 0, PL = 0), DODTLon = WL -2 = 7
- NOTE 8 tWLDQSEN must be satisfied following equation when using ODT.
- tWLDQSEN > tMOD(Min) + ODTLon + tADC : at DLL = Enable
 - tWLDQSEN > tMOD(Min) + tAONAS : at DLL = Disable

Figure 16 — Timing details of Write leveling sequence [DQS_t - DQS_c is capturing CK_t - CK_c low at Ta and CK_t - CK_c high at Tb]

4.7.3 Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge (see $\sim T_0$), stop driving the strobe signals (see $\sim T_{c0}$). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MRS command (Te1).
2. Drive ODT pin low (tIS must be satisfied) and continue registering low. (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command may be registered. (MRS commands may be issued after tMRD (Td1)).

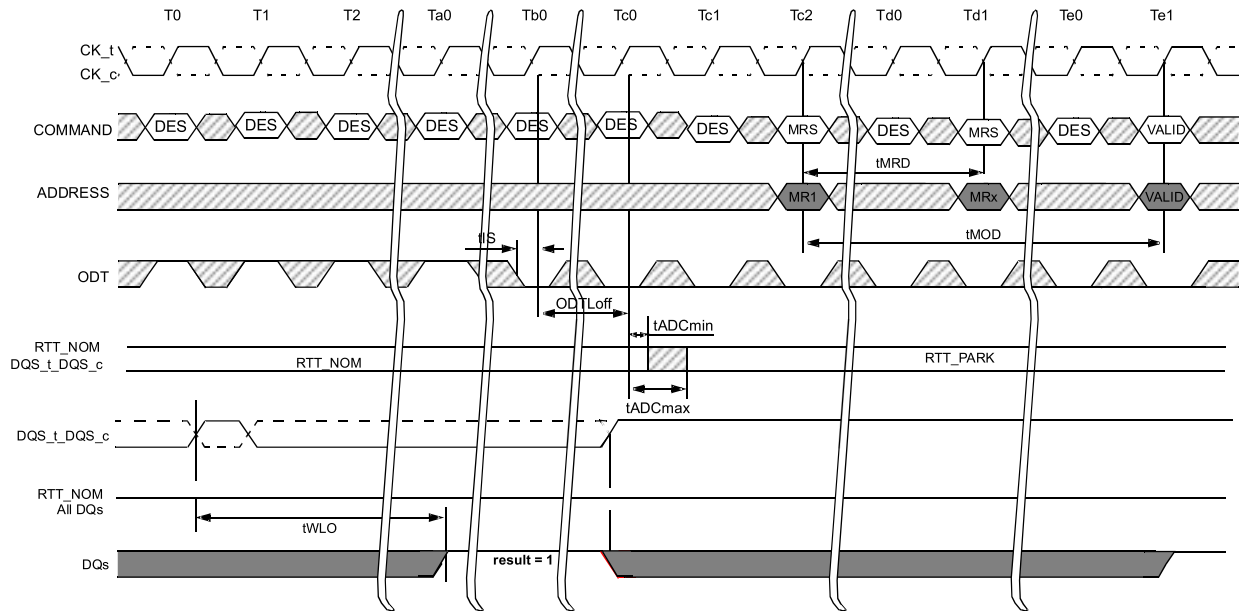


Figure 17 — Timing details of Write leveling exit

4.8 Temperature Controlled Refresh modes

This mode is, Temperature Controlled Refresh Mode (i.e., TCR), enabled and disabled by setting bit A3 in MR4. Two modes are supported that are selected by bit A2 setting in MR4. Temperature Controlled Refresh Mode operates the same for both Commercial Temperature, "CT", Devices and the optional Industrial Temperature, "IT", Devices.

4.8.1 Normal Temperature Mode (TCASE not exceed 85°C)

Commercial Temperature Device: 0°C ≤ TCASE ≤ 85°C

Industrial Temperature Device: -40°C ≤ TCASE ≤ 85°C

Once this mode, Normal Temperature Mode, is enabled by setting bit A3=1 and A2=0 in MR4, Refresh commands should be issued to DDR4 SDRAM with the Average periodic refresh interval (7.8us for 2Gb, 4Gb, 8Gb, and 16Gb device) which is tREFI of normal temperature range (0°C to 85°C or -40°C to 85°C). In this mode, the system guarantees that the DRAM temperature does not exceed 85°C.

Below 45°C, DDR4 SDRAM may adjust internal Average periodic refresh interval by skipping external refresh commands with proper gear ratio. Not more than three fourths of external refresh commands are skipped at any temperature in this mode. The internal Average periodic refresh interval adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

4.8.2 Extended Temperature Mode (TCASE not exceed 95°C)

Commercial Temperature Device: 0°C ≤ TCASE ≤ 95°C

Industrial Temperature Device: -40°C ≤ TCASE ≤ 95°C

Once this mode, Extended Temperature Mode, is enabled by setting bit A3=1 and A2=1 in MR4, Refresh commands should be issued to DDR4 SDRAM with the Average periodic refresh interval (3.9us for 2Gb, 4Gb, 8Gb, and 16Gb device) which is tREFI of extended temperature range (85°C to 95°C). In this mode, the system guarantees that the DRAM temperature does not exceed 95°C.

4.8.2 Extended Temperature Mode (TCASE not exceed 95°C) (cont'd)

In the extended normal temperature range (0°C to 95°C) or extended industrial temperature range (-40°C to 95°C), DDR4 SDRAM adjusts its internal Average periodic refresh interval to tREFI of the normal temperature range by skipping external refresh commands with proper gear ratio. Below 45°C, DDR4 SDRAM may further adjust internal Average periodic refresh interval. Not more than seven eighths of external commands are skipped at any temperature in this mode. The internal Average periodic refresh interval adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

4.9 Fine Granularity Refresh Mode

4.9.1 Mode Register and Command Truth Table

The Refresh cycle time (tRFC) and the average Refresh interval (tREFI) of DDR4 SDRAM can be programmed by MRS command. The appropriate setting in the mode register will set a single set of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device (fixed mode), or allow the dynamic selection of one of two sets of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device (on-the-fly mode). The on-the-fly mode must be enabled by MRS as shown in Table 41 before any on-the-fly-Refresh command can be issued.

Table 41 — MR3 definition for Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

There are two types of on-the-fly modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two on-the-fly modes is selected ('A8=1'), DDR4 SDRAM evaluates BG0 bit when a Refresh command is issued, and depending on the status of BG0, it dynamically switches its internal Refresh configuration between 1x and 2x (or 1x and 4x) modes, and executes the corresponding Refresh operation. The command truth table is as shown in Table 42.

Table 42 — Refresh command truth table

Function	CS _n	ACT _n	RAS _n /A16	CAS _n /A15	WE _n /A14	BG1	BG0	BA0-1	A10/ AP	A0-9, A11-12, A16-20	MR3 Setting
Refresh (Fixed rate)	L	H	L	L	H	V	V	V	V	V	A8 = '0'
Refresh (on-the-fly 1x)	L	H	L	L	H	V	L	V	V	V	A8 = '1'
Refresh (on-the-fly 2x)	L	H	L	L	H	V	H	V	V	V	A8:A7:A6='101'
Refresh (on-the-fly 4x)											A8:A7:A6='110'

4.9.2 tREFI and tRFC parameters

The default Refresh rate mode is fixed 1x mode where Refresh commands should be issued with the normal rate, i.e., tREFI1 = tREFI(base) (for Tcase ≤ 85°C), and the duration of each refresh command is the normal refresh cycle time (tRFC1). In 2x mode (either fixed 2x or on-the-fly 2x mode), Refresh commands should be issued to the DRAM at the double frequency (tREFI2 = tREFI(base)/2) of the normal Refresh rate. In 4x mode, Refresh command rate should be quadrupled (tREFI4 = tREFI(base)/4). Per each mode and command type, tRFC parameter has different values as defined in Table 43.

The refresh command that should be issued at the normal refresh rate and has the normal refresh cycle duration may be referred to as a REF1x command. The refresh command that should be issued at the double frequency (tREFI2 = tREFI(base)/2) may be referred to as a REF2x command. Finally, the refresh command that should be issued at the quadruple rate (tREFI4 = tREFI(base)/4) may be referred to as a REF4x command.

4.9.2 tREFI and tRFC parameters (cont'd)

In the Fixed 1x Refresh rate mode, only REF1x commands are permitted. In the Fixed 2x Refresh rate mode, only REF2x commands are permitted. In the Fixed 4x Refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x Refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the on-the-fly 1x/4x Refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

Table 43 — tREFI and tRFC parameters

Refresh Mode	Parameter	2Gb	4Gb	8Gb	16Gb	Unit
	tREFI(base)	7.8	7.8	7.8	7.8	us
1X mode	tREFI1	0°C ≤ TCASE ≤ 85°C	tREFI(base)	tREFI(base)	tREFI(base)	us
		85°C < TCASE ≤ 95°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	us
	tRFC1(min)	160	260	350	550(default) 450 (optional-1) 350 (optional-2)	ns
2X mode	tREFI2	0°C ≤ TCASE ≤ 85°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	us
		85°C < TCASE ≤ 95°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	us
	tRFC2(min)	110	160	260	350(default) 350 (optional-1) 260 (optional-2)	ns
4X mode	tREFI4	0°C ≤ TCASE ≤ 85°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	us
		85°C < TCASE ≤ 95°C	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	us
	tRFC4(min)	90	110	160	260(default) 260 (optional-1) 160 (optional-2)	ns

Note 1 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. tRFC2 and tRFC4 needs to be set corresponding to each setting's value (default / optional-1 / optional-2) accordingly. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.

4.9.3 Changing Refresh Rate

If Refresh rate is changed by either MRS or on the fly, new tREFI and tRFC parameters would be applied from the moment of the rate change. As shown in Figure 18, when REF1x command is issued to the DRAM, then tREF1 and tRFC1 are applied from the time that the command was issued. And then, when REF2x command is issued, then tREF2 and tRFC2 should be satisfied.

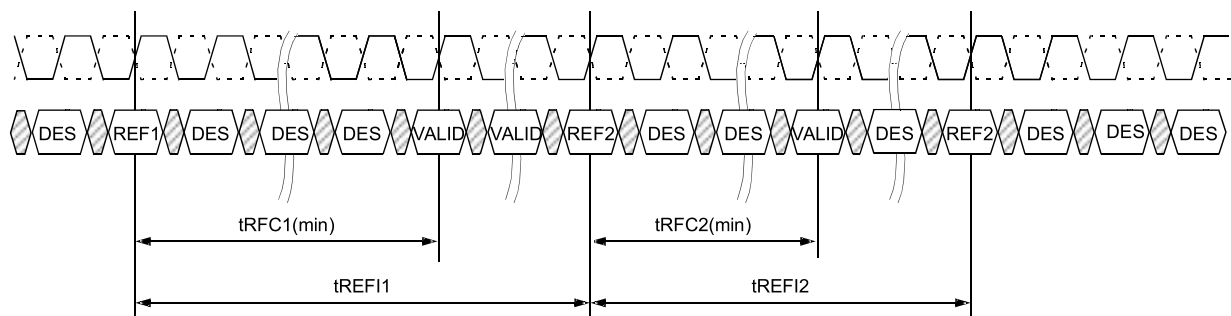


Figure 18 — On-the-fly Refresh Command Timing

The following conditions must be satisfied before the Refresh rate can be changed. Otherwise, data retention of DDR4 SDRAM cannot be guaranteed.

1. In the fixed 2x Refresh rate mode or the on-the-fly 1x/2x Refresh mode, an even number of REF2x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate mode with an MRS command before the Refresh rate can be changed by another MRS command.
2. In the on-the-fly 1x/2x Refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.

4.9.3 Changing Refresh Rate (cont'd)

3. In the fixed 4x Refresh rate mode or the on-the-fly 1x/4x Refresh mode, a multiple of-four number of REF4x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate with an MRS command before the Refresh rate can be changed by another MRS command.
4. In the on-the-fly 1x/4x Refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x Refresh rate mode. Switching between fixed and on-the-fly modes keeping the same rate is not regarded as a Refresh rate change.

4.9.4 Usage with Temperature Controlled Refresh mode

If the Temperature Controlled Refresh mode is enabled, then only the normal mode (Fixed 1x mode; A8:A7:A6='000') is allowed. If any other Refresh mode than the normal mode is selected, then the temperature controlled Refresh mode must be disabled.

4.9.5 Self Refresh entry and exit

DDR4 SDRAM can enter Self Refresh mode anytime in 1x, 2x and 4x mode without any restriction on the number of Refresh commands that has been issued during the mode before the Self Refresh entry. However, upon Self Refresh exit, extra Refresh command(s) may be required depending on the condition of the Self Refresh entry. The conditions and requirements for the extra Refresh command(s) are defined as follows

1. There are no special restrictions on the fixed 1x Refresh rate mode.
2. In the fixed 2x Refresh rate mode or the enable-on-the-fly 1x/2x Refresh rate mode, it is recommended that there should be an even number of REF2x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI).
3. In the fixed 4x Refresh rate mode or the enable-on-the-fly 1x/4x Refresh rate mode, it is recommended that there should be a multiple-of-four number of REF4x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or four extra REF4x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI).

4.10 Multi Purpose Register

4.10.1 DQ Training with MPR

The DDR4 DRAM contains four 8bit programmable MPR registers used for DQ bit pattern storage. These registers once programmed are activated with MRS read commands to drive the MPR bits on to the DQ bus during link training.

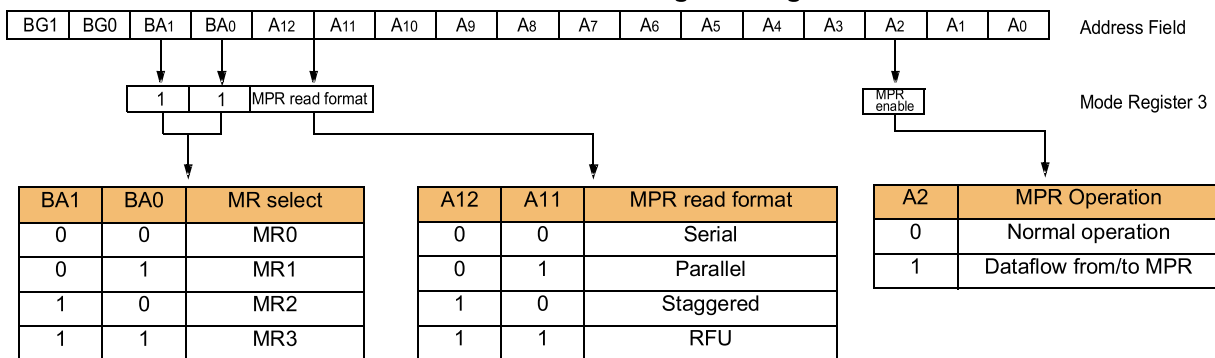
And DDR4 SDRAM only supports following command, MRS, RD, RDA WR, WRA, DES, REF and Reset during MPR enable Mode: MR3 [A2 = 1].

Note that in MPR mode RDA/WRA has the same functionality as a READ/WRITE command which means the auto precharge part of RDA/WRA is ignored. Power-Down mode and Self-Refresh command also is not allowed during MPR enable Mode. No other command can be issued within tRFC after REF command and 1x Refresh is only allowed when MPR mode is Enable. During MPR operations, MPR read or write sequence must be complete prior to a refresh command.

4.10.2 MR3 definition

Mode register MR3 controls the Multi-Purpose Registers (MPR) used for training. MR3 is written by asserting CS_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 low, ACT_n, BA0 and BA1 high and BG1¹ and BG0 low while controlling the states of the address pins according to Table 44.

Table 44 — MR3 Programming



Read or Write with MPR LOCATION :

A1	A0	MPR Page Selection
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Default value for MPR0 @ Page0= 01010101
 Default value for MPR1 @ Page0 = 00110011
 Default value for MPR2 @ Page0 = 00001111
 Default value for MPR3 @ Page0 = 00000000

NOTE 1 x4/x8 only