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DDR5 SDRAM

From JEDEC Board Ballot JCB-24-03, formulated under the cognizance of the JC-42.3 Subcommittee on Dynamic RAMs (DDR_x), item number 1848.99O.

1 Scope

This standard defines the DDR5 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 8 Gb through 32 Gb for x4, x8, and x16 DDR5 SDRAM devices. This standard was created based on the DDR4 standards (JESD79-4) and some aspects of the DDR, DDR2, DDR3, and LPDDR4 standards (JESD79, JESD79-2, JESD79-3, and JESD209-4).

1.1 JM7 Verbal Forms and Terms

JEDEC publication JM7 provides examples and directives for the use of verbal forms (e.g., 'shall' compared with 'should' and 'may' compared with 'can').

This specification adheres to the verbal forms defined in JM7.01 July 2010 revision.

2 DDR5 SDRAM Package, Pinout Description, and Addressing

2.1 DDR5 SDRAM Row for X4, X8

The DDR5 SDRAM x4/x8 component shall have 13 electrical rows of balls. Electrical is defined as rows that contain signal ball or power/ground balls. There may be additional rows of inactive balls for mechanical support.

2.2 DDR5 SDRAM Ball Pitch

The DDR5 SDRAM component shall use a ball pitch of 0.8mm by 0.8mm.
The number of fully depopulated columns is 3.

2.3 DDR5 SDRAM Columns for X4, X8

The DDR5 SDRAM x4/x8 component shall have 6 electrical columns of balls in 2 sets of 3 columns. There shall be columns between the electrical columns where there are no balls populated. The number of these is 3. Electrical is defined as columns that contain signal ball or power/ground balls. There may be additional columns of inactive balls for mechanical support.

2.4 DDR5 SDRAM x4/8 Ballout Using MO-210

Table 1 — DDR5 SDRAM x4/8 Ballout Using MO-210

AN	1	2	3	4	5	6	7	8	9	10	11	
AL		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP					ZQ ⁷	VSS	LBDQS	DNU
B		VDD	VDDQ	DQ2					DQ3	VDDQ	VDD	
C		VSS	DQ0	DQS _t					DM _n ⁴ , TDQS _t ²	DQ1	VSS	
D		VDDQ	VSS	DQS _c					TDQS _c ³	VSS	VDDQ	
E		VDD	DQ4 ¹	DQ6 ¹					DQ7 ¹	DQ5 ¹	VDD	
F		VSS	VDDQ	VSS					VSS	VDDQ	VSS	
G		CA_ODT	MIR	VDD					CK _t	VDDQ	TEN ⁵ (CS1 _n ⁵)	
H		ALERT _n	VSS	CS _n					CK _c	VSS	VDD	
J		VDDQ	CA4	CA0					CA1	CA5	VDDQ	
K		VDD	CA6	CA2					CA3	CA7	VDD	
L		VDDQ	VSS	CA8					CA9	VSS	VDDQ	
M		CAI, ZQ1 ⁸	CA10	CA12					CA13	CA11	RESET _n	
N	DNU	VDD	VSS	VDD					VPP	VSS	VDD	DNU

NOTE 1

NOTE 2

NOTE 3

NOTE 4

NOTE 5

NOTE 6

NOTE 7

NOTE 8

DQ4-DQ7 are higher order DQ pins and are not connected for the x4 configuration.
TDQS_t is not valid for the x4 configuration
TDQS_c is not available for the x4 configuration
DM_n not valid for the x4 configuration
For single die package (SDP) or 3DS, this pin is TEN; CS1_n is not connected, and is used as Test Mode Enable. For dual die package (DDP), this pin is CS1_n; and TEN is disconnected, and is used as CS1_n.
The electrical parameters for DDP package are TBD and will be covered from future ballots.
For dual die package (DDP), ZQ is connected to bottom die (Rank 0).
For single die package (SDP) or 3DS, CAI is used to indicate Command Address Inversion (ZQ1 is not applicable). However, for dual die package (DDP), CAI die pads are grounded inside the package, and ZQ1 pin is connected to the top die ZQ pad (Rank 1).

MO-210-AL (x4/x8)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	+	○	○
B	○	○	○	+	+	+	+	○	○
C	○	○	○	+	+	+	+	○	○
D	○	○	○	+	+	+	+	○	○
E	○	○	○	+	+	+	+	○	○
F	○	○	○	+	+	+	+	○	○
G	○	○	○	+	+	+	+	○	○
H	○	○	○	+	+	+	+	○	○
J	○	○	○	+	+	+	+	○	○
K	○	○	○	+	+	+	+	○	○
L	○	○	○	+	+	+	+	○	○
M	○	○	○	+	+	+	+	○	○
N	○	○	○	+	+	+	+	○	○

MO-210-AN (x4/x8)
with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	○	○	+	+	+	+	○	○	○
B	+	○	○	○	+	+	+	+	○	○	+
C	+	○	○	○	+	+	+	+	○	○	+
D	+	○	○	○	+	+	+	+	○	○	+
E	+	○	○	○	+	+	+	+	○	○	+
F	+	○	○	○	+	+	+	+	○	○	+
G	+	○	○	○	+	+	+	+	○	○	+
H	+	○	○	○	+	+	+	+	○	○	+
J	+	○	○	○	+	+	+	+	○	○	+
K	+	○	○	○	+	+	+	+	○	○	+
L	+	○	○	○	+	+	+	+	○	○	+
M	+	○	○	○	+	+	+	+	○	○	+
N	○	○	○	○	+	+	+	+	○	○	○

○ Populated ball
 + Ball not populated

NOTE(s):

- Additional columns and rows of inactive balls in MO-210 Terminal Pattern AN (x4/x8) with support balls are for mechanical support only, and should not be tied to either electrically high or low.
- Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.

Figure 1 — DDR5 Ball Assignments for the x4/8 Component

2.5 DDR5 SDRAM x16 Ballout using MO-210

Table 2 — DDR5 SDRAM x16 Ballout using MO-210

AU	1	2	3	4	5	6	7	8	9	10	11	
AT		1	2	3	4	5	6	7	8	9		
A	DNU	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	DNU	A
B		VDD	VDDQ	DQU2				DQU3	VDDQ	VDD		B
C		VSS	DQU0	DQSU_t				DMU_n	DQU1	VSS		C
D		VDDQ	VSS	DQSU_c				RFU	VSS	VDDQ		D
E		VDD	DQU4	DQU6				DQU7	DQU5	VDD		E
F		VDD	VDDQ	DQL2				DQL3	VDDQ	VDD		F
G		VSS	DQL0	DQSL_t				DML_n	DQL1	VSS		G
H		VDDQ	VSS	DQSL_c				RFU	VSS	VDDQ		H
J		VDD	DQL4	DQL6				DQL7	DQL5	VDD		J
K		VSS	VDDQ	VSS				VSS	VDDQ	VSS		K
L		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN		L
M		ALERT_n	VSS	CS_n				CK_c	VSS	VDD		M
N		VDDQ	CA4	CA0				CA1	CA5	VDDQ		N
P		VDD	CA6	CA2				CA3	CA7	VDD		P
R		VDDQ	VSS	CA8				CA9	VSS	VDDQ		R
T		CAI	CA10	CA12				CA13	CA11	RESET_n		T
U	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU	U

MO-210-AT (x16)

	1	2	3	4	5	6	7	8	9
A	○	○	○	+	+	+	○	○	○
B	○	○	○	+	+	+	○	○	○
C	○	○	○	+	+	+	○	○	○
D	○	○	○	+	+	+	○	○	○
E	○	○	○	+	+	+	○	○	○
F	○	○	○	+	+	+	○	○	○
G	○	○	○	+	+	+	○	○	○
H	○	○	○	+	+	+	○	○	○
J	○	○	○	+	+	+	○	○	○
K	○	○	○	+	+	+	○	○	○
L	○	○	○	+	+	+	○	○	○
M	○	○	○	+	+	+	○	○	○
N	○	○	○	+	+	+	○	○	○
P	○	○	○	+	+	+	○	○	○
R	○	○	○	+	+	+	○	○	○
T	○	○	○	+	+	+	○	○	○
U	○	○	○	+	+	+	○	○	○

MO-210-AU (x16)
with support balls

	1	2	3	4	5	6	7	8	9	10	11
A	○	○	○	○	+	+	+	○	○	○	○
B	+	○	○	○	+	+	+	○	○	○	+
C	+	○	○	○	+	+	+	○	○	○	+
D	+	○	○	○	+	+	+	○	○	○	+
E	+	○	○	○	+	+	+	○	○	○	+
F	+	○	○	○	+	+	+	○	○	○	+
G	+	○	○	○	+	+	+	○	○	○	+
H	+	○	○	○	+	+	+	○	○	○	+
J	+	○	○	○	+	+	+	○	○	○	+
K	+	○	○	○	+	+	+	○	○	○	+
L	+	○	○	○	+	+	+	○	○	○	+
M	+	○	○	○	+	+	+	○	○	○	+
N	+	○	○	○	+	+	+	○	○	○	+
P	+	○	○	○	+	+	+	○	○	○	+
R	+	○	○	○	+	+	+	○	○	○	+
T	+	○	○	○	+	+	+	○	○	○	+
U	○	○	○	○	+	+	+	○	○	○	○

○ Populated ball
+ Ball not populated

NOTE(s):

- Additional columns and rows of inactive balls in MO-210 Terminal Pattern AU (x16) with support balls are for mechanical support only, and should not be tied to either electrically high or low.
- Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.

Figure 2 — DDR5 Ball Assignments for the x16 Component

2.6 Pinout Description**Table 3 — Pinout Description**

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CS_n, (CS1_)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DM_n, DMU_n, DML_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
CA [13:0]	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are Multi-Cycle, the pins may not be interchanged between devices on the same bus.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DDQ} .
DQ	Input / Output	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via MR5:OP[4]=1, the DRAM shall enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via MR5:OP[4]=0, DM_n/TDQS_t shall provide the data mask function depending on MR5:OP[5]; TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via MR5:OP[4]=0.
ALERT_n	Input/Output	Alert: If a CRC error is detected, ALERT_n goes LOW for a time interval and goes back HIGH. During Connectivity Test mode, this pin works as an input. Optional use of this signal is dependent on the system. If the ALERT_n is not used, the ALERT_n pin must be pulled to VDDQ on the board.
TEN	Input	Connectivity Test Mode Enable: Required on x4, x8 & x16 devices. HIGH in this pin shall enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of V _{DDQ} . Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
MIR	Input	Mirror: Used to inform SDRAM device that it is being configured for Mirrored mode vs. Standard mode. With the MIR pin connected (strapped) to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSS if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1) CA4 with CA5 (not CA3). Note that the CA[13] function is only relevant for certain densities (including stacking) of DRAM component. In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected (Strapped) to VDDQ. No active signaling requirements defined.
CAI	Input	Command & Address Inversion: With the CAI pin connected (strapped) to VDDQ, DRAM internally inverts the logic level present on all the CA signals. Normally the CAI pin must be connected to VSS if no CA inversion is required. No active signaling requirements defined.
CA_ODT	Input	ODT for Command and Address. Apply Group A settings if the pin is connected (strapped) to VSS and apply Group B settings if the pin is connected (strapped) to V _{DDQ} . No active signalling requirements defined.
LBDQ	Output	Loopback Data Output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].

Table 3 — Pinout Description (cont'd)

Symbol	Type	Function
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.1 V
VDD	Supply	Power Supply: 1.1 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 1.8 V
ZQ, (ZQ1)	Reference	Reference Pin for ZQ calibration. This ball is tied to an external 240 ohm resistor(RZQ), which is tied to V _{SS} .

2.7 DDR5 SDRAM Addressing

Table 4 — 8 Gb Addressing Table

Configuration		2 Gb x4	1 Gb x8	512 Mb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0	BA0	BA0
	# BG / # Banks per BG / # Banks	8 / 2 / 16	8 / 2 / 16	4 / 2 / 8
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

Table 5 — 16 Gb Addressing Table

Configuration		4 Gb x4	2 Gb x8	1 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

Table 6 — 24 Gb Addressing Table

Configuration		6 Gb x4	3 Gb x8	1.5 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R16	R0~R16	R0~R16
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H
NOTE 1	For non-binary memory densities, a quarter of the row address space is invalid. When the MSB address bit is "HIGH", the MSB-1 address bit shall be "LOW".			

Table 7 — 32 Gb Addressing Table

Configuration		8 Gb x4	4 Gb x8	2 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R16	R0~R16	R0~R16
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

2.7 DDR5 SDRAM Addressing (cont'd)

Table 8 — 64 Gb Addressing Table

Configuration		16 Gb x4	8 Gb x8	4 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R17	R0~R17	R0~R17
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~2 / 8H	CID0~2 / 8H	CID0~2 / 8H

3.2 Basic Functionality

The DDR5 SDRAM is a high-speed dynamic random-access memory. To ease transition from DDR4 to DDR5, the introductory density (8 Gb) shall be internally configured as 16-bank, 8 bank group with 2 banks for each bank group for x4/x8 and 8-bank, 4 bank group with 2 banks for each bankgroup for x16 DRAM. When the industry transitions to higher densities (≥ 16 Gb), it doubles the bank resources and internally be configured as 32-bank, 8 bank group with 4 banks for each bank group for x4/x8 and 16-bank, 4-bank group with 4 banks for each bankgroup for x16 DRAM.

The DDR5 SDRAM uses a 16n prefetch architecture to achieve high-speed operation. The 16n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR5 SDRAM consists of a single 16n-bit wide, eight clock data transfer at the internal DRAM core and sixteen corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR5 SDRAM are burst oriented, start at a selected location, and continue for a burst length of sixteen or a 'chopped' burst of eight in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered with the ACTIVATE Command are used to select the bank and row to be activated (i.e. in a 16Gb part, BG0-BG2 in a x4/8 and BG0-BG1 in x16 select the bankgroup; BA0-BA1 select the bank; R0-R17 select the row; refer to "DDR5 SDRAM Addressing" for specific requirements). The address bits registered with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (CA10=L), and select BC8 on-the-fly (OTF), fixed BL16, fixed BL32 (optional), or BL32 OTF (optional) mode if enabled in the mode register.

Prior to normal operation, the DDR5 SDRAM must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

3.3 RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings need to be defined.

Table 9 — MR Default Settings

Item	Mode Register	Default Setting	Description
Burst Length	MR0 OP[1:0]	00 _B	BL16
Read Latency	MR0 OP[6:2]	00010 _B	RL(CL) = 26 @3200
Write Latency	n/a	WL=RL-2 (CWL=CL-2)	Fixed based on RL (CL)
Write Recovery (tWR)	MR6 OP[3:0]	0000 _B	WR = 48nCK @3200 or 30ns
Read to Precharge Delay (tRTP)	MR6 OP[7:4]	0000 _B	tRTP=12nCK @3200 or 7.5ns
VrefDQ Value	MR10	0010 1101 _B	VREF(DQ) Range: 75% of V _{DDQ}
VrefCA Value	MR11	0010 1101 _B	VREF(CA) Range: 75% of V _{DDQ}
VrefCS Value	MR12	0010 1101 _B	VREF(CS) Range: 75% of V _{DDQ}
ECS Error Threshold Count (ETC)	MR15	011 _B	256
Post Package Repair	MR23 OP[1:0]	00 _B	hPPR and sPPR Disabled
CK ODT	MR32 OP[2:0]	CK ODT is based on strap value	Group A= RTT_OFF=000 _B Group B= 40 Ohms=111 _B
CS ODT	MR32 OP[5:3]	CS ODT is based on strap value	Group A= RTT_OFF=000 _B Group B= 40 Ohms=111 _B
CA ODT	MR33 OP[2:0]	CA ODT is based on strap value	Group A= RTT_OFF=000 _B Group B= 80 Ohms=100 _B
DQS_RTT_PARK	MR33 OP[5:3]	000 _B	RTT OFF
RTT_PARK	MR34 OP[2:0]	000 _B	RTT OFF
RTT_WR	MR34 OP[5:3]	001 _B	240 Ohm
RTT_NOM_WR	MR35 OP[2:0]	011 _B	80 Ohm
RTT_NOM_RD	MR35 OP[5:3]	011 _B	80 Ohm
RTT Loopback	MR36 OP[2:0]	000 _B	RTT OFF
RFM RAAIMT	MR58 OP[4:1]	vendor specific	vendor specific
RFM RAAMMT	MR58 OP[7:5]	vendor specific	vendor specific
RFM RAA Counter	MR59 OP[7:6]	vendor specific	vendor specific

3.3.1 Power-up Initialization Sequence

The following sequence shall be used to power up the DDR5 device. Unless specified otherwise, these steps are mandatory.

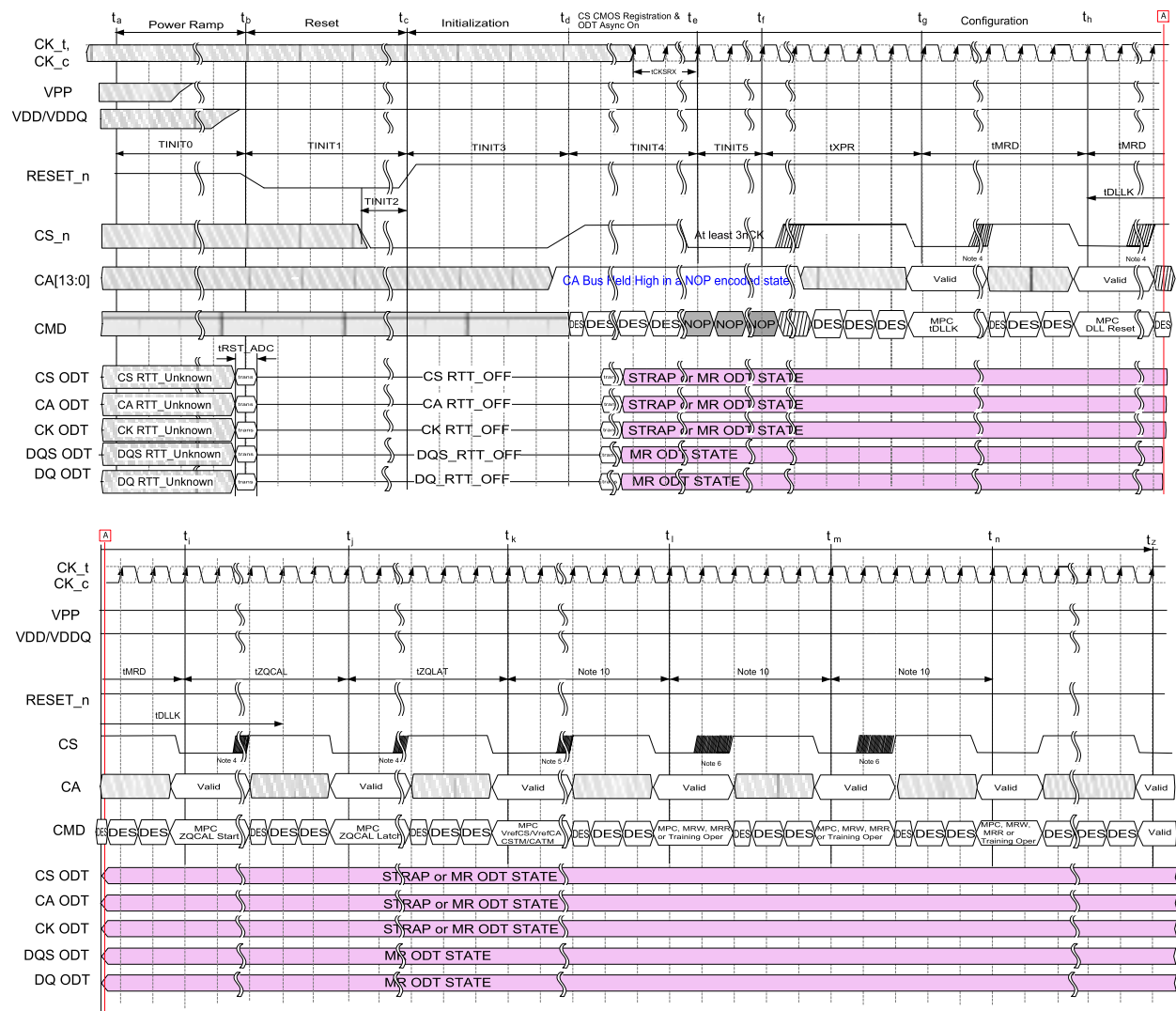
- While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times V_{DDQ}$) and all other inputs may be undefined. The device outputs remain disabled while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 10 VPP shall ramp at the same time or earlier than VDD.

Table 10 — Voltage Ramp Conditions

After	Application Conditions
Ta is reached	VPP shall be greater than VDD
NOTE 1 Ta is the point when any power supply first reaches 300 mV NOTE 2 Voltage ramp conditions in the table above apply between (Ta) and Power-off (controlled or uncontrolled). NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges. NOTE 4 Power ramp duration (Tb-Ta) shall not exceed tINIT0.	

- Following the completion of the voltage ramp (Tb), RESET_n shall be maintained LOW. DQ, DQS_t, DQS_c, voltage levels shall be between VSS and VDDQ to avoid latch-up. CS_n, CK_t, CK_c and CA input levels shall be between VSS and VDDQ to avoid latch-up.
- Beginning at Tb, RESET_n shall be maintained LOW for a minimum of tINIT1 (Tb to Tc), after which RESET_n may be de-asserted to HIGH (Tc). At least tINIT2 before RESET_n de-assertion, CS_n is required to be set LOW. All other input signals are "Don't Care". The DRAM shall support the ability for RESET_n to be held indefinitely.

3.3.1 Power-up Initialization Sequence (cont'd)



NOTES:

- From time point (T_a) until (T_b), RTT_OFF may not be guaranteed due to the limitation for the DRAM to control the RTT status during the Power Ramp period.
- From time point (T_d) until (T_e), the command/address (CA) bus shall be held high in a NOP encoded state.
- From time point (T_e) until (T_f), NOP commands shall be applied on the command/address (CA) bus.
- From time point (T_f) until (T_k), DES commands must be applied between legal commands (MRR, MRW, MPC, VREFCS & VREFCA). MRR and MRW command, while legal, may not execute properly until CS and CA training routines are completed.
- Prior to ZQcal completion at (T_k), MPC commands shall be Multi-Cycle as described in the MPC command Timings section.
- From time point (T_k) until (T_l) all MPC, VREFCS and VREFCA commands prior to CS and CA training successfully completing, shall be Multi-Cycle (MR2:OP[4]=0) as described in the MPC, VREFCS, and VREFCA timing sections.
- At time point (T_l), with successful completion of CS and CA training, an MRW command setting MR2:OP[4]=1 is recommended and allows for MPC, VREFCS, VREFCA commands to be single-cycle, improving training duration.
- From time point (T_k) until (T_z), DES commands shall be applied between legal commands (MRR, MRW, MPC, VREFCS & VREFCA).
- Starting at T_l, MRW Commands shall be issued to all Mode Registers that require defined settings.
- Default ODT tolerances are wider prior to ZQ calibration.
- All MPC/MRW/MRR to MPC/MRW/MRR commands shall meet the timing restrictions required.
- Between (T_k to T_z), the SRX/NOP Clock-Sync feature can be enabled through an MRW command by programming MR13:OP[5]=1. When it is enabled, after CSTM/CATM prior to DCA training, host shall issue an SRE/SRX pair to ensure that the Clock-Sync is in effect during DCA training. It is also applied for CS Geardown Initialization sequence (for example, after Power-Up Initialization, CSTM, MPC (CS Geardown enable), Sync Pulse, CATM, MRW (SRX/NOP Clock-Sync enable), then host shall issue an SRE/SRX pair). Host (including RCD and Clock Driver) is responsible to ensure the same phases of the system clock all the time during DCA training.

Figure 4 — RESET_n and Initialization Sequence at Power-on Ramping

- After RESET_n is de-asserted (T_c), wait at least tINIT3 before driving CS_n high.

3.3.1 Power-up Initialization Sequence (cont'd)

5. After setting CS_n high (Td), wait a minimum of tINIT4 to allow the DRAM CMOS based receiver to register the exit and allow the CS_n, CK, CA, DQ and DQS ODT to go to the defined strap or MRS state (Te). Clock (CK_t, CK_c) is required to be started and stabilized for tCKSRX before exit of tINIT4 (Te). Upon the completion of Te, all ODT states (CA, CS_n, CK, DQ and DQS ODT) should be valid and the DRAM's CS_n receiver should no longer be in its CMOS based mode. ODT termination states will be uncalibrated until completion of ZQCal at (Tj)
6. Upon (Te), NOP commands shall be issued for a minimum of tINIT5 to conclude exit of initialization process and start tXPR timer at (Tf). The system shall wait at least tXPR before issuing any legal configuration commands (Tg). During early configuration steps (Tg to Tk), only MRR, MRW, MPC, VREFCS and VREFCA commands are legal. MRR and MRW command, while legal, may not execute properly until CS and CA training routines are completed.
7. Between (Tg to Tj), the following initial configuration modes shall be completed prior to other training modes:
 - MPC for setting MR13 (tCCD_L*tDLLK) shall be issued before the MPC command to reset the DLL.
 - MPC to execute DLL RESET shall be issued before ZQCal Start
 - MPC to execute ZQCal Start followed by ZQCal Latch shall be issued before any other training modes such as VrefCS, VrefCA, CS and CA Training.
8. Between (Tk to Tz), any number of legal configuration commands are allowed. Many training based commands are optional and may be done at the system architect's discretion and may vary depending on the systems, though proper setting of certain registers, such as those related to Write Leveling Training, is required. The host shall follow Multi-Cycle MPC timing requirements in cases where the alignment between CS_n, CA, and CK is unknown, (ie., prior to successfully completing VREFCS, VREFCA, CS, and CA training commands or host provided successful training solutions). MRW and MRR commands can be used once the alignment between CS_n, CA and CK are known. Single-cycle CS_n assertion are allowed after setting MR2:OP[4]=1.
9. Between (Tk to Tz), the SRX/NOP Clock-Sync feature can be enabled through an MRW command by programming MR13:OP[5]=1. When it is enabled, after CSTM/CATM prior to DCA training, host shall issue an SRE/SRX pair to ensure that the Clock-Sync is in effect during DCA training. It is also applied for CS Geardown Init sequence (for example, after PowerUp Initialization, CSTM, MPC (CS Geardown enable), Sync Pulse, CATM, MRW (SRX/NOP Clock-Sync enable), then host shall issue an SRE/SRX pair). Host (including RCD and Clock Driver) is responsible to ensure the same phases of the system clock all the time during DCA training to make the DCA training effective with the consistent phases of system and DRAM internal clocks.
10. After (Tz), and the completion of any training or calibration timing parameters (i.e. tZQLAT is satisfied), the DDR5 device is ready for normal operation and is able to accept any valid command. Any additional mode registers that have not previously been set up for normal operation should be written at this time. If host use writeback suppression mode, it should be set after the initial write process to prevent aliasing to 2-bit errors.
11. After all mode registers have been programmed for normal operation, optional MBIST mode can be entered by writing MR23:OP[4] to HIGH, followed by subsequent MR24 PPR guard keys, then DRAM will drive ALERT_n to LOW for a maximum of tSELFTEST time. DRAM will drive ALERT_n to HIGH to indicate that this operation is completed. After ALERT_n is driven high, the DRAM is immediately ready to receive valid commands. The MBIST/mPPR transparency status shall subsequently be checked in MR22:OP[2:0] in order to determine whether mPPR should be performed. Please refer to Ch. 4.30 MBIST/mPPR for more detailed operation procedures.

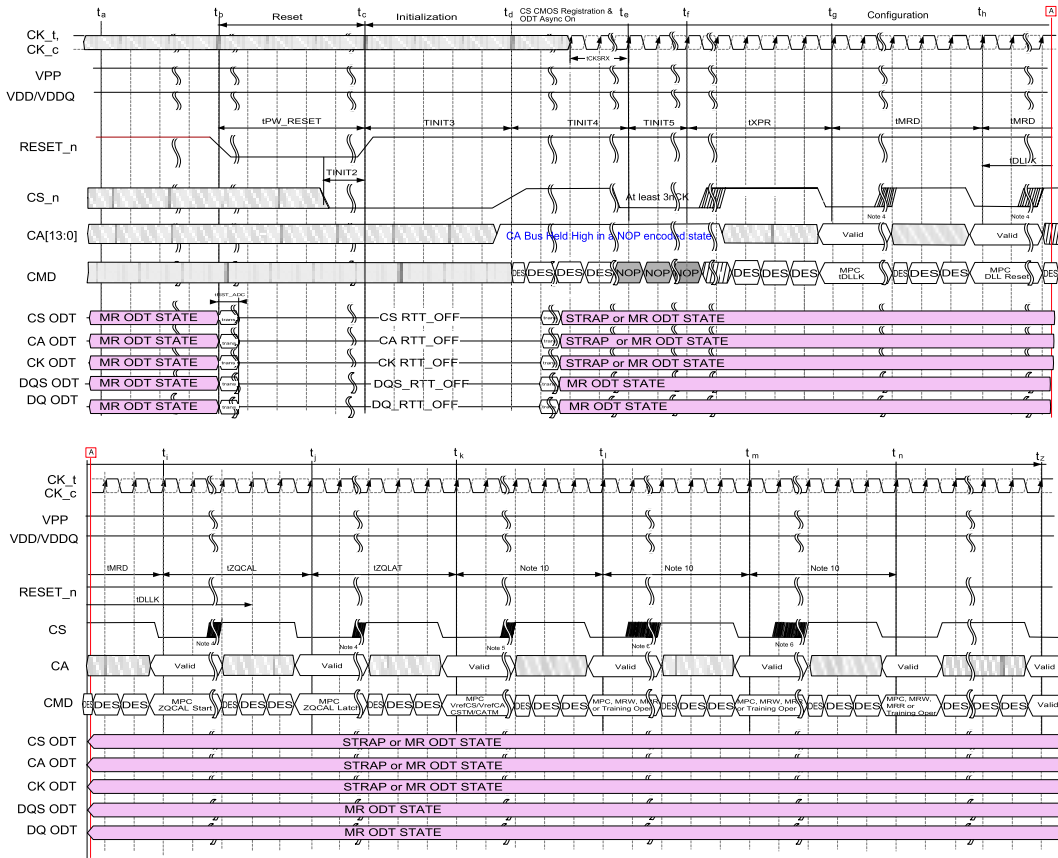
Table 11 — Initialization Timing Parameters

Parameter	Symbol	Value		Units	Note(s)
		MIN	MAX		
Maximum voltage-ramp time	tINIT0	-	20	ms	
Minimum RESET_n LOW time after completion of voltage ramp	tINIT1	200		μs	
Minimum CS_n LOW time before RESET_n HIGH	tINIT2	10	-	ns	
Minimum CS_n LOW time after RESET_n HIGH	tINIT3	4	-	ms	
Minimum time for DRAM to register EXIT on CS_n with CMOS.	tINIT4	2	-	μs	
Minimum cycles required after CS_n HIGH	tINIT5	3	-	nCK	1
Minimum time from Exit Reset to first valid Configuration Command	tXPR	tXS	-	ns	
Minimum stable clock time	tCKSRX	SEE Self Refresh Timing Table			
NOTE 1 Min number of NOP commands issued after CS_n High (tINIT4).					

3.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization as shown in Figure 5.

1. Assert RESET_n below $0.2 \times VDDQ$ anytime when reset is needed. RESET_n needs to be maintained for a minimum of tPW_RESET. CS_n shall be pulled LOW at least tINIT2 before de-asserting RESET_n.
2. Repeat steps 4 to 11 in Section 3.3.1



NOTES:

1. From time point (Td) until (Te), the command/address (CA) bus shall be held high in a NOP encoded state.
2. From time point (Te) until (Tf), NOP commands shall be applied on the command/address (CA) bus.
3. From time point (Tf) until (Tk), DES commands shall be applied between legal commands (MRR, MRW, MPC, VREFCS & VREFCA). MRR and MRW command while legal, may not execute properly until CS and CA training routines are completed.
4. Prior to ZQcal completion at (Tk), MPC commands shall be Multi-Cycle as described in the MPC command Timings section.
5. From time point (Tk) until (Tl) all MPC, VREFCS and VREFCA commands prior to CS and CA training successfully completing, shall be Multi-Cycle (MR2:OP[4]=0) as described in the MPC, VREFCS, and VREFCA timing sections.
6. At time point (Tl), with successful completion of CS and CA training, an MRW command setting MR2:OP[4] = 1 is recommended and allows for MPC, VREFCS, VREFCA commands to be single-cycle, improving training duration.
7. From time point (Tk) until (Tz), DES commands shall be applied between legal commands (MRR, MRW, MPC, VREFCS & VREFCA).
8. Starting at Tl, MRW Commands shall be issued to all Mode Registers that require defined settings.
9. Default ODT tolerances are wider prior to ZQ calibration.
10. All MPC/MRW/MRR to MPC/MRW/MRR commands shall meet the timing restrictions required.
11. MRR is legal after DLL_reset.
12. Between (Tk to Tz), the SRX/NOP Clock-Sync feature can be enabled through an MRW command by programming MR13:OP[5]=1. When it is enabled, after CSTM/CATM prior to DCA training, host shall issue an SRE/SRX pair to ensure that the Clock-Sync is in effect during DCA training. It is also applied for CS Geardown Initialization sequence (for example, after Power-Up Initialization, CSTM, MPC (CS Geardown enable), Sync Pulse, CATM, MRW (SRX/NOP Clock-Sync enable), then host shall issue an SRE/SRX pair). Host (including RCD and Clock Driver) is responsible to ensure the same phases of the system clock all the time during DCA training.

Figure 5 — Reset Procedure at Stable Power

3.3.2 Reset Initialization with Stable Power (cont'd)

Table 12 — Reset Timing Parameters

Parameter	Symbol	Value		Units	Note(s)
		Min	Max		
Minimum RESET_n low time for Reset Initialization with stable power	tPW_RESET	1	-	μS	
Maximum time after RESET_n assertion to ODT off	tRST_ADC	-	50	nS	

3.3.3 Input Voltage Power-up and Power-Down Sequence

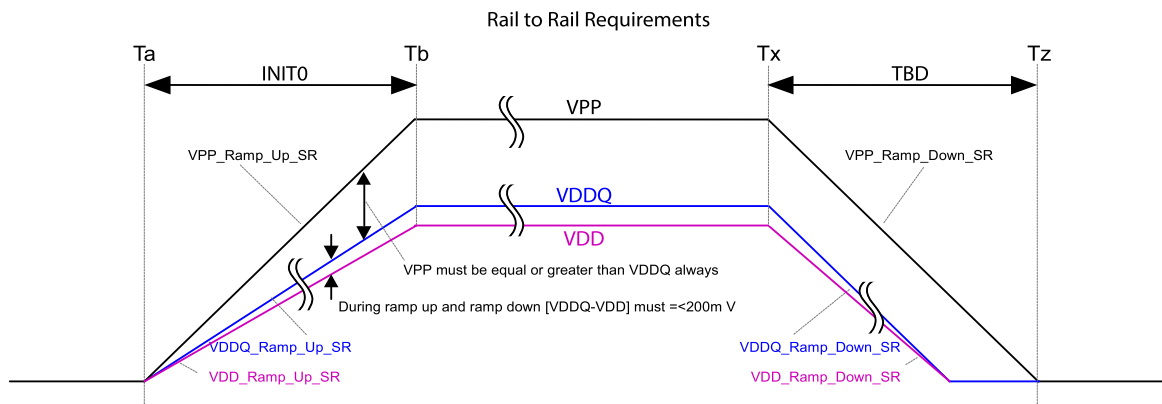


Table 13 — Input Voltage Slew Rates and Power Ramp Down Time

Description	Symbol	Min	Max	Units	Notes
VPP Rail	VPP_Ramp_Up_SR	0.2	5	V/ms	1,2,3,4,5
	VPP_Ramp_Down_SR	0.1	4.5	V/ms	
VDD Rail	VDD_Ramp_Up_SR	0.1	4.5	V/ms	
	VDD_Ramp_Down_SR	0.1	4.5	V/ms	
VDDQ Rail	VDDQ_Ramp_Up_SR	0.1	4.5	V/ms	
	VDDQ_Ramp_Down_SR	0.1	4.5	V/ms	
Power Ramp Down Time	tPRD	-	19.08	ms	
NOTE 1 Both VDD and VPP supply measurements made between 10% and 90% nominal voltage NOTE 2 1Mhz bandwidth limited measurement NOTE 3 VPP shall be equal to or greater than VDD/VDDQ at all times. NOTE 4 During ramp up and ramp down [VDDQ-VDD] must be equal or less than 200 mV. NOTE 5 After tINIT0, all supplies shall be within their specified tolerance, as defined in the DC Operating Tables.					

3.4 Mode Register Definition

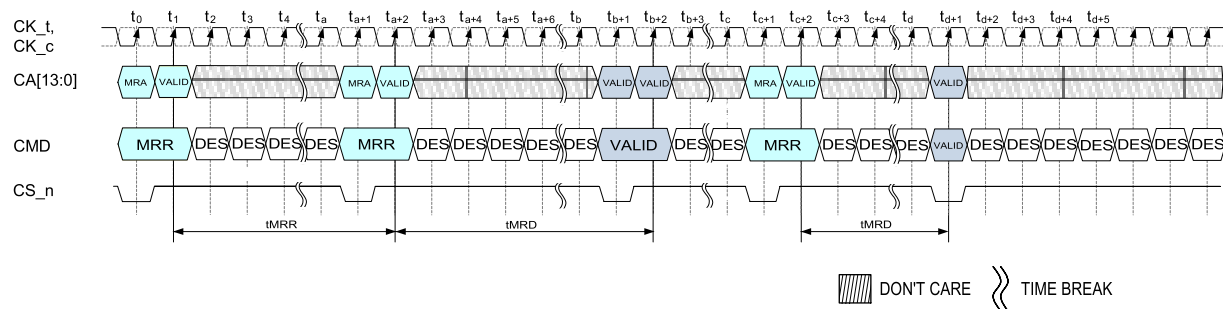
3.4.1 Mode Register Read (MRR)

The Mode Register Read (MRR) command is used to read configuration and status data from the DDR5-SDRAM registers. The MRR command is initiated with CS_n and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[7:0]) allow the user to select one of 256 registers. The mode register contents are available on the second 8 UI's of the burst and are repeated across all DQ's after the CL following the MRR command. To avoid a potentially worst-case pattern, every odd DQ bit (represented with !) shall have its contents inverted. Data in the burst (BL0-7) shall be either "0" or "1", with "1" indicating that the content of the later UI's (BL8-15) are inverted.

MRR commands require all banks to be idle on the DRAM. For 3DS, MRR commands require all banks to be idle on all logical ranks. The 3DS base die (CID[3:0]=0x0) is the targeted logical rank for most Mode Register Reads, however the CID setting of MR14:OP[3:0] designates the targeted logical rank for MRR commands to MR14-MR20, MR22 and MR54-MR57, and still requires all banks to be idle not only on the targeted logical rank but also on all other logical ranks.

DQS is toggled for the duration of the MRR burst. The MRR has a command burst length 16 regardless of the MR0 setting, the training mode or the mode register address. MRR termination control and ODT timings are the same as for the Read command. The MRR operation must not be interrupted. Non-Target ODT encoding is available for MRR, just like a normal Read. MRR NT ODT termination control and ODT timings are the same as for the Read NT command.

In the case that CRC is enabled, MRR's output will come with BL18 (BL16 plus 2 CRC-bit), but the host has the option to consider the 17th and 18th bits "don't care" for MRR handling. Regardless on if the host uses the 17th and 18th bits, while CRC is enabled, the strobe needs to toggle for BL18.



3.4.1 Mode Register Read (MRR) (cont'd)

Table 15 — DQ Output Mapping for x8 Device

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

NOTE 1 The read pre-amble and post-amble of MRR are same as normal read.

Table 16 — DQ Output Mapping for x16 Device (OSC Count - MR46 and MR47 only)

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ9	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ10	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ11	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ12	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ13	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ14	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ15	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

NOTE 1 The read pre-amble and post-amble of MRR are same as normal read.

NOTE 2 Output map excludes per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)

3.4.1 Mode Register Read (MRR) (cont'd)**Table 17 — DQ Output Mapping for x16 Device (DFE Registers Excluded)**

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	Don't Care								
DQ9									
DQ10									
DQ11									
DQ12									
DQ13									
DQ14									
DQ15									
NOTE 1	The read pre-amble and post-amble of MRR are same as normal read.								
NOTE 2	Output of mode register data is only duplicated and inverted across the first 8 bits of a x16 device.								
NOTE 3	Output map excludes per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)								

Table 18 — DQ Output Mapping for x16 Device (DFE Lower Byte - DQ[0:7], DML)

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	Don't Care								
DQ9									
DQ10									
DQ11									
DQ12									
DQ13									
DQ14									
DQ15									
NOTE 1	The read pre-amble and post-amble of MRR are same as normal read.								
NOTE 2	Output of mode register data is only duplicated and inverted across the first 8 bits of a x16 device when reading from a DFE register associated with a lower byte DQ or DML.								
NOTE 3	Output map is ONLY for per bit DFE, DCA and VrefDQ mode registers (MR103 through MR255)								