

JEDEC STANDARD

Double Data Rate (DDR) SDRAM

JESD79F

(Revision of JESD79E, May 2005)

FEBRUARY 2008

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2008
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards and Documents for alternative contact information.

DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

16 M X4 (4 M X4 X4 banks), 8 M X8 (2 M X8 X4 banks), 4 M X16 (1 M X16 X4 banks)

32 M X4 (8 M X4 X4 banks), 16 M X8 (4 M X8 X4 banks), 8 M X16 (2 M X16 X4 banks)

64 M X4 (16 M X4 X4 banks), 32 M X8 (8 M X8 X4 banks), 16 M X16 (4 M X16 X4 banks)

128 M X4 (32 M X4 X4 banks), 64 M X8 (16 M X8 X4 banks), 32 M X16 (8 M X16 X4 banks)

256 M X4 (64 M X4 X4 banks), 128 M X8 (32 M X8 X4 banks), 64 M X16 (16 M X16 X4 banks)

FEATURES

- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4, or 8
- CAS Latency: 2 or 2.5, DDR400 also includes CL = 3
- AUTO PRECHARGE option for each burst access
- Auto Refresh and Self Refresh Modes
- 2.5 V (SSTL_2 compatible) I/O
- VDDQ: +2.5 V ± 0.2 V for DDR 200, 266, or 333
+2.6 ± 0.1 V for DDR 400
- VDD:
+3.3 V ± 0.3 V or +2.5 V ± 0.2 V for DDR 200, 266, or 333
+2.6 ± 0.1 V for DDR 400

GENERAL DESCRIPTION

The DDR SDRAM is a high-speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits:

64 Mb has 67,108,864 bits

128 Mb has 134,217,728 bits

256 Mb has 268,435,456 bits

512 Mb has 536,870,912 bits

1 Gb has 1,073,741,824 bits

The DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR

SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The DDR SDRAM operates from a differential clock (CK and $\overline{\text{CK}}$; the crossing of CK going HIGH and $\overline{\text{CK}}$ going LOW will be referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable read or write burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Initial devices may have a VDD supply of 3.3 V (nominal). Eventually, all devices will migrate to a VDD supply of 2.5 V (nominal). During this initial period of product availability, this split will be vendor and device specific.

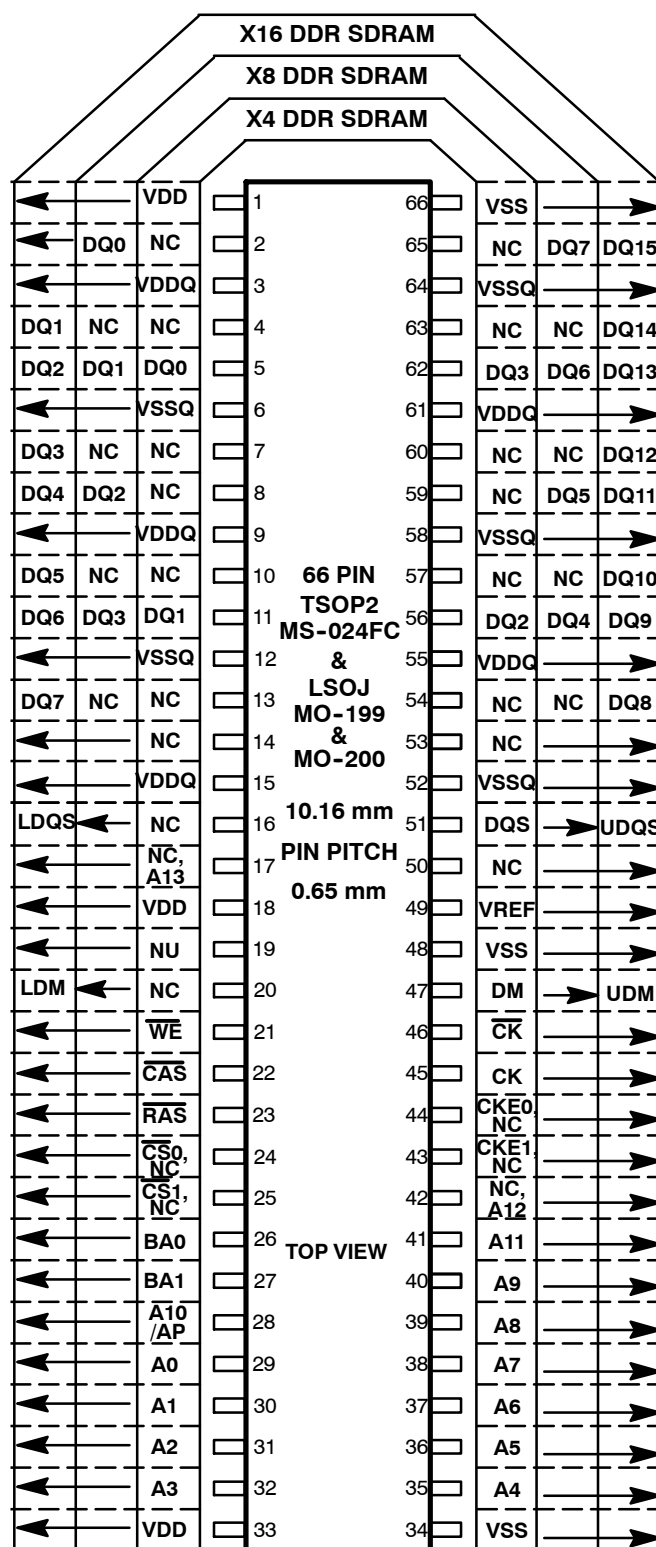
This data sheet includes all features and functionality required for JEDEC DDR devices; options not required, but listed, are noted as such. Certain vendors may elect to offer a superset of this specification by offering improved timing and/or including optional features. Users benefit from knowing that any system design based on the required aspects of this specification are supported by all DDR SDRAM vendors; conversely, users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

Note: The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Note: This specification defines the minimum set of requirements for JEDEC X4/X8/X16 DDR SDRAMs. Vendors will provide individual data sheets in their specific format. Vendor data sheets should be consulted for optional features or superset specifications.

CONTENTS

Features	1	Fig. 27, Write To Read - Max tDQSS, Odd Number of Data, Interrupting	39
General Description	1	Fig. 28, Write To Precharge - Max tDQSS, Non-Interrupting	40
Pin Assignment Diagram, TSOP2 Package	3	Fig. 29, Write To Precharge - Max tDQSS, Interrupting	41
Address Assignment Table 1a TSOP2 Package	3	Fig. 30, Write To Precharge - Max tDQSS, Odd Number of Data, Interrupting	42
Pin Assignment Diagram, BGA Package	4	Precharge	43
Address Assignment Table 1b BGA Package	5	Fig. 31, Precharge Command	43
Functional Block Diagram - X4/X8/X16	5	Powerdown	43
Pin Descriptions, Table 2	6	Fig. 32, Power-Down	44
Functional Description	7	Fig. 33, Clock Frequency Change in Precharge Power-Down Mode	44
Initialization	7	Absolute Maximum Ratings	45
Register Definition	7	Table 5 - Capacitance	45
Mode Register	7	Tab. 6 - DC Electrical Characteristics and Operating Conditions	45
Burst Length	8	Table 7 - AC Operating Conditions	46
Table 3, Burst Definition	8	Table 8 - Low Power DDR SDRAM Electrical Characteristics	46
Fig. 4, Mode Register Definition	8	Table 9 Idd Specifications and Conditions, ...	47 & 48
Burst Type	9	Fig. 34, IDD7 Measurement Timing Waveforms	48
Read Latency	9	Table 10 Low Power DDR Idd Specifications and Conditions, ...	49
Operating Mode	9	Table 11 - AC Electrical Characteristics (Timing Table), ...	50 & 51
Terminology Definitions		AC Timing Variations, DDR200, DDR266, DDR333, Table 12	52
DDR200	9	Fig. 35, Test Reference Load	52
DDR266	9	Fig. 36, Method for Calculating Transitions and Endpoints	53
DDR333	9	Component Specification Notes	52 & 53
DDR400	9	System Characteristics, DDR200, DDR266, & DDR333	54
Fig. 5, Required CAS Latencies	10	Tables 13-19Signal Derating Specifications	54
Extended Mode Register	11	Figs. 37 & 38, AC Overshoot/Undershoot Specification, Tables 20 & 21, ...	55
DLL Enable/Disable	11	Table 22, Clamp V-I Characteristics	56
Output Drive Strength	11	Fig. 39, Pullup Slew Rate Test Load	57
Fig.6, Extended Mode Register Definitions	11	Fig. 40, Pulldown Slew Rate Test Load	57
Commands	12	System Characteristics Notes	57 & 58
Truth Table 1a (Commands)	12	Fig. 41, Full Strength Output V-I Characteristics	59 & 60
Truth Table 1b (DM Operation)	12	Fig. 42 Weak Output V-I Characteristics	61 & 62
Truth Table 2 (CKE)	13	DDR SDRAM Output Driver V-I Characteristics	63
Truth Table 3 (Current State, Same Bank)	14 & 15	Timing Waveforms	
Truth Table 4 (Current State, Different Bank)	16 & 17	Fig. 43, Data Input Timing	64
Fig. 7, Simplified State Diagram	18	Fig. 44, Data Output Timing	64
Command definitions	19 & 20	Fig. 45, Initialize and Mode Register Set	65
DESELECT	19	Fig. 46, Power-Down Mode	66
NO OPERATION (NOP)	19	Fig. 47, Auto Refresh Mode	67
MODE REGISTER SET	19	Fig. 48, Self Refresh Mode	68
ACTIVE	19	Reads	
READ	19	Fig. 49, Read - Without Auto Precharge	69
WRITE	19	Fig. 50, Read - Without Auto Precharge (CL=1.5, BL=4)	70
BURST TERMINATE	19	Fig. 51, Read - With Auto Precharge	71
PRECHARGE	20	Fig. 52, Bank Read Access	72
AUTO PRECHARGE	20	Writes	
REFRESH REQUIREMENTS	20	Fig. 53, Write - Without Auto Precharge	73
AUTO REFRESH	20	Fig. 54, Write - With Auto Precharge	74
SELF REFRESH	20	Fig. 55, Bank Write Accesses	75
Table 4, Row-Column Organization by Density	19	Fig. 56, Write - DM Operation	76
Operations	21	Annex A (Informational) Differences Between 79D and 79C	77
Bank/Row Activation	21		
Fig. 8, Activating a Specific Row	21		
Fig. 9, tRCD & tRRD Definition	21		
Reads	22 & 23		
Fig. 10, Read Command	22		
Fig. 11, Read Burst	24		
Fig. 12, Consecutive Read Bursts	25		
Fig. 13, Nonconsecutive Read Bursts	26		
Fig. 14, Random Read Accesses	27		
Fig. 15, Terminating a Read Burst	28		
Fig. 16, Read to Write	29		
Fig. 17, Read to Precharge	30		
Writes	31		
Fig. 18, Write Command	31		
Fig. 19, Write to Write-Max tDQSS	32		
Fig. 20, Write to Write-Min tDQSS	32		
Fig. 21, Write Burst - Nom., Min., and Max tDQSS	33		
Fig. 22, Write To Write - Max tDQSS	34		
Fig. 23, Write To Write - Max tDQSS, Non Consecutive	35		
Fig. 24, Random Write Cycles - Max tDQSS	36		
Fig. 25, Write To Read - Max tDQSS, Non-Interrupting	37		
Fig. 26, Write To Read - Max tDQSS, Interrupting	38		



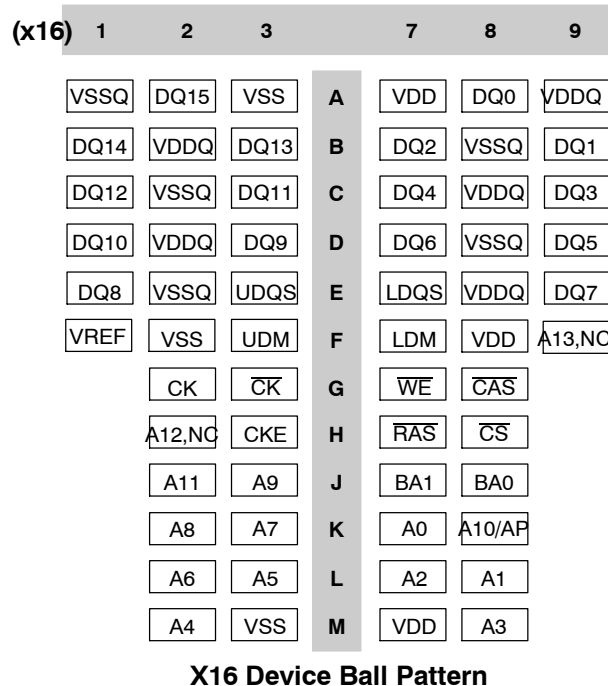
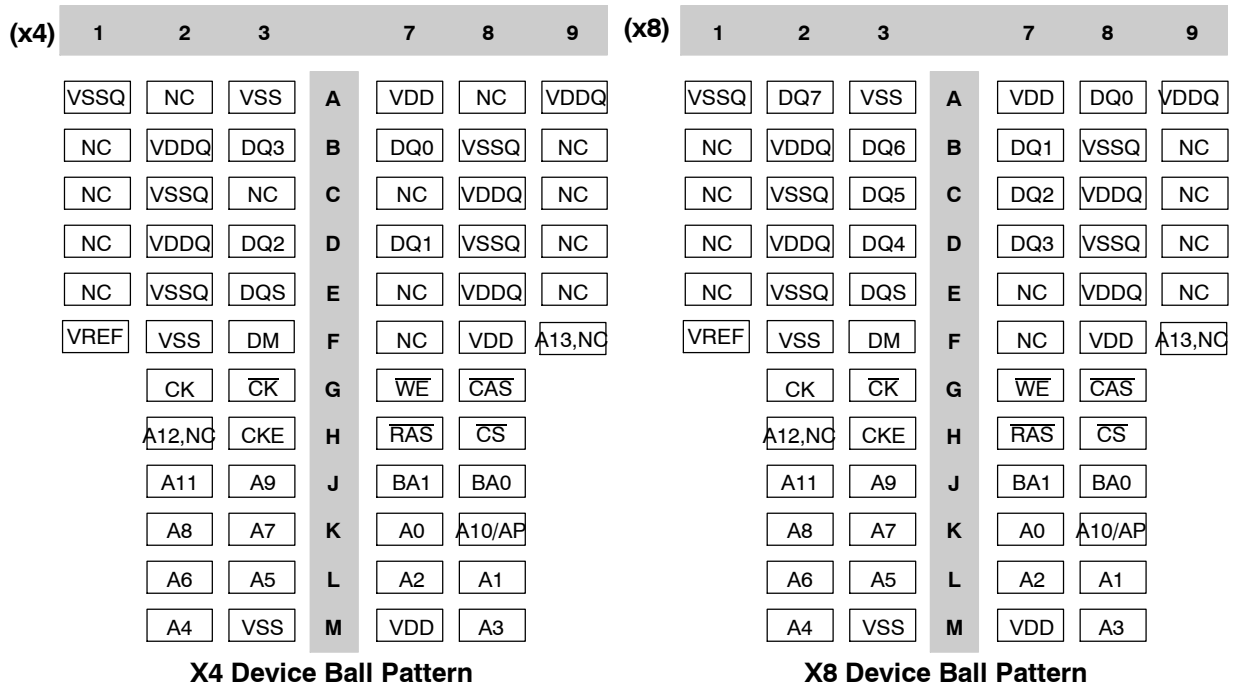
ADDRESS ASSIGNMENT TABLE					
Density	Org.	Bank	Row Addr.	Col Addr	Bank Addr
64 Mb	16M X 4	4	A0⇒A11	A0⇒A9	BA0, BA1
	8M X 8	4	A0⇒A11	A0⇒A8	BA0, BA1
	4M X 16	4	A0⇒A11	A0⇒A7	BA0, BA1
128 Mb	32M X 4	4	A0⇒A11	A0⇒A9, A11	BA0, BA1
	16M X 8	4	A0⇒A11	A0⇒A9	BA0, BA1
	8M X 16	4	A0⇒A11	A0⇒A8	BA0, BA1
256 Mb	64M X 4	4	A0⇒A12	A0⇒A9, A11	BA0, BA1
	32M X 8	4	A0⇒A12	A0⇒A9	BA0, BA1
	16M X 16	4	A0⇒A12	A0⇒A8	BA0, BA1
512 Mb	128M X 4	4	A0⇒A12	A0⇒A9, A11, A12	BA0, BA1
	64M X 8	4	A0⇒A12	A0⇒A9, A11	BA0, BA1
	32M X 16	4	A0⇒A12	A0⇒A9	BA0, BA1
1 Gb	256M X 4	4	A0⇒A13	A0⇒A9, A11, A12	BA0, BA1
	128M X 8	4	A0⇒A13	A0⇒A9, A11	BA0, BA1
	64M X 16	4	A0⇒A13	A0⇒A9	BA0, BA1

TABLE 1a: TSOP2 Device Address Assignment Table

The following pin assignments apply for $\overline{CS}$ and CKE pins for Stacked and Non-stacked devices.

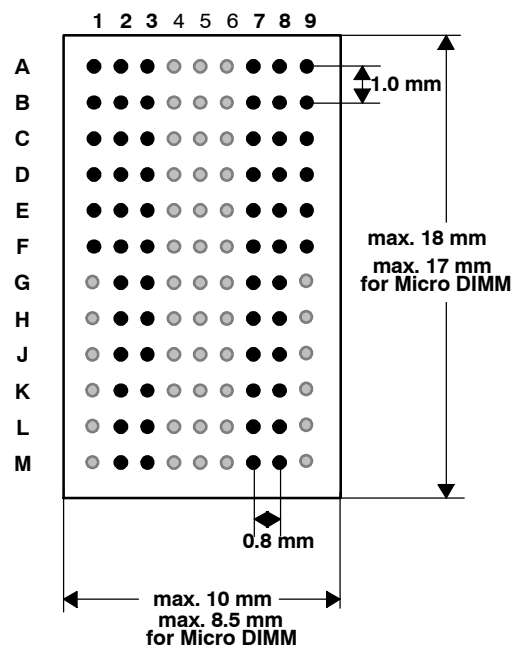
Pin	Non-Stacked	Stacked	
24	$\overline{CS}$	$\overline{CS0}$	
25	NC	$\overline{CS1}$	
43	NC	CKE1	
44	CKE	CKE0	

Figure 1
64 Mb Through 1Gb DDR SDRAM (X4, X8, & X16) IN TSOP2 & LSOJ



● : Ball Existing [For Reference Only]
○ : Depopulated Ball

Top View(See the balls through the Package)

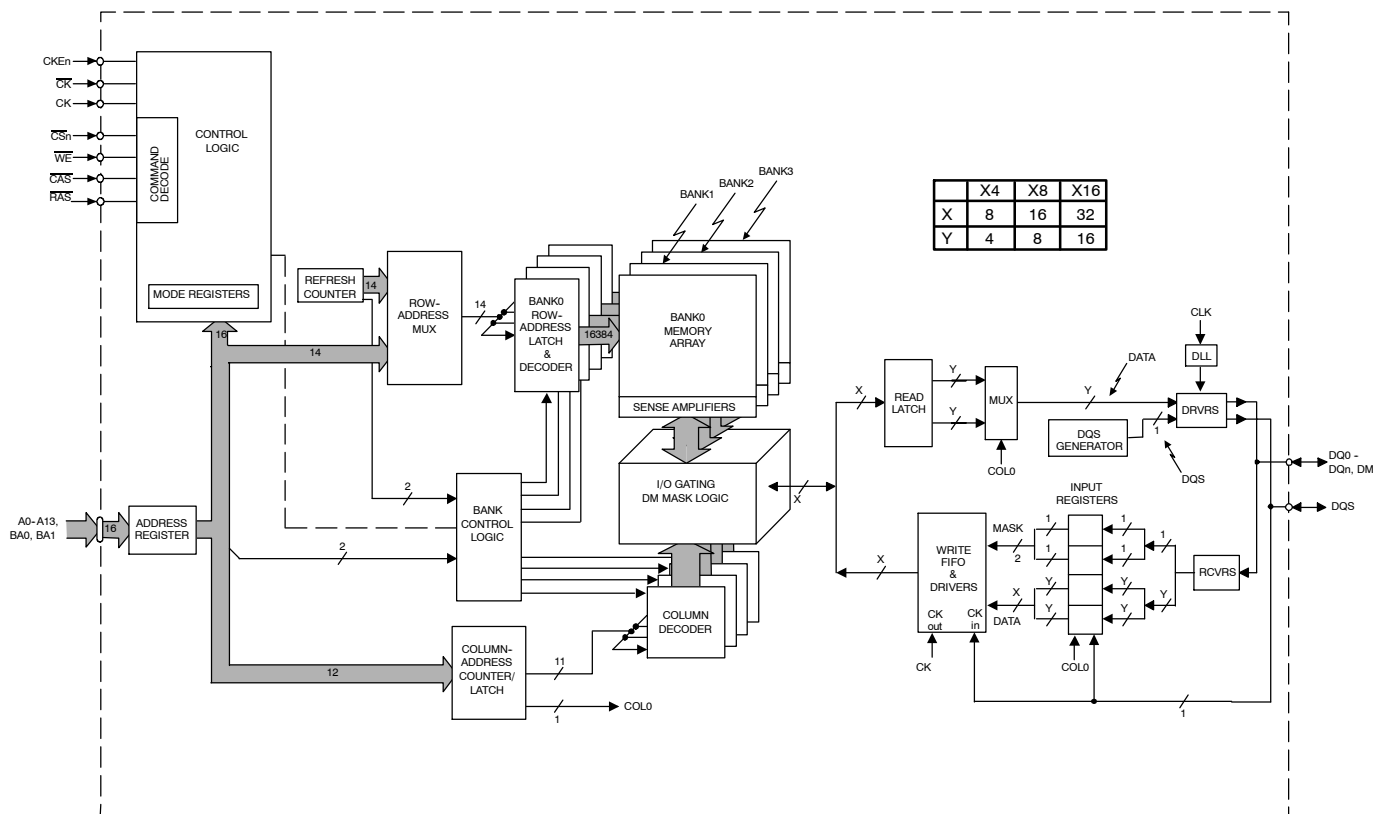


**BGA Package Ball Pattern,
Top View**

Figure 2
128 Mb Through 1Gb DDR SDRAM (X4, X8, & X16) IN BGA

Item	128Mb	256Mb	512Mb	1Gb	Note
Number of banks	4	4	4	4	
Bank Address Pins	BA0, BA1	BA0, BA1	BA0, BA1	BA0, BA1	
Autoprecharge Pins	A10/AP	A10/AP	A10/AP	A10/AP	
Row Addresses	A0-A11	A0-A12	A0-A12	A0-A13	
Column Addresses x4 x8 x16	A0-A9,A11 A0-A9 A0-A8	A0-A9,A11 A0-A9 A0-A8	A0-A9,A11,A12 A0-A9,A11 A0-A9	A0-A9,A11,A12 A0-A9,A11 A0-A9	
H2 pin function	NC	A12	A12	A12	
F13 pin function	NC	NC	NC	A13	
JC11 MO #	MO-233A	MO-233A	MO-233A	MO-233A	
JC11 Variation #	AA	AA	AA	AA	
JC11 Package Name	DSBGA	DSBGA	DSBGA	DSBGA	
Pin Pitch	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	

TABLE 1b: BGA Device Address Assignment and Package Table



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Note 3: Not all address inputs are used on all densities.

FIGURE 3: FUNCTIONAL BLOCK DIAGRAM OF DDR SDRAM

TABLE 2: PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{\text{CK}}$	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to the crossings of CK and $\overline{\text{CK}}$ (both directions of crossing).
CKE (CKE0) (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{\text{CK}}$ and CKE are disabled during POWER-DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied upon 1st power up. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. The standard pinout includes one CKE pin. Optional pinouts include CKE0 and CKE1 on different pins, to facilitate device stacking.
$\overline{\text{CS}}$ ($\overline{\text{CS0}}$) ($\overline{\text{CS1}}$)	Input	Chip Select: All commands are masked when $\overline{\text{CS}}$ is registered high. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. $\overline{\text{CS}}$ is considered part of the command code. The standard pinout includes one $\overline{\text{CS}}$ pin. Optional pinouts include $\overline{\text{CS0}}$ and $\overline{\text{CS1}}$ on different pins, to facilitate device stacking.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
DM (LDM) (UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the X16, LDM corresponds to the data on DQ0-DQ7; UDM corresponds to the data on DQ8-DQ15. DM may be driven high, low, or floating during READs.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A0-A13	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS). A12 is used on device densities of 256Mb and above; A13 is used on device densities of 1Gb.
DQ	I/O	Data Bus: Input/Output.
DQS (LDQS) (UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the X16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15.
NC	—	No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: +2.5 V $\pm$ 0.2 V for DDR 200, 266, or 333 +2.6 $\pm$ 0.1 V for DDR 400
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply: One of +3.3 V $\pm$ 0.3 V or +2.5 V $\pm$ 0.2 V for DDR 200, 266, or 333 +2.6 $\pm$ 0.1 V for DDR 400
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

FUNCTIONAL DESCRIPTION

The DDR SDRAM is a high-speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits:

64Mb has 67,108,864 bits

128Mb has 134,217,728 bits

256Mb has 268,435,456 bits

512Mb has 536,870,912 bits

1Gb has 1,073,741,824 bits

The DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a 2n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins. DQ, DQS, & DM may be floated when no data is being transferred

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A13 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. No power sequencing is specified during power up and power down given the following criteria:

- VDD and VDDQ are driven from a single power converter output, AND
- VTT is limited to 1.35 V, AND
- VREF tracks VDDQ/2

OR, the following relationships must be followed:

- VDDQ is driven after or with VDD such that $VDDQ < VDD + 0.3 \text{ V}$ AND
- VTT is driven after or with VDDQ such that $VTT < VDDQ + 0.3 \text{ V}$, AND
- VREF is driven after or with VDDQ such that $VREF < VDDQ + 0.3 \text{ V}$.

At least one of these two conditions must be met.

Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 μs delay prior to applying an executable command.

Once the 200 μs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any executable command. A PRECHARGE ALL command should be applied, placing the device in the "all banks idle" state.

Once in the idle state, two AUTO refresh cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

REGISTER DEFINITION

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure NO TAG. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which may be self-clearing).

Mode Register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A13 or (A12 on 256Mb/512Mb, A13 on 1Gb see figure 4) specify the operating mode.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure NO TAG. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Table 3
BURST DEFINITION

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:

- For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
- For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
- For a burst length of eight, A3-Ai selects the eight-data-element block; A0-A2 selects the first access within the block.
- Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2-Ai when the burst length is set to four and by A3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

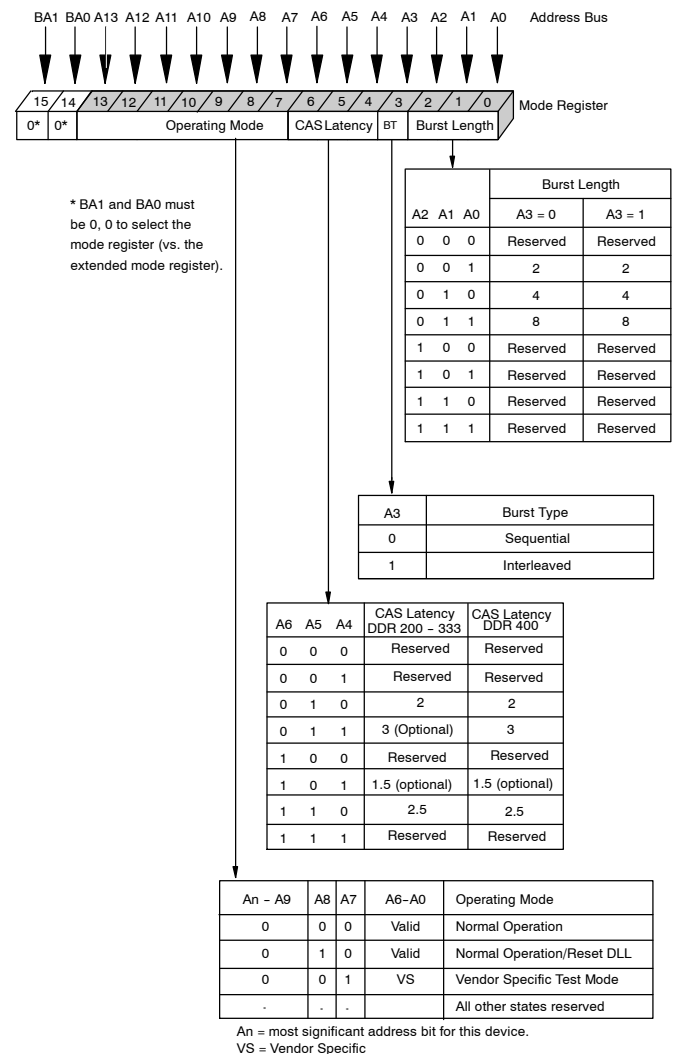


Figure 4
Mode Register Definition

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 3.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. For DDR200, DDR266, and DDR333, the latency can be set to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors). For DDR400, the latency can be set to 3 clocks (latencies of 2 or 2.5 are optional, and one or both of these optional latencies might be supported by some vendors).

If a READ command is registered at clock edge n , and the latency is m clocks, the data will be available nominally coincident with clock edge $n + m$.

Reserved states should not be used as unknown operation, or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set command with bits A7–A13 each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9–A13 each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. A Mode Register Set command issued to reset the DLL must always be followed by a Mode Register Set command to select normal operating mode (i.e., with A8=0).

All other combinations of values for A7–A13 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Terminology Definitions.

The following are definitions of the terms DDR200, DDR266, & DDR333, as used in this specification.

DDR200: A speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 100 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100 MHz clock frequency). The cor-

responding nominal data rate is *200 MHz.

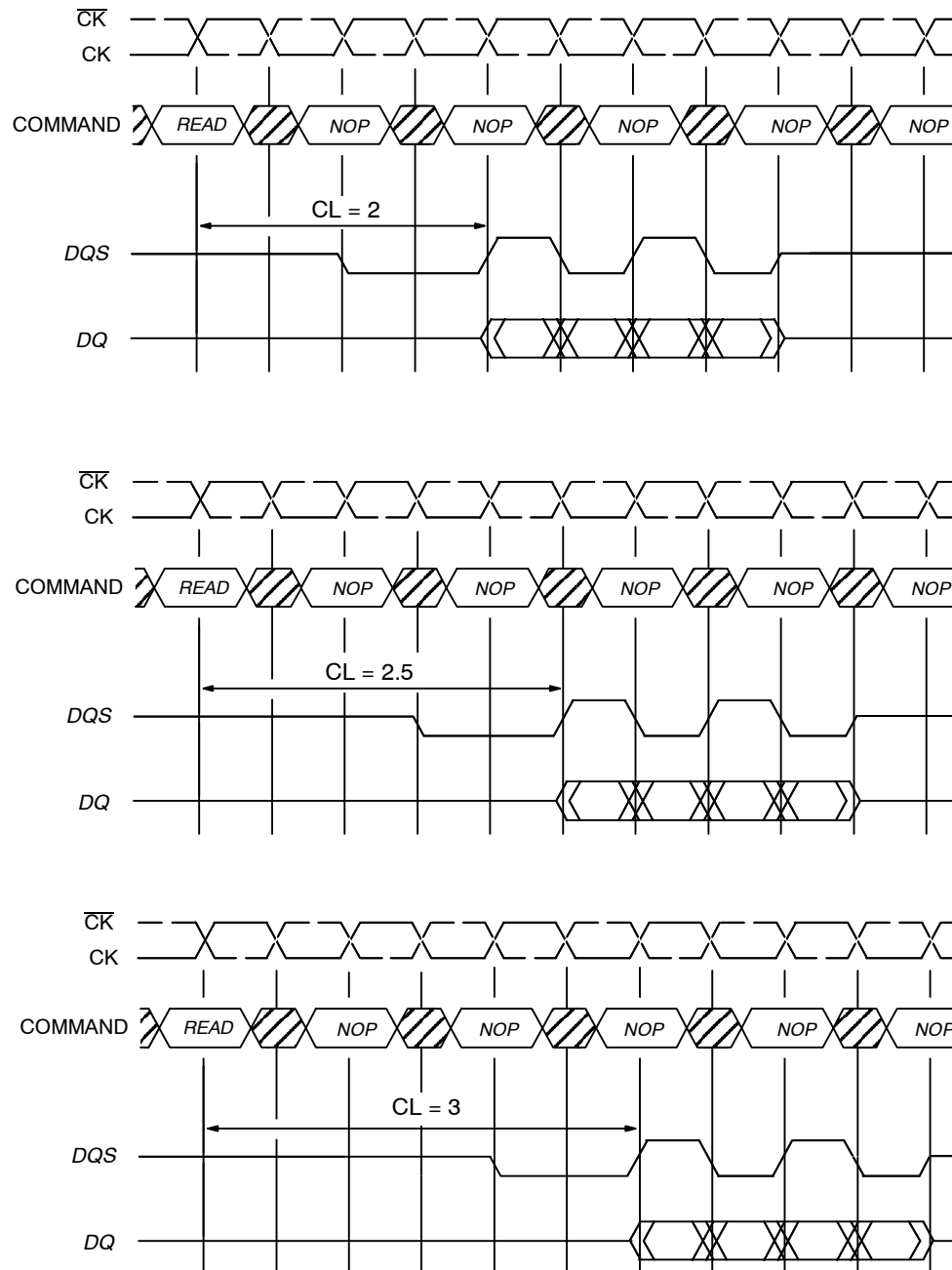
DDR266: A Speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 133 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133 MHz clock frequency). The corresponding nominal data rate is *266 MHz.

DDR333: A Speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 167 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 167 MHz clock frequency). The corresponding nominal data rate is *333 MHz.

DDR400: A Speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 200 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 200 MHz clock frequency). The corresponding nominal data rate is *400 MHz.

In addition to the above DDRxxx specification, a letter modifier may be applied to indicate special timing characteristics for these devices in various market applications. For example, DDR266A and DDR266B classifications define distinct sorts for operation as a function of CAS latency. These differences between sorts are described in Table 12, "AC Timing Variations".

* In this context, the term MHz is used loosely. A more technically precise definition is "million transfers per second per data pin"



Burst Length = 4 in the cases shown
Shown with nominal t_{DQSCK}

 DON'T CARE

Figure 5
REQUIRED CAS LATENCIES

EXTENDED MODE REGISTER

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output drive strength selection (optional). These functions are controlled via the bits shown in Figure 6. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles must occur before any executable command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Some vendors might also support a weak driver strength option, intended for lighter load and/or point-to-point environments. I-V curves for the normal drive strength and weak drive strength are included in this document.

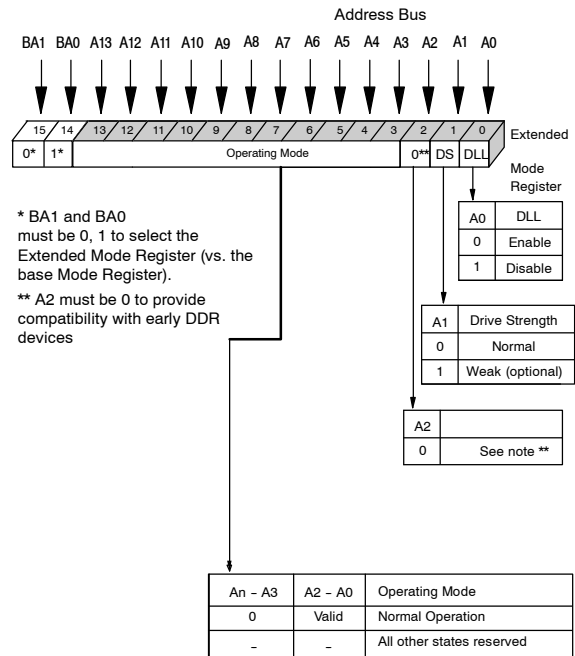


Figure 6
EXTENDED MODE REGISTER
DEFINITION

COMMANDS

Truth Table 1a provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE 1a - Commands

(Notes: 1, 11)

NAME (Function)	CS	RAS	CAS	WE	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	6, 7, 12
MODE REGISTER SET	L	L	L	L	Op-Code	2

TRUTH TABLE 1b - DM Operation

NAME (Function)	DM	DQs	NOTES
Write Enable	L	Valid	10
Write Inhibit	H	X	10

NOTE: 1. CKE is HIGH for all commands shown except SELF REFRESH.

2. BA0-BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A13 provide the op-code to be written to the selected Mode Register.
3. BA0-BA1 provide bank address and A0-A13 provide row address.
4. BA0-BA1 provide bank address; A0-Ai provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0-BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0-BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
9. Deselect and NOP are functionally interchangeable.
10. Used to mask write data, provided coincident with the corresponding data.
11. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
12. VREF must be maintained during Self Refresh operation.

TRUTH TABLE 2 - CKE

(Notes: 1–4, 6)

CKEn-1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power-Down	X	Maintain Power-Down	
L	L	Self Refresh	X	Maintain Self Refresh	7
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	
L	H	Self Refresh	DESELECT or NOP	Exit Self Refresh	5, 7
H	L	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
H	L	Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Truth Table 3		

NOTE: 1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.

2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.

3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.

4. All states and sequences not shown are illegal or reserved.

5. DESELECT or NOP commands should be issued on any clock edges occurring during the tXSNR or tXSRD period. A minimum of 200 clock cycles is needed before applying any executable command, for the DLL to lock.

6. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

7. VREF must be maintained during Self Refresh operation.

TRUTH TABLE 3 - Current State Bank n - Command to Bank n

(Notes: 1-6, 13; notes appear below and on next page)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	MODE REGISTER SET	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start new WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start precharge)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start precharge)	8, 11

NOTE:

- This table applies when $CKEn-1$ was HIGH and $CKEn$ is HIGH (see Truth Table 2) and after $tXSNR$ or $tXSRD$ has been met (if the previous state was self refresh).
- This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
- Current state definitions:
 - Idle: The bank has been precharged, and tRP has been met.
 - Row Active: A row in the bank has been activated, and $tRCD$ has been met. No data bursts/accesses and no register accesses are in progress.
 - Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
 - Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
- The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
 - Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
 - Row Activating: Starts with registration of an ACTIVE command and ends when $tRCD$ is met. Once $tRCD$ is met, the bank will be in the "row active" state.
 - Read w/Auto-Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
 - Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

NOTE (continued):

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

Refreshing:	Starts with registration of an AUTO REFRESH command and ends when tRC is met. Once tRFC is met, the DDR SDRAM will be in the "all banks idle" state.
Accessing Mode Register:	Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMRD is met, the DDR SDRAM will be in the "all banks idle" state.
Precharging All:	Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for pre-charging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with AUTO PRECHARGE enabled and Reads or Writes with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst Terminate must be used to end the READ prior to asserting a WRITE command.
13. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

TRUTH TABLE 4 - Current State Bank n - Command to Bank m

(Notes: 1-6, 10; notes appear below and on next page)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start WRITE burst)	3a, 7, 9
	L	L	H	L	PRECHARGE	
Write (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start new WRITE burst)	3a, 7
	L	L	H	L	PRECHARGE	

NOTE:

- This table applies when $CKEn-1$ was HIGH and $CKEn$ is HIGH (see Truth Table 2) and after $tXSNR$ or $tXSRD$ has been met (if the previous state was self refresh).
- This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
- Current state definitions:
 - Idle: The bank has been precharged, and tRP has been met.
 - Row Active: A row in the bank has been activated, and $tRCD$ has been met. No data bursts/accesses and no register accesses are in progress.
 - Read: A READ burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
 - Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.

NOTE: (continued)

3. Current state definitions: (Continued)

Read with Auto

Precharge Enabled: See following text, notes 3a, 3b, and 3c:

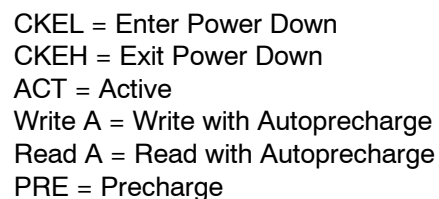
Write with Auto

Precharge Enabled: See following text, notes 3a, 3b, and 3c:

- 3a. For devices which *do not support* the optional “concurrent auto precharge” feature, the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).
- 3b. For devices which *do support* the optional “concurrent auto precharge” feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided.)
- 3c. The minimum delay from a read or write command with auto precharge enable, to a command to a different bank, is summarized below, for both cases of “concurrent auto precharge,” supported or not:

From Command	To Command (different bank)	Minimum Delay without Concurrent Auto Precharge Support	Minimum Delay with Concurrent Auto Precharge Support	Units
Write w/AP	Read or Read w/AP	$1 + (BL/2) + (tWR/tCK)$ (rounded up)	$1 + (BL/2) + tWTR$	tCK
	Write or Write w/AP	$1 + (BL/2) + (tWR/tCK)$ (rounded up)	BL/2	tCK
	Precharge or Activate	1		tCK
Read w/AP	Read or Read w/AP	BL/2		tCK
	Write or Write w/AP	CL (rounded up) + (BL/2)		tCK
	Precharge or Activate	1		tCK

4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of data output, otherwise a Burst Terminate must be used to the READ prior to asserting a WRITE command..
10. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.



AVA Documents
Document Sharing Hub

DESELECT

The Deselect function ($\overline{CS}$ = High) prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to a DDR SDRAM which is selected ($\overline{CS}$ is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET

The mode registers are loaded via inputs A0–A13. See mode register descriptions in the Register Definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A13 selects the row. This row remains active (or open) for accesses until a precharge (or READ or WRITE with AUTOPRECHARGE) is issued to that bank. A PRECHARGE (or READ or WRITE with AUTOPRECHARGE) command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai, shown in Table 4, selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai, shown in Table 4, selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

Density	Column Address			Row Address
	X16	X8	X4	
64 Mb	A0⇒A7	A0⇒A8	A0⇒A9	A0⇒A11
128 Mb	A0⇒A8	A0⇒A9	A0⇒A9,A11	A0⇒A11
256 Mb	A0⇒A8	A0⇒A9	A0⇒A9,A11	A0⇒A12
512 Mb	A0⇒A9	A0⇒A9,A11	A0⇒A9,A11,A12	A0⇒A12
1 Gb	A0⇒A9	A0⇒A9,A11	A0⇒A9,A11,A12	A0⇒A13

Table 4

ROW-COLUMN ORGANIZATION BY DENSITY

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual Read or Write command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

REFRESH REQUIREMENTS

DDR SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 64 ms interval defines the average refresh interval, tREFI, which is a guideline to controllers for distributed refresh timing. For example, a 256 Mb DDR SDRAM has 8192 rows resulting in a tREFI of 7.8 μ s. To avoid excessive interruptions to the memory controller, higher density DDR SDRAMs maintain the 7.8 μ s average refresh time and perform multiple internal refresh bursts. In these cases, the refresh recovery times, tRFC and tXSNR, are extended to accommodate these internal operations.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS-BEFORE-RAS (CBR) refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The DDR SDRAM requires AUTO REFRESH cycles at an average periodic interval of tREFI (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is $8 * tREFI$.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH. Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles should occur before a READ command can be issued. Input signals except CKE are "Don't Care" during SELF REFRESH. Since CKE is an SSTL 2 input, VREF must be maintained during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra auto refresh command is recommended.

OPERATIONS

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command (Figure 8), which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (pre-charged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

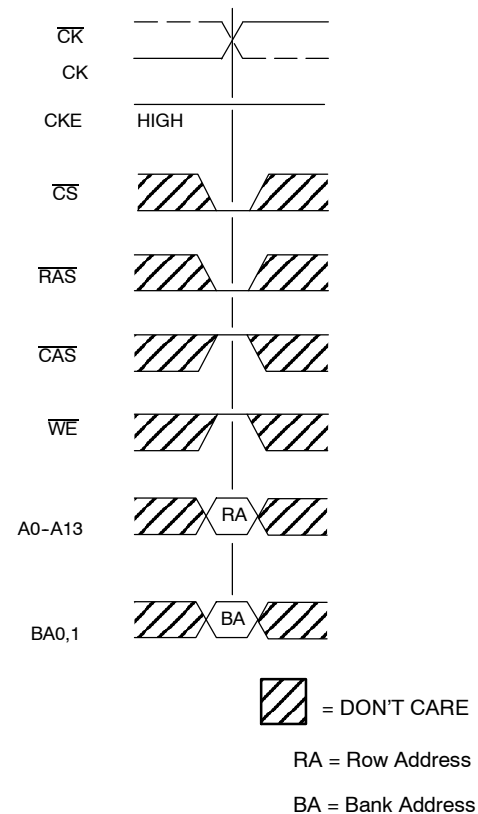


Figure 8
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

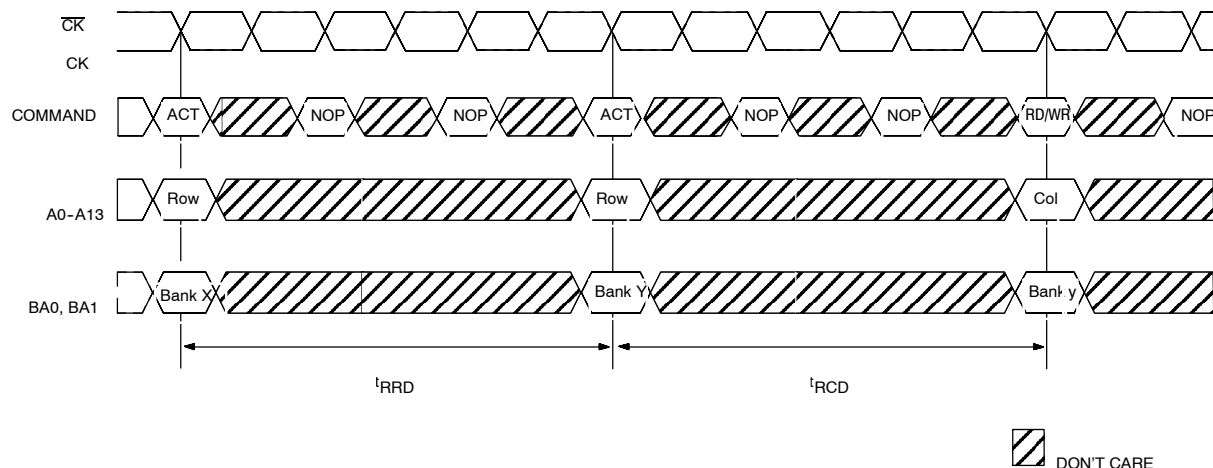


Figure 9
tRCD and tRRD Definition

Reads

READ bursts are initiated with a READ command, as shown in Figure 10.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row that is accessed will start precharge at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and $\overline{CK}$). Figure 11 shows general timing for each required (CL=2 and CL=2.5 and CL=3) CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 12. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive READ data is shown for illustration in Figure 13. Full-speed random read accesses within a page (or pages) can be performed as shown in Figure 14.

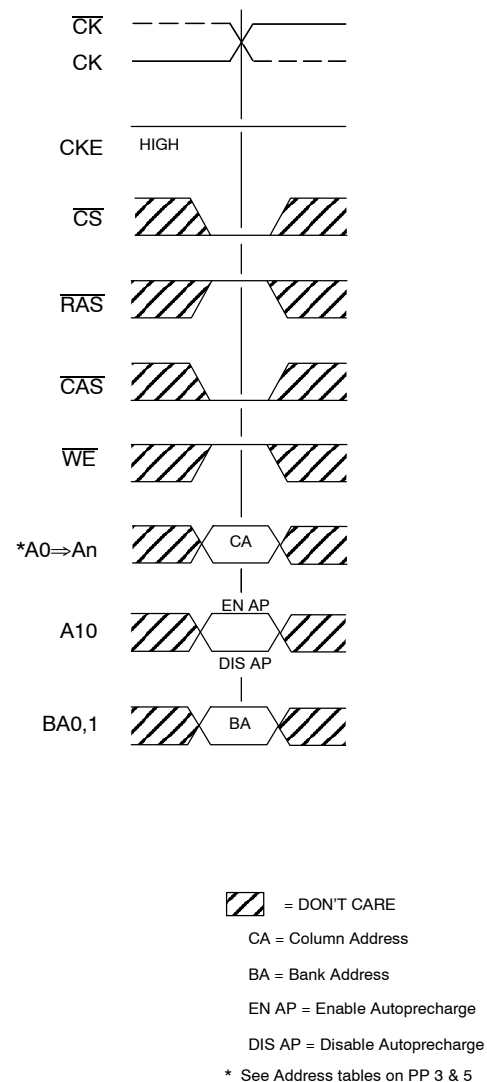


Figure 10
READ COMMAND