

JEDEC STANDARD

Stub Series Terminated Logic for 1.8 V (SSTL_18)

JESD8-15A

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STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18)

(From JEDEC Board Ballots JCB-02-36, JCB-02-37, JCB-02-55, JCB-02-56, JCB-02-57, JCB-02-83, JCB-02-119, and JCB-03-40 formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_18 logic switching range, nominally 0 V to 1.8 V. The standard may be applied to ICs operating with separate V_{DD} and V_{DDQ} supply voltages. The V_{DD} value is not specified in this standard; however V_{DD} and V_{DDQ} will have the same voltage level in many cases.

1.1 Standard Structure

The standard is defined in four clauses:

The first clause defines pertinent supply voltage requirements common to all compliant ICs.

The second clause defines the minimum dc and ac input parametric requirements and ac test conditions for inputs on compliant devices.

The third clause specifies the minimum required output characteristics of, and ac test conditions for, compliant outputs targeted for various application environments.

The fourth clause specifies requirements for differential signaling.

The full input reference level (V_{REF}) range specified is required on each IC in order to allow any SSTL_18 integrated circuit to receive signals from any SSTL_18 output driver.

1.2 Rationale and assumptions

The SSTL_18 standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs. External resistors provide this isolation and also reduce the on-chip power dissipation of the drivers. Busses may be terminated by resistors to an external termination voltage.

Actual selection of the resistor values is a system design decision and beyond the scope of this standard. However in order to provide a basis, the driver characteristics will be derived in terms of a typical 50 Ω environment.

While driver characteristics are derived from a 50 Ω environment, this standard will work for other impedance levels. The system designer will be able to vary impedance levels, termination resistors and supply voltage and be able to calculate the effect on system voltage margins. This is accomplished precisely because drivers and receivers are specified independently of each other. The standard defines a reference voltage V_{REF} which is used at the receivers as well as a voltage V_{TT} to which termination resistors are connected. In typical applications, V_{REF} and V_{TT} are nominally equal to $V_{DDQ}/2$.

2 Supply voltage and input logic levels

The standard defines both the ac and dc input signal values. Making this distinction is important for the design of the high gain, differential receivers that are required. The ac values indicate the voltage levels at which the receiver must meet its timing specifications. The dc values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. Once the receiver input has crossed the ac value, the receiver will change to the new logic state. The new logic state will then be maintained as long as the input stays beyond the dc threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform “ringing”. The relationship of the different levels is shown in Figure 1. An example of ringing is illustrated in the waveform.

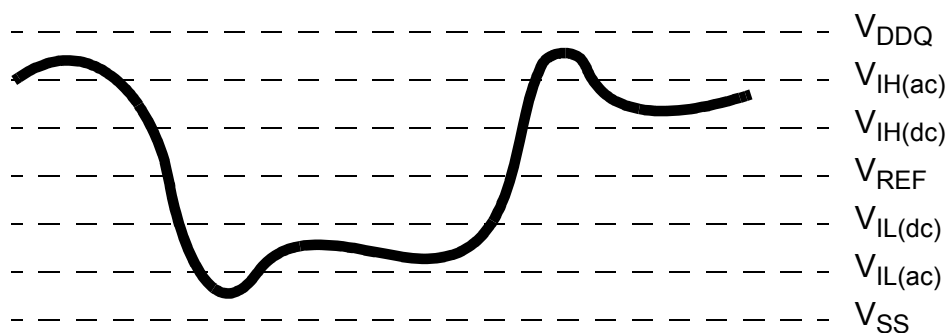


Figure 1 — SSTL_18 Input Voltage Levels

2.1 Supply Voltage Levels

Table 1 — Supply Voltage Levels

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
V_{DDQ}	Output supply voltage	1.7	1.8	1.9	V	
V_{REF}	Input reference voltage	833	900	969	mV	1, 2
V_{TT}	Termination voltage	$V_{REF} - 40$	V_{REF}	$V_{REF} + 40$	mV	3

NOTE 1 The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be $(50 \pm 1)\% \cdot V_{DDQ}$ of the transmitting device, e.g., $V_{REF} \text{ min} = 0.49 \cdot V_{DDQ} \text{ min}$ and $V_{REF} \text{ max} = 0.51 \cdot V_{DDQ} \text{ max}$. V_{REF} is expected to track variations in V_{DDQ} .

NOTE 2 Peak to peak ac noise on V_{REF} may not exceed $\pm 2\%$ of $V_{REF(dc)}$.

NOTE 3 V_{TT} is expected to track V_{REF} of the receiving device.

2.2 Input logic levels

Table 2 — DC input logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH(dc)}$	dc input logic high	$V_{REF} + 125$	$V_{DDQ} + 300$	mV	1
$V_{IL(dc)}$	dc input logic low	-300	$V_{REF} - 125$	mV	1

NOTE 1 Within this standard, it is the relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device that determines noise margins. However, in the case of $V_{IH(dc)}$ max (i.e., input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented that supports SSTL_18 inputs but has no SSTL_18 outputs (e.g., a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 2.2 V (V_{DDQ} max + 300 mV).

Table 3 — AC input logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH(ac)}$	ac input logic high	$V_{REF} + 250$	-	mV	
$V_{IL(ac)}$	ac input logic low	-	$V_{REF} - 250$	mV	

2.3 AC test conditions

The ac input test conditions are specified to be able to obtain reliable, reproducible test results in an automated test environment, where a relatively high noise environment makes it difficult to create clean signals with limited swing. The tester may therefore supply signals with a 1.0 V peak to peak swing to drive the receiving device. Note however, that all timing specifications are still set relative to the ac input level. This is illustrated in Figure 2.

Table 4 — AC input test conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	$0.5 * V_{DDQ}$	V	1, 4
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1, 2
SLEW	Input signal minimum slew rate	1.0	V/ns	3

NOTE 1 Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test. Table 1 identifies the V_{REF} range supported in SSTL_18.

NOTE 2 Compliant devices must still meet the $V_{IH(ac)}$ and $V_{IL(ac)}$ specifications under actual use conditions.

NOTE 3 The input signal minimum slew rate is to be maintained over the range from $V_{IL(dc)}$ max to $V_{IH(ac)}$ min for rising edges and the range from $V_{IH(dc)}$ min to $V_{IL(ac)}$ max for falling edges as shown in Figure 2, consistent with the specifications of Tables 2 and 3. This is not a monotonicity requirement: ringing is still allowed as shown in Figure 1.

NOTE 4 ac test conditions may be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis that the device will meet its timing specifications under all supported voltage conditions.