

JEDEC STANDARD

Bus Interconnect Logic (BIC) for 1.2 Volts

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BUS INTERCONNECT LOGIC (BIC) FOR 1.2 V

(From JEDEC Board Ballot JCB-04-101, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the input and output specifications for devices that are designed to operate in the BIC logic switching range, nominally 0 V to 1.2 V. The standard may be applied to ICs operating with separate V_{DD} and V_{DDQ} supply voltages; however, the V_{DD} value is not specified in this standard. The standard also suggests bus configurations in which optimum performance may be gained.

The standard defines the voltage thresholds, termination schemes, and test conditions for BIC compatibility. Class structures have been established to standardize output drive characteristics under various application conditions. Vendors may specify tighter tolerances on any or all parameters to increase performance.

2 Overview

BIC is defined in both a differential form and a single ended with V_{REF} form. While the two versions have different signal requirements and are not fully interchangeable, they are compatible at the signal level and can be interconnected with minimal performance degradation.

BIC is optimized for use with on die termination (ODT). In some applications, this allows the components on the interface to be actively tuned for optimum performance and low noise under varying conditions.

The single ended version has been optimized for parallel bus operation, requiring termination at both the source and receiver. It is expected that all termination will be on die, eliminating the need for external resistors, but external resistive components are compatible with BIC should the application require them.

The differential version of BIC has been optimized for distributing clock signals or other very high-speed signals where signal integrity is critical. Differential BIC can also be used for parallel busses, if the user can tolerate the extra signal lines required for differential signaling.

This standard is a physical interface only and does not define training, or other potential bus architecture requirements, but BIC is fully compatible with these if the user wishes to expand upon BIC capabilities.

3 Standard specifications for single ended interfaces

3.1 Supply voltage levels

Table 1 — Supply voltage levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Device supply voltage	n/a	n/a	n/a	V	1
V_{DDQ}	Output supply voltage	1.14	1.2	1.26	V	
$V_{REF}(dc)$	Input reference voltage	$0.48 * V_{DDQ}$	$0.5 * V_{DDQ}$	$0.52 * V_{DDQ}$	V	2
$V_{REF}(ac)$	Input reference voltage	$0.47 * V_{DDQ}$	$0.5 * V_{DDQ}$	$0.53 * V_{DDQ}$	V	2
V_{TT}	Termination voltage		$V_{DDQ}/2$		V	3

NOTE 1 Interface is not affected by device core voltage.

NOTE 2 The referenced V_{DDQ} is the power supply voltage for the device receiving the V_{REF} input. $V_{REF}(ac)$ is $V_{REF}(dc)$ plus noise. Peak to peak noise on $V_{REF}(ac)$ may not exceed 2% of $V_{REF}(dc)$.

NOTE 3 The interface may be used with either ODT or external termination. The termination voltage V_{TT} may either be supplied by an independent power supply or created through a Thevenin equivalent circuit. Regardless, the termination should be arranged for optimum signal integrity balanced at $V_{DDQ}/2$ at the receiver. The min and max values should be set by the system designer to meet application needs.

3.2 Input voltage levels

Table 2 — Input voltage levels

Symbol	Parameter	Min.	Nom	Max	Units	Notes
$V_{IH}(dc)$	dc input high	$V_{REF} + 0.08$		$V_{DDQ} + 0.15$	V	4, 6
$V_{IL}(dc)$	dc input low	-0.15		$V_{REF} - 0.08$	V	6
$V_{IH}(ac)$	ac input high	$V_{REF} + 0.15$		$V_{DDQ} + 0.24$	V	4, 5, 6
$V_{IL}(ac)$	ac input low	-0.24		$V_{REF} - 0.15$	V	5, 6

NOTE 4 It is expected that most BIC compatible devices will utilize input clamp diodes, restricting the input voltage to the levels shown. For devices that have been specifically designed for hot insertion or power down on an active bus, the maximum input voltage shall be 1.26 V, regardless of the level of V_{DDQ} .

NOTE 5 The ac timing measurements, including propagation delays and setup/hold times will be measured beginning when the input signal crosses V_{REF} . The ac overshoot above V_{DDQ} and below V_{SS} should not exceed 20% of the duty cycle of the signal, or exceed vendor specified limits.

NOTE 6 For optimum noise margin and performance, the signal must maintain a center balance around $V_{DDQ}/2$, V_{REF} , and V_{TT} , both at the driver and the receiver. Furthermore, V_{REF} of the receiving device should track the variations in the dc value of the V_{DDQ} of the sending device.

3 Standard specifications for single ended interfaces (cont'd)

3.3 Devices with On Die Termination (ODT)

The standard termination for BIC is a resistor (R_T) at the end of the transmission line tied to a voltage level (V_T) that is $\frac{1}{2} V_{DDQ}$. BIC devices may perform the termination function internally with On Die Termination (ODT) or externally with discrete devices. V_T may be externally supplied, internally supplied, or generated through a Thevenin equivalent circuit within the device. If ODT is used, the parameters for specifying ODT as shown in Table 3 must be used.

Table 3 — BIC Input Impedance Parameters for Devices with Thevenin ODT

Symbol	Parameter Description	Units	Notes
R_T	Termination impedance	Ω	7
R_{IL}	Specified input impedance when the input is logic low	Ω	8
R_{IH}	Specified input impedance when the input is logic high	Ω	9
$R_{I\Delta}$	Correlation between R_{IL} and R_{IH}	%	10

NOTE 7 R_T is the termination impedance. In order to identify differences in the value of R_T between input high and low conditions in ODT devices, the value of R_T will be described and specified as R_{IL} when the input is low and R_{IH} when the input is high. Either R_T or both R_{IL} and R_{IH} must be specified. It is not necessary to specify all three values.

NOTE 8 R_{IL} is the value of R_T when ODT is active and the input is held at the nominal logic low position. The tested value of R_{IL} must not exceed $\pm 15\%$ of the specified value of R_{IL} .

NOTE 9 R_{IH} is the value of R_T when ODT is active and the input is held at the nominal logic high position. The tested value of R_{IH} must not exceed $\pm 15\%$ of the specified value of R_{IH} .

NOTE 10 $R_{I\Delta} = (\text{actual } R_{IH} - \text{actual } R_{IL}) / (0.5 * (\text{actual } R_{IH} + \text{actual } R_{IL}))$. The correlation between R_{IL} and R_{IH} must not exceed 10%.

3.3.1 Testing devices with On Die Termination (ODT)

The testing of ODT consists of forcing a current, and verifying that the input voltage falls within an expected range. This test is performed at the nominal logic high and low voltage levels. If the values of either R_T or V_T are outside of tolerances, one or both of the tests will fail. Table 4 shows the test condition limits for a BIC input with ODT turned on with $\pm 15\%$ impedance tolerance. The measured values of V_{IL} and V_{IH} must be used to calculate and guarantee $R_{I\Delta}$.

Table 4 — Impedance test Limits

Symbol	Parameter and Condition	Min	Nom	Max	Unit
V_{IL}	Input low, $I_L = 0.25 * V_{DDQ} / R_{IL}$	$0.212 * V_{DDQ}$	$0.25 * V_{DDQ}$	$0.288 * V_{DDQ}$	V
V_{IH}	Input high, $I_H = -0.25 * V_{DDQ} / R_{IH}$	$0.712 * V_{DDQ}$	$0.75 * V_{DDQ}$	$0.788 * V_{DDQ}$	V

3.3 Devices with On Die Termination (ODT) (cont'd)

3.3.2 Applications information for ODT use with BIC (for reference only)

When optimizing ODT for use in typical transmission line environments, the ODT impedance should be equal to or greater than the transmission line impedance for optimal performance. Setting the ODT impedance to match the transmission line impedance will avoid reflections in ideal applications. In less than ideal applications, losses, noise and other anomalies will degrade the signal on the transmission line prior to the arrival at the ODT, making it desirable to slightly increase the impedance value of ODT to compensate. Increasing the value of ODT impedance will increase the edge rate of incoming signals in most applications, benefiting timing margins and accuracy.

Implementation of ODT as a Thevenin circuit to V_{DDQ} increases power dissipation by providing a current path directly through the pull up and pull down impedances from V_{DDQ} to V_{SS} . Increasing the ODT impedance of Thevenin implementations will reduce power consumption. Turning ODT off when the device is not receiving will also reduce power consumption in Thevenin implementations. This is especially true in bi-directional devices when the device is transmitting.

Table 5 shows an example of an ODT specification for use in a 50 Ω environment. In the example, the impedance is specified as both an R_{IL} and R_{IH} . The impedance is set at 55 Ω to allow for losses and to provide a clean signal edge. In addition, the vendor would need to include a table similar to Table 4 to guarantee test limits.

Table 5 — Example of an ODT specification for a 50 Ω environment

Symbol	Parameter Description	Value	Units
R_T	Termination impedance	55	Ω
$R_{I\Delta}^\dagger$	Correlation between R_{IL} and R_{IH}	± 10	%
$^\dagger R_{I\Delta} = (R_{IH} - R_{IL}) / (0.5 * (R_{IH} + R_{IL}))$ where R_{IH} is R_T measured at $V_I = 0.75 * V_{DDQ}$ and R_{IL} is R_T measured at $V_I = 0.25 * V_{DDQ}$.			

Table 6 shows an example of an ODT specification for a device with adjustable input impedance. In the example, the impedance can be set at any value from 55 Ω to 85 Ω . The vendor would also need to include a table similar to Table 4 to guarantee test limits.

Table 6 — Example of a specification for a device with variable ODT

Symbol	Parameter Description	Min	Max	Units
R_{IL}	Specified input impedance when the input is logic low	50	85	Ω
R_{IH}	Specified input impedance when the input is logic high	50	85	Ω
$R_{I\Delta}^\dagger$	Correlation between R_{IL} and R_{IH}		± 10	%
$^\dagger R_{I\Delta} = (R_{IH} - R_{IL}) / (0.5 * (R_{IH} + R_{IL}))$ where R_{IH} measured at $V_I = 0.75 * V_{DDQ}$ and R_{IL} is measured at $V_I = 0.25 * V_{DDQ}$.				