

JEDEC STANDARD

FBDIMM Specification: High Speed Differential PTP Link at 1.5 V

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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FBDIMM HIGH SPEED DIFFERENTIAL PTP LINK AT 1.5 V

Introduction

This specification is a JEDEC standard for the point-to-point link for the Fully Buffered DIMM. It is the result of a large amount of work from many people and is derived from prior internal specifications used at Intel Corporation with feedback from external vendors and the JEDEC Fully-Buffered DIMM Link Signaling Task Group.

FBDIMM HIGH SPEED DIFFERENTIAL PTP LINK AT 1.5 V

(From JEDEC Board ballot JCB-06-01, JCB-06-60, JCB-06-61, and JCB-06-62, formulated under the cognizance of the JC-16 on Interface technology.)

1 Scope

This specification defines the high-speed differential point-to-point signaling link for FBDIMM, operating at the buffer supply voltage of 1.5V that is provided at the FBDIMM DIMM connector. This specification also applies to FBDIMM host chips which may operate with a different supply voltage. The link consists of a transmitter and a receiver and the interconnect in between them. The transmitter sends serialized bits into a lane and the receiver accepts the electrical signals of the serialized bits and transforms them into a serialized bit-stream. The first generation FBDIMM link is being specified to operate from 3.2 to 4.8 Gb/s. The specifications are defined for three distinct bit-rates of operation: 3.2 Gb/s, 4.0 Gb/s and 4.8 Gb/s.

The link utilizes a derived clock approach and transmitter de-emphasis to compensate for channel loss characteristics. The link definition has the flexibility to accommodate future silicon enhancement circuits such as forwarded clocking or advanced equalization techniques to meet future signaling targets.

1.1 Structure

The specification is defined in four sections, covering the general signaling specifications for the silicon I/O:

Section 1 covers the scope of the document, and defines important terms.

Section 2 lists key reference documents.

Section 3 defines important terms.

Section 4 defines the interface requirements and is divided into four subsections:

Section 4.1 defines the clocking requirements.

Section 4.2 defines common requirements for both transmitter and receiver.

Section 4.3 defines requirements that are unique to the transmitter.

Section 4.4 defines requirements that are unique to the receiver.

Section 5 defines measurement and compliance testing procedures.

The interconnect between transmitter and receiver is not directly specified but implied by the difference between receiver and transmitter specifications. The interconnect needs to have a smooth enough characteristic to be operational at the frequencies which it is intended to support.

1.2 Interconnect Definition

The overall budget for voltage and timing margins are divided into transmitter (TX), interconnect, and receiver (RX) specifications. The link signaling specifications defines the TX and RX requirements at the package pins. In the context of this specification, the interconnect consists of everything between the pins at a transmitter package and the pins of a receiver package. The interconnect components in FBDIMM are socket(s) (if used), PCB (printed circuit board(s)) and connector(s).

Interconnect voltage and timing budgets are derived from the output specifications of the TX and the input specifications for the RX. Note that the TX and RX termination (specified in Table 4.3 and Table 4.4) and the test load are $50\ \Omega$ (specified in Section 5). Figure 1.1 depicts the compliance measurement points to capture each portion of the budget. The transmitter and receiver parameters are defined into test loads. This methodology ensures that the channel interactions are not included in the TX and RX measurement.

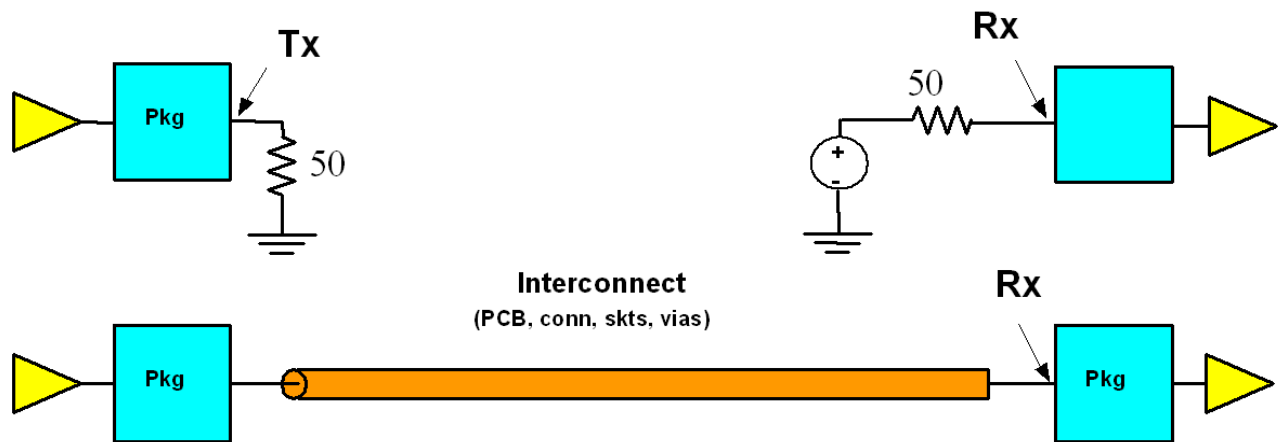


Figure 1.1 — TX to RX Connection

The transmitter, receiver, and reference clock specifications presented in Section 4 have been derived based on analysis of two specific interconnects: a host-to-first-DIMM interconnect and a DIMM-to-DIMM interconnect. The interconnect descriptions provided below are not intended to be used as a design specification. System designers must perform thorough analysis of any proposed FBD interconnect.

The interconnect model used to analyze the host-to-first-DIMM configuration has the following components:

- MB trace (host to connector): 3.0 to 12.0 inches
- Optional riser card trace: connector to connector: 2.0 to 5.0 inches
- DIMM trace (DIMM connector to AMB): 0.33 to 2.0 inches

The interconnect model used to analyze the DIMM-to-DIMM configuration has the following components:

- DIMM trace (AMB to DIMM connector): 0.33 to 2.0 inches
- Motherboard trace: connector to connector: 0.5 to 2.0 inches
- DIMM trace (DIMM connector to AMB): 0.33 to 2.0 inches

1.2 Interconnect Definition

The analysis was performed assuming FR4 PCB dielectric for both motherboard and DIMM; the differential impedance (Z_{DIFF}) was $85\ \Omega \pm 15\%$ for motherboard and DIMM stripline traces and was $85\ \Omega \pm 20\%$ for DIMM microstrip traces. Note that using the above description as a system design recipe is not enough to guarantee a working channel. The range of achievable lengths may be narrower or wider than the above, depending on materials, stackups, trace geometries, and other design choices.

2 References

The following documents contain provisions that, through references in this text, constitute provisions of this specification. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this specification are encouraged to investigate the possibility of applying the most recent editions of the referenced documents below. For undated references, the latest edition of the document referred to applies.

JEDEC JC-40, FBDIMM Architecture and Protocol Draft Specification

INTEL, FBD240 Connector Draft Specification

JEDEC JC-40, Advanced Memory Buffer Design Draft Speciation

JEDEC JC-45, FB4300/5300/6400 DDR Fully Buffered DIMM Design Specification

JEDEC MO-256B, Fully Buffered Dual Inline Memory Module Family. (Module Outline)

JEDEC SO-003, FBDIMM Socket Outline

JEDEC JESD22A114, Electrostatic Discharge (ESD) Sensitivity Testing (HBM)

3 Terms and Definitions

3.1 D+ and D-

The D+ and D- terms used in this document are used to indicate the two conductors or signals of a differential signaling pair.

3.2 Lane

One differential pair in one direction, consisting of a D+ and a D- conductor.

3.3 Port

In physical terms, a group of transmitters and receivers physically located on the same chip that define a Link.

3 Terms and Definitions (cont'd)

3.4 Link

A dual-simplex communications path between two components. The collection of two Ports and their interconnecting Lanes.

3.5 Differential Signaling

A Differential Signal is defined by taking the voltage difference between two conductors. In this specification, a differential signal or differential pair is comprised of a voltage on a positive conductor, **VD+**, and a negative conductor, **VD-**. The differential voltage (**VDIFF**) is defined as the difference of the positive conductor voltage and the negative conductor voltage (**VDIFF = VD+ - VD-**). The Common Mode Voltage (**VCM**) is defined as the average or mean voltage present on the same differential pair (**VCM = [VD+ + VD-]/2**).

This document's electrical specifications often refer to peak-to-peak measurements or peak measurements, which are defined by the following equations.

VDIFFp-p = (2*max|VD+ - VD-|) (This applies to a symmetric differential swing)

VDIFFp-p = (max|VD+ - VD-| {VD+ > VD-} + max|VD+ - VD-| {VD+ < VD-}) (This applies to an asymmetric differential swing.)

VDIFFp = (max|VD+ - VD-|) (This applies to a symmetric differential swing)

VDIFFp = (max|VD+ - VD-| {VD+ > VD-}) or (max|VD+ - VD-| {VD+ < VD-}) which ever is greater (This applies to an asymmetric differential swing.)

VCMp = (max|VD+ + VD-|/2)

NOTE The maximum value is calculated on a per unit interval evaluation. The maximum function as described is implicit for all peak-to-peak and peak equations throughout the rest of this section, and thus a max function will not appear in any following representations of these equations.

In this section, DC is defined as all frequency components below Fdc = 30 kHz. AC is defined as all frequency components at or above Fdc = 30 kHz. These definitions pertain to all voltage and current specifications.

An example waveform is shown in Figure 3.1. In this waveform the differential peak-peak signal is approximately 0.6 V, the differential peak signal is approximately 0.3 V and the common mode is approximately 0.25 V.

3 Terms and Definitions (cont'd)

3.5 Differential Signaling

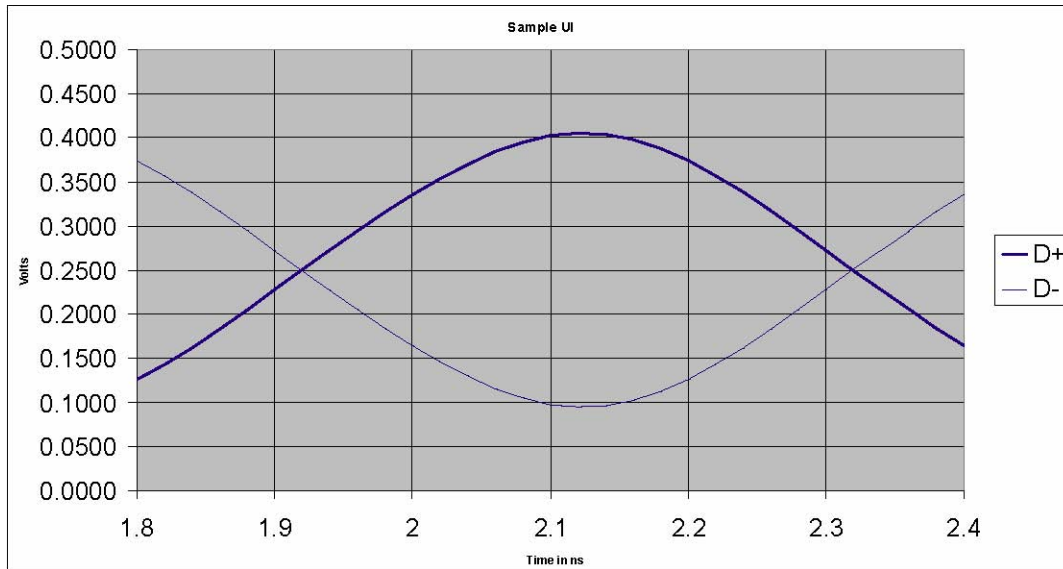


Figure 3.1 — Sample Differential Signal

3.6 Unit Interval (UI)

Given a <...1010...> data pattern, the Unit Interval is the value measured by averaging the time interval between voltage transitions, over a time interval long enough to make all intentional frequency modulation of the source clock negligible. The UI will be different depending on the data rate of operation.

3.7 Transition Density in Transmitted Signals

The FBDIMM link doesn't prescribe encoding. However the link bit stream needs to maintain a minimum transition density. The transition density is defined as the number of transitions that occurs either from 0 to 1 or from 1 to 0 within any bit stream of a prescribed length. The minimum prescribed transition density Transition-Density_min is:

6 transitions per 512 bits: FBDIMM at 3.2 Gb/s, 4.0 Gb/s and 4.8 Gb/s

The prescribed minimum is required to enable phase tracking of the received data by the receiver while at the same time minimize the overhead requirements.

3 Terms and Definitions (cont'd)

3.8 Jitter and BER

Jitter is defined as the deviation in the edges of a sequence of data bits from their ideal timing positions. This deviation can be in phase, period or duty cycle. Jitter is further categorized into random jitter and deterministic jitter. The total jitter is the convolution of the probability density for all the independent jitter sources. The random jitter magnitude can be approximated as Gaussian and can be used to estimate the bit error ratio (BER) of the link. In this document the allocation to random jitter and deterministic jitter has not been separately specified. The total jitter must support a maximum BER of 10^{-12} . The methods for measuring BER compliance are still being evaluated.

3.9 De-emphasis

De-emphasis is the engineering term used to describe the technique of utilizing a voltage swing reduction of non-transition bits. Figure 3.2 shows an example of a de-emphasized differential signal. De-emphasis is different from pre-emphasis in that non-transition bits are reduced in voltage as opposed to an increase in voltage swing for transition bits with pre-emphasis. De-emphasis is included to minimize Inter-symbol interference (ISI) due to the difference in loss across the frequency band where the main energy of the transmitted bit patterns is located. De-emphasis must be implemented when multiple bits of the same polarity are output in succession. Subsequent bits are driven at a differential voltage level below the first bit and individual bits are always driven at the full voltage level, for normal operation.

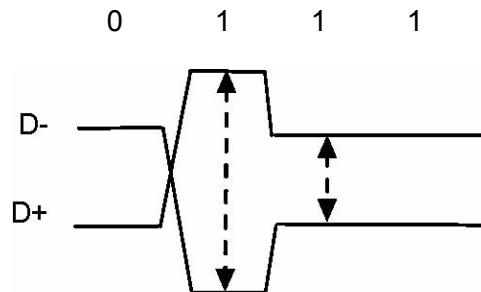


Figure 3.2 — De-emphasis

3.10 Electrical Idle (EI)

The condition when both conductors of a differential pair are at 0 volt (grounded) level. Electrical idle is primarily used in power saving and inactive states (i.e., DISABLE).

3.11 Reference Clock

The reference clock network consists of the clock generator and the clock buffer that drives the PLL of any front-end transmitter or receiver. The same reference clock shall be transmitted to the front-end of the chips at both ends of the link. The reference clock signal shall meet the High-Speed Current Steering Logic (HCSL) specification.

3 Terms and Definitions (cont'd)

3.12 Front-End Transmitter and Receiver

The differential transmitter consists of pre-driver, driver and package signal traces ending at the package pin. The receiver consists of the input package pins and signal traces leading to the input sampling amplifier, recovery circuit for the sampling clock phases and appropriate deskew circuits for passing the received data to the back-end. A depiction is in Figure 3.3.

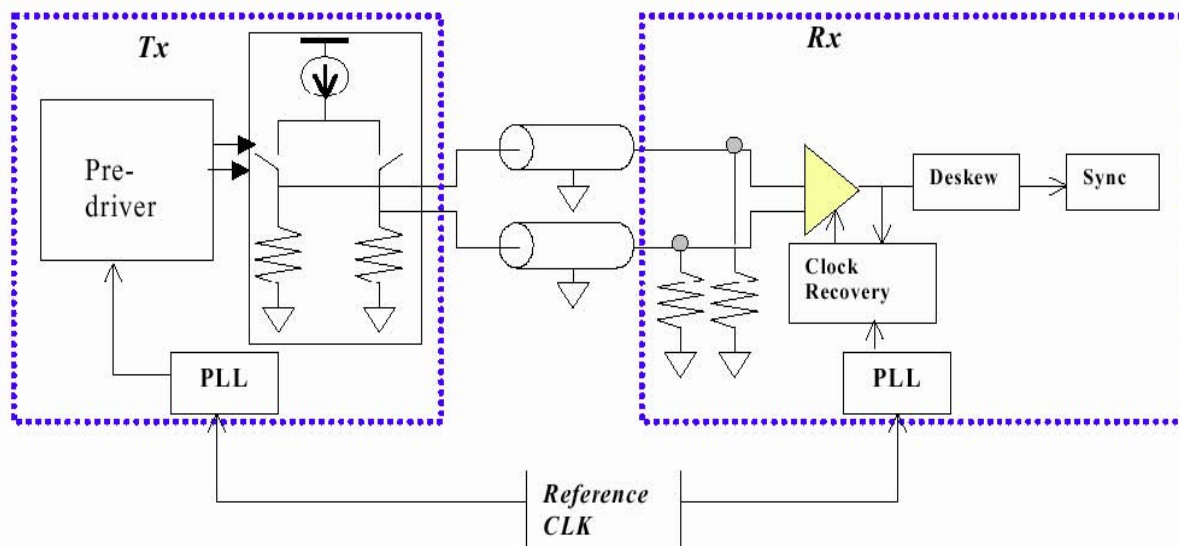


Figure 3.3 — TX to RX Connection

Figure 3.3 shows an example of the connection for one lane at the TX-RX level. The appropriate phase of the receiver end sampling clock is derived from the transmitted data. The connection between the two physical layer front-ends is DC coupled.

The following rules shall be obeyed by the link:

- 1) The transmitter output and the receiver input is VSS referenced.
- 2) Each TX-RX bit connection between two components through the interconnect channel must be DC coupled.
- 3) The signal stream from TX-RX shall maintain a minimum transition density Transition-Density_{min} (specified earlier).

Additional specifications for the transmitter front-end and the receiver front-end are in Section 4.

3 Terms and Definitions (cont'd)

3.13 List of Abbreviations and Definitions

This document uses the following abbreviations and definitions:

Abbreviation	Definition
AC	Alternating Current
AMB	Advanced Memory Buffer
BER	Bit Error Ratio
BIST	Built-in Self Test
CAL	Crosstalk Aggressor Lane: any lane that can influence the Lane Under Test (other than itself)
CDF	Cumulative Distribution Function
CDR	Clock and Data Recovery
CM	Common Mode
dB	Decibel .One tenth of the common logarithm of the ratio of relative powers, equal to 0.1 B (bel)
DC	Direct Current
DDJ	Data Dependent Jitter: a bounded distribution of jitter, with amplitude fully correlated to the data pattern sampling it, measured by its peak-to-peak value for a given pattern
DIMM	Dual Inline Memory Module
DJ	Deterministic Jitter: an even distribution of jitter, measured by its effective mean shift on a convolved Gaussian Jitter
DUT	Device Under Test: the AMB component that is being tested
EI	Electrical idle, where both conductors of a differential pair are at VSS level
EMI	Electro Magnetic Interference
End components	Components at either end of the FBDIMM channel, i.e. the host and the last AMB
ESD	Electro Static Discharge
FB(D)	Fully-Buffered (DIMM)
HCSL	High-speed Current Steering Logic
Host	Memory controller agent on an FBDIMM channel
Intermediate components	Any FBDIMM component that is not at either end of the channel
Interconnect	
ISI	Inter Symbol Interference
MEMBIST	Memory Built-in Self Test
Mesochronous	Same frequency with unknown (but fixed) phase relationship
Northbound	The direction of signals running from the furthest DIMM toward the host
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)
LUT	Lane Under Test: the lane for which the specification is being validated
PDF	Probability Density Function
PLL	Phase Locked Loop

3 Terms and Definitions (cont'd)

3.13 List of Abbreviations and Definitions (cont'd)

Abbreviation	Definition
PTP	Point To Point
PTH	Plated Through-Hole
PVT	Process, Voltage and Temperature
rad/s	Radians per second. Unit of angular frequency measure
RJ	Random Jitter: an unbounded Gaussian distributed jitter, defined by its RMS variance
RX	Receiver
SE	Single Ended
SI	Signal Integrity
Simplex	Simplex means that communication can only flow in one direction
SJ	Sinusoidal Jitter: a jitter distribution caused by a sinusoidal amplitude modulation
Southbound	The direction of signals running from the host controller toward the DIMMs
SSC	Spread Spectrum Clocking. Utilized to lower EMI.
SSO	Simultaneously Switching Outputs
TP_AMB	Test Point AMB: the ball of the AMB package
TX	Transmitter
UI	Unit Interval. Time period per data bit.
VSS	Ground (0V)
99.7% Confidence Level	Defines that the result derived from a measurement, is a confidence interval in which a measurement or trial falls corresponding to a probability of 99.7%. The confidence interval of interest is symmetrically placed around the mean.

NOTE The terms host, chipset and memory controller are used interchangeably throughout the rest of this document. The term motherboard is used as a generic term to describe the PCB onto which the memory controller is mounted. Actual implementations could have distributed memory controllers mounted on separate boards.

4 Specification Details

4.1 Clocking Specifications

4.1.1 HCSL reference clocks

To reduce jitter and allow for future silicon fabrication process changes, HCSL (High-Speed Current Steering Logic) clocks are used, as illustrated in Figure 4.1. The nominal single-ended swing for each clock is 0 to 0.7 V. The same system clock shall be transmitted to the two components at the ends of the link, if necessary, through connector(s).

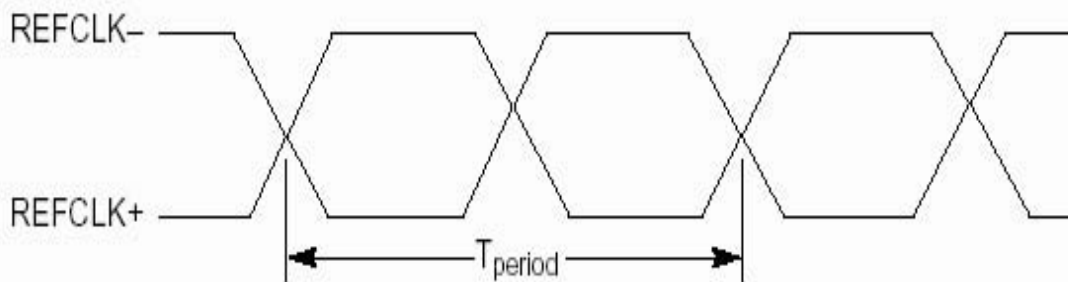


Figure 4.1 — Differential Reference CLK Waveforms

The reference clock frequency is 1/24 of the link data rate, e.g., 166.67 MHz for a data rate of 4.0 Gb/s. The reference clock pair is routed point-to-point to each device from the system board.

The FBDIMM channel utilizes mesochronous clocking, i.e., the phase relationship between TX reference clock and RX reference clock is unspecified. However, in order to limit the jitter difference between TX and RX there is an upper limit for the phase difference between data and reference clock at the RX (also known as the transport delay, specified in Table 4.1).

The clocks must be routed according to best-known clock routing rules for SI and EMI performance. The routing of each signal in any given clock pair between the clock source and the connector must be well matched in length (< 5 mils) and appropriately spaced away from other non-clock signals to avoid excessive crosstalk.

4.1.2 Reference Clock Frequency Tolerance

The frequency of the reference clock has a static tolerance, and a temporal variation. This temporal part varies due to the spread spectrum modulation and due to the mean period of the phase noise over different periods of integration.

The implementation of the multiplying PLL in the AMB should be aware that the frequency tracking capabilities of the integrated VCO should be capable of following the mean period variation. For example as the forward tracking bandwidth of PLL is increased, then the variation of the mean period will increase. As the bandwidth requirements of the PLL are well defined within the standard, it is possible to define exactly the expected maximum frequency tracking requirements of the VCO.

4.1 Clocking Specifications (cont'd)

4.1.2 Reference Clock Frequency Tolerance (cont'd)

To be able to measure the maximum tracking frequency, the reference clock phase is filtered by an equivalent 2nd order PLL transfer function represents the worst case, i.e., maximum bandwidth and maximum peaking, in the frequency domain. [Need to fix subscripts in equation below]:

$$\frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \quad (4.1)$$

After multiplying these frequency domain filters by the reference clock phase jitter spectrum, the spectra is converted back into the time domain, and the maximum instantaneous frequency is measured. To ensure that a true peak value has been calculated, sufficient edge samples must be used to ensure that the filtered underlying random source has reached a peak value for the link's target BER.

The methods used to implement the measurement of reference clock jitter are beyond the scope of this specification, any testing method may be used that will provide a mathematically equivalent result. This function is not meant as a requirement for an implementation. It is used as a bounding function for modeling purposes to establish the limits for the f_{3dB} frequency and the maximum peaking. Other implementations that can meet at least the roll off and limit the peaking given by this function are also acceptable.

The temporal variation referred to above is specified in Table 4.1 as the “reference clock dynamic frequency,” or $f_{Refclk-dyn}$. Table 4.2 indicates how this dynamic frequency range differs from the absolute frequency range.

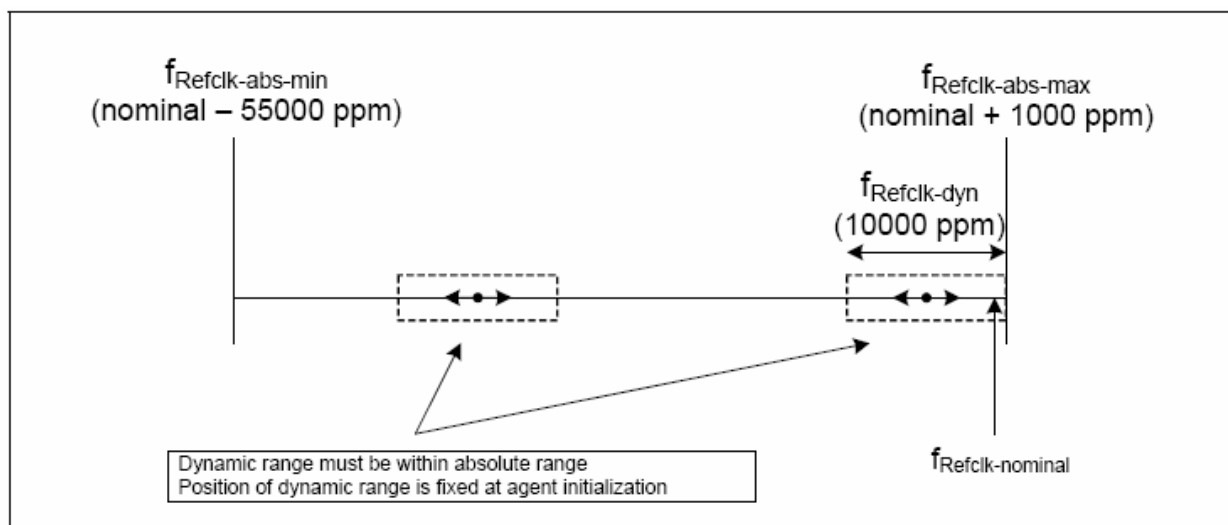


Figure 4.2 — Reference Clock Absolute and Dynamic Ranges

4.1 Clocking Specifications (cont'd)

4.1.3 Spread Spectrum Clocking (SSC)

Spread Spectrum Clock (SSC) with up to -0.5% down spread in frequency shall be supported. The frequency of the clock and therefore bit rate can be modulated from 0% to -0.5% of the nominal data rate/frequency, at a modulation rate in the range between 30 kHz and 33 kHz. The modulation profile of SSC shall be able to provide optimal or close to optimal EMI reduction. Typical profiles include triangular or “Hershey kiss” profile.

4.1.4 Reference Clock Jitter Spectrum

Different devices may have different phase jitter¹ tracking behaviors due to variation of the jitter transfer function of their PLLs, transport delays between transmitter and receiver, and differences in the propagation delays in the devices. In order for the FBDIMM channel function properly when the transmitter and receiver utilize devices with different phase jitter tracking behavior, a specification of the reference clock jitter spectrum is necessary.

To be able to measure jitter¹ on the reference clock and translate this directly into a data eye closure at the receiver, the reference clock phase jitter is filtered by a phase jitter transfer function that represents the worst case mismatch between transmitter and receiver phase tracking. Figure 4.3 shows the four filter functions defined for 4.8 Gb/s. After multiplying these frequency domain filters by the reference clock phase jitter spectrum, the SSC from the reference clock is separated from the spectrum. After converting these spectra back into the time domain, peak-to-peak amplitude of the SSC spectrum and the RMS of the remaining spectrum is measured, and the maximum is then found for the four filter functions. To ensure that a stable RMS of the spectrum is calculated, sufficient edge samples must be used to ensure that the RMS is valid at the link's target BER.

The methods used to implement the measurement of reference clock jitter are beyond the scope of this specification, any testing method may be used that will provide a mathematically equivalent result.

¹ Phase jitter is defined as the difference between the actual position of a clock edge and the edge of an ideal clock whose period is constant and is the average period of clock being measured.

4.1 Clocking Specifications(cont'd)

4.1.4 Reference clock Jitter Spectrum (cont'd)

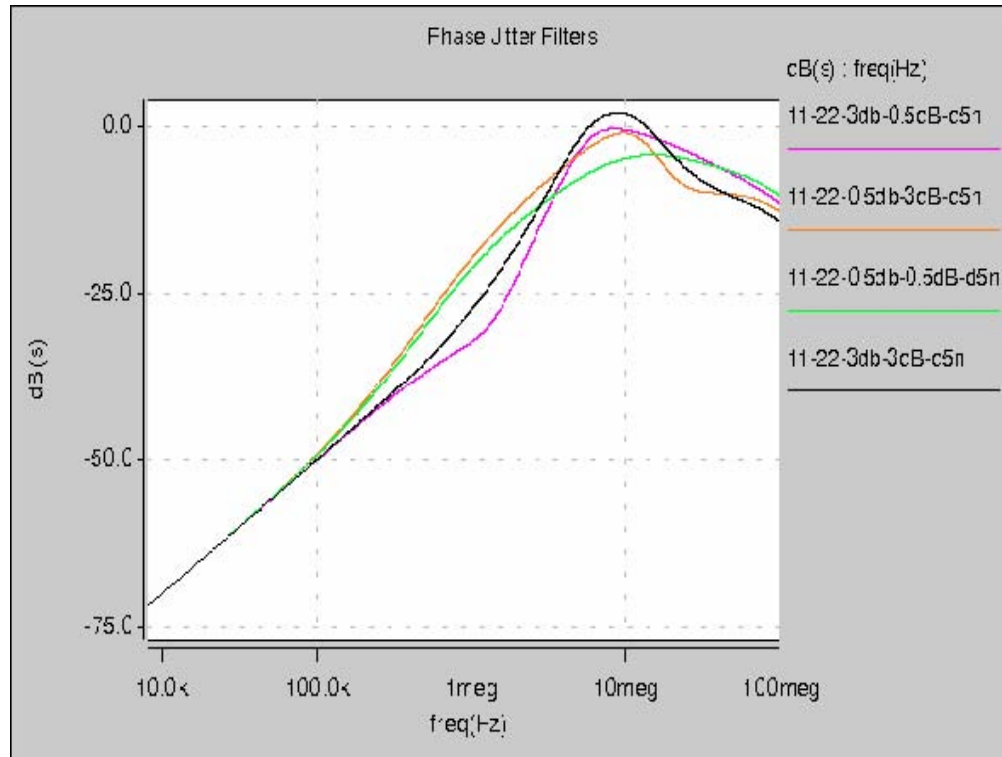


Figure 4.3 — Phase Jitter Filter for Reference Clocks

The specification uses a second-order PLL transfer function to approximate the jitter transfer function of a device's PLL. Actual PLLs used in typical CMOS processes are sampled systems often using third-order or higher order transfer functions. However, they can all be approximated by a second-order transfer function. The transfer function assuming second order PLLs is defined by the following s domain equation:

$$H(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} e^{-sT_D} - \frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \right] \quad (4.2)$$

In this equation, ζ_1 and ζ_2 are the damping factors for PLL 1 and 2, and ω_{n1} and ω_{n2} are the natural frequencies for PLL 1 and 2. The variable T_D represents the total transport delay measured from the sample clock to the data measured around the loop through Rx PLL, clock distribution delays, Tx PLL, and TX data flight time (see Figure 4.9).

This function is not meant as a requirement for an implementation. It is used as a bounding function for modeling purposes to establish the limits for the f_{3dB} frequency and the maximum peaking. Other implementations that can meet at least the roll off and limit the peaking given by this function are also acceptable.