

JEDEC STANDARD

POD18 - 1.8 V Pseudo Open Drain I/O

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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POD18 - 1.8 V PSEUDO OPEN DRAIN I/O

(From JEDEC Board Ballot JCB-06-27, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the dc and ac single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.8 V Pseudo Open Drain I/Os. The 1.8 V Pseudo Open Drain interface, also known as POD18, is primarily used to communicate with GDDR3 SGRAM devices.

2 Operating conditions

Table 1 — DC Electrical Characteristics and Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	1.7	1.8	1.9	V
I/O Supply Voltage	VDDQ	1.7	1.8	1.9	V
I/O Reference Voltage	VREF	$0.69 * VDDQ$	$0.70 * VDDQ$	$0.71 * VDDQ$	V
Input High (Logic 1) Voltage	VIH (DC)	$VREF + 0.15$	-		V
Input Low (Logic 0) Voltage	VIL (DC)	-	-	$VREF - 0.15$	V
Input Leakage Current Any Input $0V \leq V_{IN} \leq VDD$ (All other pins not under test = 0V)	II	-5	-	5	μA
Output Leakage Current (DQs are disabled; $0V \leq V_{out} \leq VDDQ$)	Ioz	-5	-	5	μA
Output Logic LOW	VOL (DC)	-	-	0.76	V

Table 2 — AC Input Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input High (Logic 1) Voltage; DQ	VIH (AC)	$VREF + 0.250$	-	-	V
Input Low (Logic 0) Voltage; DQ	VIL (AC)	-	-	$VREF - 0.250$	V
Clock Input Differential Voltage; CK & CK#	VID (AC)	0.5	-	$VDDQ + 0.5$	V
Clock Input Crossing Point Voltage; CK & CK#	VIX (AC)	$VREF - 0.15$	$0.70 * VDDQ$	$VREF + 0.15$	V