

JEDEC STANDARD

POD15 - 1.5V Pseudo Open Drain I/O

JESD8-20A
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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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POD15 - 1.5V PSEUDO OPEN DRAIN I/O

(From JEDEC Board ballot JCB-09-71, formulated under the cognizance of the JC-16 Committee on Voltage Level and Electrical Interface.)

1 Scope

This standard defines the dc and ac single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.5 V Pseudo Open Drain I/Os. The 1.5 V Pseudo Open Drain interface, also known as POD15, is primarily used to communicate with GDDR4 and GDDR5 SGRAM devices.

2 Operating conditions

Table 1 — DC Operating Conditions

Parameter	Symbol	POD15			Unit	Note
		Min	Typ	Max		
Device Supply Voltage	VDD	1.455	1.5	1.545	V	1
Output Supply Voltage	VDDQ	1.455	1.5	1.545	V	1
Reference Voltage	VREF	0.69 * VDDQ		0.71 * VDDQ	V	2, 9
Reference Voltage for DQ and DBI# pins	VREFD	0.69 * VDDQ		0.71 * VDDQ	V	2, 3, 10
Reference Voltage for DQ and DBI# pins	VREFD2	0.49 * VDDQ		0.51 * VDDQ	V	2, 3, 4, 10
External Reference Voltage for address and command	VREFC	0.69 * VDDQ		0.71 * VDDQ	V	5, 10
DC Input Logic HIGH Voltage	VIH (DC)	VREF + 0.12			V	9
DC Input Logic LOW Voltage	VIL (DC)			VREF - 0.12	V	9
DC Input Logic HIGH Voltage for address and command	VIHA (DC)	VREFC + 0.15			V	10
DC Input Logic LOW Voltage for address and command	VILA (DC)			VREFC - 0.15	V	10
DC Input Logic HIGH Voltage for DQ and DBI# pins with VREFD	VIHD (DC)	VREFD + 0.10			V	10
DC Input Logic LOW Voltage for DQ and DBI# pins with VREFD	VILD (DC)			VREFD - 0.10	V	10
DC Input Logic HIGH Voltage for DQ and DBI# pins with VREFD2	VIHD2 (DC)	VREFD2 + 0.30			V	10
DC Input Logic LOW Voltage for DQ and DBI# pins with VREFD2	VILD2 (DC)			VREFD2 - 0.30	V	10
Input Logic HIGH Voltage for RESET#, SEN, MF	VIHR	VDDQ - 0.50			V	10
Input Logic LOW Voltage for RESET#, SEN, MF	VILR			0.30	V	10
Input logic HIGH voltage for EDC1/2 (x16 mode detect)	VIHX	VDDQ - 0.3			V	8, 10
Input logic LOW voltage for EDC1/2 (x16 mode detect)	VILX			0.30	V	8, 10
Input Leakage Current Any Input 0V ≤ VIN ≤ VDDQ (All other pins not under test = 0V)	II				μA	
Output Leakage Current (DQs are disabled; 0V ≤ Vout ≤ VDDQ)	Ioz				μA	
Output Logic LOW Voltage	VOL (DC)			0.62	V	

NOTE 1 GDDR4 and GDDR5 SGRAMs are designed to tolerate PCB designs with separate VDD and VDDQ power regulators.

NOTE 2 AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.

NOTE 3 Source of Reference Voltage and control of Reference Voltage for DQ and DBI# pins is determined by VREFD, Half VREFD, Auto VREFD, VREFD MERGE and VREFD Offsets mode registers.

NOTE 4 VREFD Offsets are not supported with VREFD2.

NOTE 5 External VREFC is to be provided by the controller as there is no other alternative supply.

NOTE 6 DQ/DBI# input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC) or VREFD2 crossing and VIHD2(AC) or VILD2(AC).

NOTE 7 ADR/CMD input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).

NOTE 8 VIHx and VILx define the voltage levels for the receiver that detects x32 or x16 mode with RESET# going High.

NOTE 9 Applicable to GDDR4 or other interface with a single VREF for the device.

NOTE 10 Applicable to GDDR5 or other interface with multiple VREF pins and levels.