

# **JEDEC STANDARD**

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## **HSUL\_12 LPDDR2 and LPDDR3 I/O with Optional ODT**

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### **JESD8-22B**

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## HSUL\_12 LPDDR2 and LPDDR3 I/O with Optional ODT

(From JEDEC Board Ballot JCB-14-01, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

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### 1 Scope

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This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the High Speed Unterminated Logic (HSUL\_12) logic switching range, nominally 0 V to 1.2 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages.

#### 1.1 Standard structure

The standard is defined in four clauses:

The first clause defines absolute maximum DC rating requirements common to all compliant ICs.

The second clause defines pertinent supply voltage requirements.

The third clause defines the minimum dc and ac input parametric requirements and ac test conditions for inputs on compliant devices.

The fourth clause specifies the minimum required output characteristics of, and ac test conditions for, compliant outputs targeted for various application environments.

Input parametric requirements and Output specifications are divided into two classes where necessary, Class I for LPDDR2, and Class II for LPDDR3 which operates at higher frequency than LPDDR2.

#### 1.2 Rationale and assumptions

The HSUL\_12 standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve the bus power consumption when operating at higher speed. This bus is mainly for point-to-point unterminated bus topology.

The standard defines both the ac and dc input signal values. Making this distinction is important for the design of the high gain, differential receivers that are required. The ac values indicate the voltage levels at which the receiver must meet its timing specifications. The dc values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. Once the receiver input has crossed the ac value, the receiver will change to the new logic state. The new logic state will then be maintained as long as the input stays beyond the dc threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform.

## 2 Absolute Maximum Ratings

### 2.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 1 — Absolute Maximum DC Ratings**

| Parameter                                                                                                                         | Symbol                                | Min  | Max | Units | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------|---------------------------------------|------|-----|-------|-------|
| VDDCA supply voltage relative to VSSCA                                                                                            | VDDCA                                 | -0.4 | 1.6 | V     | 2     |
| VDDQ supply voltage relative to VSSQ                                                                                              | VDDQ                                  | -0.4 | 1.6 | V     | 1     |
| Voltage on any ball relative to VSS                                                                                               | V <sub>IN</sub> ,<br>V <sub>OUT</sub> | -0.4 | 1.6 | V     |       |
| NOTE 1 $V_{REFDQ} \leq 0.6 \times VDDQ$ ; however, $V_{REFDQ}$ may be $\geq VDDQ$ provided that $V_{REFDQ} \leq 300\text{mV}$ .   |                                       |      |     |       |       |
| NOTE 2 $V_{REFCA} \leq 0.6 \times VDDCA$ ; however, $V_{REFCA}$ may be $\geq VDDCA$ provided that $V_{REFCA} \leq 300\text{mV}$ . |                                       |      |     |       |       |

## 3 AC & DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

### 3.1 Recommended DC Operating Conditions

**Table 2 — Recommended HSUL\_12 DC Operating Conditions**

| Symbol | Min  | Typ  | Max | DRAM               | Unit |
|--------|------|------|-----|--------------------|------|
| VDDCA  | 1.14 | 1.20 | 1.3 | Input Buffer Power | V    |
| VDDQ   | 1.14 | 1.20 | 1.3 | I/O Buffer Power   | V    |

## 4 AC and DC Input Measurement Levels

### 4.1 AC and DC Logic Input Levels for Single-Ended Signals

#### 4.1.1 AC and DC Input Levels for Single-Ended CA and CS<sub>n</sub> Signals

**Table 3 — Single-Ended AC and DC Input Levels for CA and CS<sub>n</sub> Inputs, Class I**

| Symbol                                                                                                                                                                                                                                                                                                                                                                                                                         | Parameter                                           | 1066 to 466 Mbps         |                          | 400 to 200 Mbps          |                          | Unit | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|--------------------------|--------------------------|--------------------------|--------------------------|------|-------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                     | Min                      | Max                      | Min                      | Max                      |      |       |
| V <sub>IHCA</sub> (AC)                                                                                                                                                                                                                                                                                                                                                                                                         | AC input logic high                                 | V <sub>ref</sub> + 0.220 | Note 2                   | V <sub>ref</sub> + 0.300 | Note 2                   | V    | 1, 2  |
| V <sub>ILCA</sub> (AC)                                                                                                                                                                                                                                                                                                                                                                                                         | AC input logic low                                  | Note 2                   | V <sub>ref</sub> - 0.220 | Note 2                   | V <sub>ref</sub> - 0.300 | V    | 1, 2  |
| V <sub>IHCA</sub> (DC)                                                                                                                                                                                                                                                                                                                                                                                                         | DC input logic high                                 | V <sub>ref</sub> + 0.130 | V <sub>DDCA</sub>        | V <sub>ref</sub> + 0.200 | V <sub>DDCA</sub>        | V    | 1     |
| V <sub>ILCA</sub> (DC)                                                                                                                                                                                                                                                                                                                                                                                                         | DC input logic low                                  | V <sub>SSCA</sub>        | V <sub>ref</sub> - 0.130 | V <sub>SSCA</sub>        | V <sub>ref</sub> - 0.200 | V    | 1     |
| V <sub>RefCA</sub> (DC)                                                                                                                                                                                                                                                                                                                                                                                                        | Reference Voltage for CA and CS <sub>n</sub> inputs | 0.49 * V <sub>DDCA</sub> | 0.51 * V <sub>DDCA</sub> | 0.49 * V <sub>DDCA</sub> | 0.51 * V <sub>DDCA</sub> | V    | 3, 4  |
| NOTE 1 For CA and CS <sub>n</sub> input only pins. V <sub>ref</sub> = V <sub>refCA</sub> (DC).<br>NOTE 2 See 5.5, Overshoot and undershoot specifications<br>NOTE 3 The ac peak noise on V <sub>RefCA</sub> may not allow V <sub>RefCA</sub> to deviate from V <sub>RefCA</sub> (DC) by more than +/-1% V <sub>DDCA</sub> (for reference: approx. +/- 12 mV).<br>NOTE 4 For reference: approx. V <sub>DDCA</sub> /2 +/- 12 mV. |                                                     |                          |                          |                          |                          |      |       |

**Table 4 — Single-Ended AC and DC Input Levels for CA and CS<sub>n</sub> inputs, Class II**

| Symbol                                                                                                                                                                                                                                                                                                                                                                                                                         | Parameter                                           | 1333/1600                |                          | 1866/2133                |                          | Unit | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|--------------------------|--------------------------|--------------------------|--------------------------|------|-------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                     | Min                      | Max                      | Min                      | Max                      |      |       |
| V <sub>IHCA</sub> (AC)                                                                                                                                                                                                                                                                                                                                                                                                         | AC input logic high                                 | V <sub>Ref</sub> + 0.150 | Note 2                   | V <sub>Ref</sub> + 0.135 | Note 2                   | V    | 1, 2  |
| V <sub>ILCA</sub> (AC)                                                                                                                                                                                                                                                                                                                                                                                                         | AC input logic low                                  | Note 2                   | V <sub>Ref</sub> - 0.150 | Note 2                   | V <sub>Ref</sub> - 0.135 | V    | 1, 2  |
| V <sub>IHCA</sub> (DC)                                                                                                                                                                                                                                                                                                                                                                                                         | DC input logic high                                 | V <sub>Ref</sub> + 0.100 | V <sub>DDCA</sub>        | V <sub>Ref</sub> + 0.100 | V <sub>DDCA</sub>        | V    | 1     |
| V <sub>ILCA</sub> (DC)                                                                                                                                                                                                                                                                                                                                                                                                         | DC input logic low                                  | V <sub>SSCA</sub>        | V <sub>Ref</sub> - 0.100 | V <sub>SSCA</sub>        | V <sub>Ref</sub> - 0.100 | V    | 1     |
| V <sub>RefCA</sub> (DC)                                                                                                                                                                                                                                                                                                                                                                                                        | Reference Voltage for CA and CS <sub>n</sub> inputs | 0.49 * V <sub>DDCA</sub> | 0.51 * V <sub>DDCA</sub> | 0.49 * V <sub>DDCA</sub> | 0.51 * V <sub>DDCA</sub> | V    | 3, 4  |
| NOTE 1 For CA and CS <sub>n</sub> input only pins. V <sub>Ref</sub> = V <sub>RefCA</sub> (DC).<br>NOTE 2 See 5.5, Overshoot and undershoot specifications<br>NOTE 3 The ac peak noise on V <sub>RefCA</sub> may not allow V <sub>RefCA</sub> to deviate from V <sub>RefCA</sub> (DC) by more than +/-1% V <sub>DDCA</sub> (for reference: approx. +/- 12 mV).<br>NOTE 4 For reference: approx. V <sub>DDCA</sub> /2 +/- 12 mV. |                                                     |                          |                          |                          |                          |      |       |

#### 4.1 AC and DC Logic Input Levels for Single-Ended Signals

##### 4.1.2 AC and DC Input Levels for CKE

**Table 5 — Single-Ended AC and DC Input Levels for CKE,Class I**

| Symbol                                                  | Parameter            | Min              | Max              | Unit | Notes |
|---------------------------------------------------------|----------------------|------------------|------------------|------|-------|
| $V_{IHCKE}$                                             | CKE Input High Level | $0.8 * V_{DDCA}$ | Note 1           | V    | 1     |
| $V_{ILCKE}$                                             | CKE Input Low Level  | Note 1           | $0.2 * V_{DDCA}$ | V    | 1     |
| NOTE 1 See 5.5, Overshoot and undershoot specifications |                      |                  |                  |      |       |

**Table 6 — Single-Ended AC and DC Input Levels for CKE,Class II**

| Symbol                                                  | Parameter            | Min               | Max               | Unit | Notes |
|---------------------------------------------------------|----------------------|-------------------|-------------------|------|-------|
| $V_{IHCKE}$                                             | CKE Input High Level | $0.65 * V_{DDCA}$ | Note 1            | V    | 1     |
| $V_{ILCKE}$                                             | CKE Input Low Level  | Note 1            | $0.35 * V_{DDCA}$ | V    | 1     |
| NOTE 1 See 5.5, Overshoot and undershoot specifications |                      |                   |                   |      |       |

##### 4.1.3 AC and DC Input Levels for Single-Ended Data Signals

**Table 7 — Single-Ended AC and DC Input Levels for DQ and DM,Class I**

| Symbol                                                                                                                                                                                                                                                                                                                                              | Parameter                           | 1066 to 466 Mbps  |                   | 400 to 200 Mbps   |                   | Unit | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|-------------------|-------------------|-------------------|-------------------|------|-------|
|                                                                                                                                                                                                                                                                                                                                                     |                                     | Min               | Max               | Min               | Max               |      |       |
| $V_{IHDQ}(AC)$                                                                                                                                                                                                                                                                                                                                      | AC input logic high                 | $V_{ref} + 0.220$ | Note 2            | $V_{ref} + 0.300$ | Note 2            | V    | 1, 2  |
| $V_{ILDQ}(AC)$                                                                                                                                                                                                                                                                                                                                      | AC input logic low                  | Note 2            | $V_{ref} - 0.220$ | Note 2            | $V_{ref} - 0.300$ | V    | 1, 2  |
| $V_{IHDQ}(DC)$                                                                                                                                                                                                                                                                                                                                      | DC input logic high                 | $V_{ref} + 0.130$ | $V_{DDQ}$         | $V_{ref} + 0.200$ | $V_{DDQ}$         | V    | 1     |
| $V_{ILDQ}(DC)$                                                                                                                                                                                                                                                                                                                                      | DC input logic low                  | $V_{SSQ}$         | $V_{ref} - 0.130$ | $V_{SSQ}$         | $V_{ref} - 0.200$ | V    | 1     |
| $V_{RefDQ}(DC)$                                                                                                                                                                                                                                                                                                                                     | Reference Voltage for DQ, DM inputs | $0.49 * V_{DDQ}$  | $0.51 * V_{DDQ}$  | $0.49 * V_{DDQ}$  | $0.51 * V_{DDQ}$  | V    | 3, 4  |
| NOTE 1 For DQ input only pins. $V_{ref} = V_{refDQ}(DC)$ .<br>NOTE 2 See 5.5, Overshoot and undershoot specifications<br>NOTE 3 The ac peak noise on $V_{RefDQ}$ may not allow $V_{RefDQ}$ to deviate from $V_{RefDQ}(DC)$ by more than +/-1% $V_{DDQ}$ (for reference: approx. +/- 12 mV).<br>NOTE 4 For reference: approx. $V_{DDQ}/2$ +/- 12 mV. |                                     |                   |                   |                   |                   |      |       |

#### 4.1 AC and DC Logic Input Levels for Single-Ended Signals (cont'd)

##### 4.1.3 AC and DC Input Levels for Single-Ended Data Signals (cont'd)

**Table 8 — Single-Ended AC and DC Input Levels for DQ and DM, Class II**

| Symbol                               | Parameter                           | 1333/1600                     |                               | 1866/2133                     |                               | Unit | Notes   |
|--------------------------------------|-------------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|------|---------|
|                                      |                                     | Min                           | Max                           | Min                           | Max                           |      |         |
| $V_{IHDQ}(AC)$                       | AC input logic high                 | $V_{Ref} + 0.150$             | Note 2                        | $V_{Ref} + 0.135$             | Note 2                        | V    | 1, 2, 5 |
| $V_{ILDQ}(AC)$                       | AC input logic low                  | Note 2                        | $V_{Ref} - 0.150$             | Note 2                        | $V_{Ref} - 0.135$             | V    | 1, 2, 5 |
| $V_{IHDQ}(DC)$                       | DC input logic high                 | $V_{Ref} + 0.100$             | $V_{DDQ}$                     | $V_{Ref} + 0.100$             | $V_{DDQ}$                     | V    | 1       |
| $V_{ILDQ}(DC)$                       | DC input logic low                  | $V_{SSQ}$                     | $V_{Ref} - 0.100$             | $V_{SSQ}$                     | $V_{Ref} - 0.100$             | V    | 1       |
| $V_{RefDQ}(DC)$<br>(DQ ODT disabled) | Reference Voltage for DQ, DM inputs | $0.49 * V_{DDQ}$              | $0.51 * V_{DDQ}$              | $0.49 * V_{DDQ}$              | $0.51 * V_{DDQ}$              | V    | 3, 4    |
| $V_{RefDQ}(DC)$<br>(DQ ODT enabled)  | Reference Voltage for DQ, DM inputs | $V_{ODTR}/2 - 0.01 * V_{DDQ}$ | $V_{ODTR}/2 + 0.01 * V_{DDQ}$ | $V_{ODTR}/2 - 0.01 * V_{DDQ}$ | $V_{ODTR}/2 + 0.01 * V_{DDQ}$ | V    | 3, 5, 6 |

NOTE 1 For DQ input only pins.  $V_{Ref} = V_{RefDQ}(DC)$ .

NOTE 2 See 5.5, Overshoot and undershoot specifications

NOTE 3 The ac peak noise on  $V_{RefDQ}$  may not allow  $V_{RefDQ}$  to deviate from  $V_{RefDQ}(DC)$  by more than  $\pm 1\% V_{DDQ}$  (for reference: approx.  $\pm 12$  mV).

NOTE 4 For reference: approx.  $V_{DDQ}/2 \pm 12$  mV.

NOTE 5 For reference: approx.  $V_{ODTR}/2 \pm 12$  mV.

NOTE 6 The nominal mode register programmed value for  $R_{ODT}$  and the nominal controller output impedance  $R_{ON}$  are used for the calculation of  $V_{ODTR}$ . For testing purposes a controller  $R_{ON}$  value of 50  $\Omega$  is used.

$$V_{ODTR} = \frac{2R_{ON} + R_{TT}}{R_{ON} + R_{TT}} \times V_{DDQ}$$

## 4.2 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages  $V_{\text{RefCA}}$  and  $V_{\text{RefDQ}}$  are illustrated in Figure 1. It shows a valid reference voltage  $V_{\text{Ref}}(t)$  as a function of time.

( $V_{\text{Ref}}$  stands for  $V_{\text{RefCA}}$  and  $V_{\text{RefDQ}}$  likewise). VDD stands for VDDCA for  $V_{\text{RefCA}}$  and VDDQ for  $V_{\text{RefDQ}}$ .  $V_{\text{Ref}}(\text{DC})$  is the linear average of  $V_{\text{Ref}}(t)$  over a very long period of time (e.g., 1 sec) and is specified as a fraction of the linear average of VDDQ or VDDCA also over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirements in Table 3, Table 4, Table 7, and Table 8. Furthermore  $V_{\text{Ref}}(t)$  may temporarily deviate from  $V_{\text{Ref}}(\text{DC})$  by no more than  $\pm 1\%$  VDD.  $V_{\text{Ref}}(t)$  cannot track noise on VDDQ or VDDCA if this would send  $V_{\text{Ref}}$  outside these specifications.:

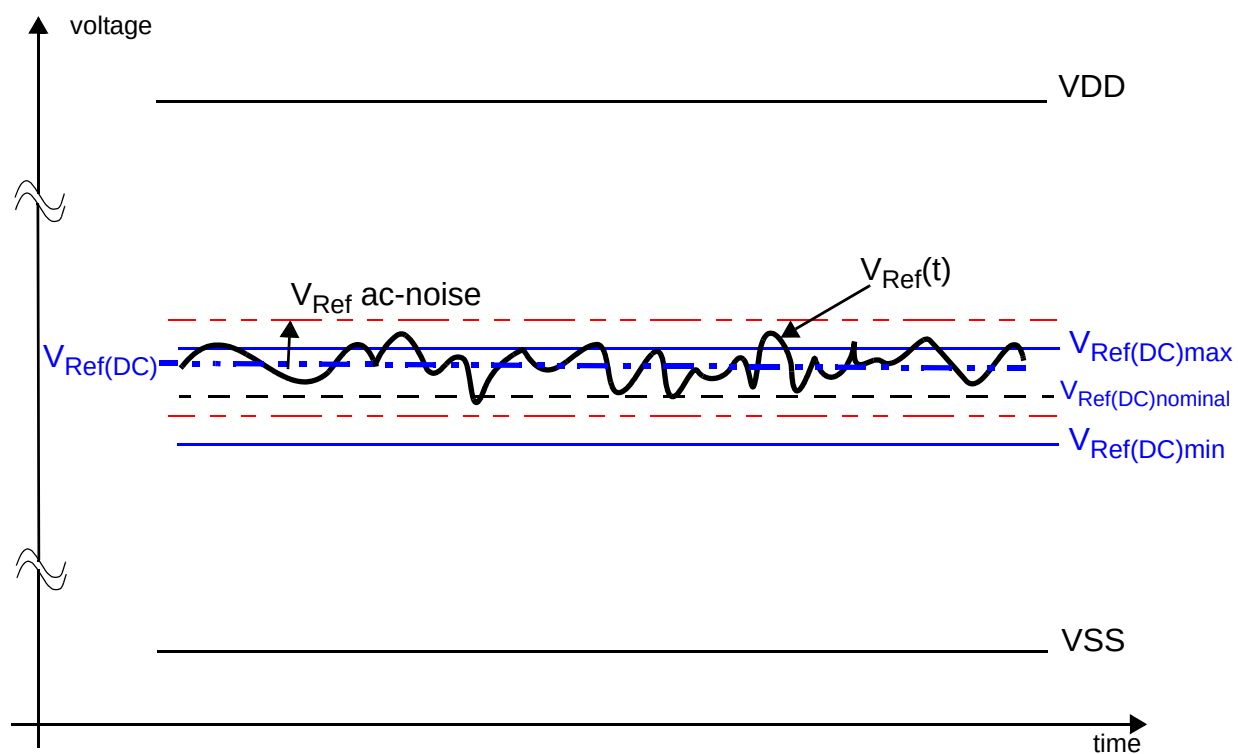


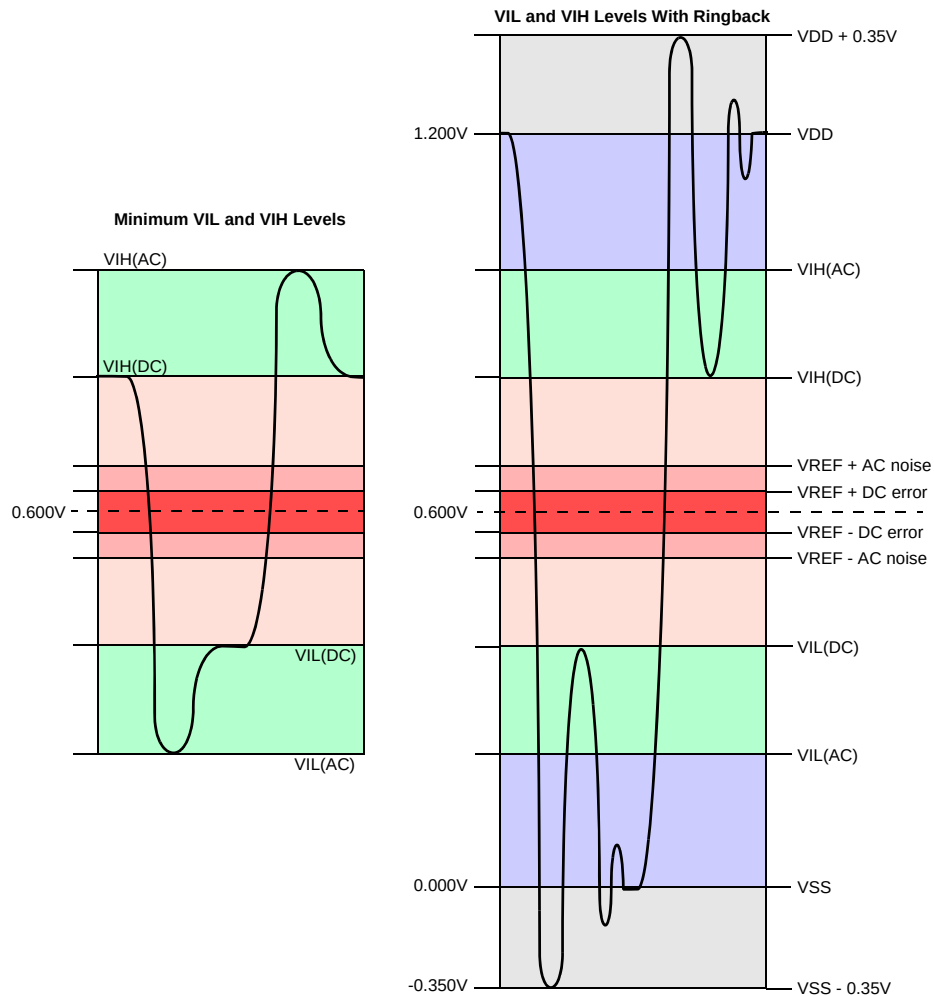
**Figure 1 — Illustration of  $V_{\text{Ref}}(\text{DC})$  tolerance and  $V_{\text{Ref}}$  ac-noise limits**

The voltage levels for setup and hold time measurements  $V_{\text{IH}}(\text{AC})$ ,  $V_{\text{IH}}(\text{DC})$ ,  $V_{\text{IL}}(\text{AC})$  and  $V_{\text{IL}}(\text{DC})$  are dependent on  $V_{\text{Ref}}$ . “ $V_{\text{Ref}}$ ” shall be understood as  $V_{\text{Ref}}(\text{DC})$ , as defined in Figure 1.

This clarifies that dc-variations of  $V_{\text{Ref}}$  affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for  $V_{\text{REF}}$  deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the LPDDR2 and LPDDR3 setup/hold specification and derating values need to include time and voltage associated with  $V_{\text{Ref}}$  ac-noise. Timing and voltage effects due to ac-noise on  $V_{\text{Ref}}$  up to the specified limit ( $\pm 1\%$  of VDD) are included in LPDDR2 and LPDDR3 timings and their associated deratings.

## 4.3 Input Signal



NOTE 1 Numbers reflect nominal values.

NOTE 2 For CA0-9, CK\_t, CK\_c, and CS\_n, VDD stands for VDDCA. For DQ, DM/DNV, DQS\_t, and DQS\_c, VDD stands for VDDQ.

NOTE 3 For CA0-9, CK\_t, CK\_c, and CS\_n, VSS stands for VSSCA. For DQ, DM/DNV, DQS\_t, and DQS\_c, VSS stands for VSSQ.

**Figure 2 — Input Signal**

## 4.4 AC and DC Logic Input Levels for Differential Signals

### 4.4.1 Differential signal definition

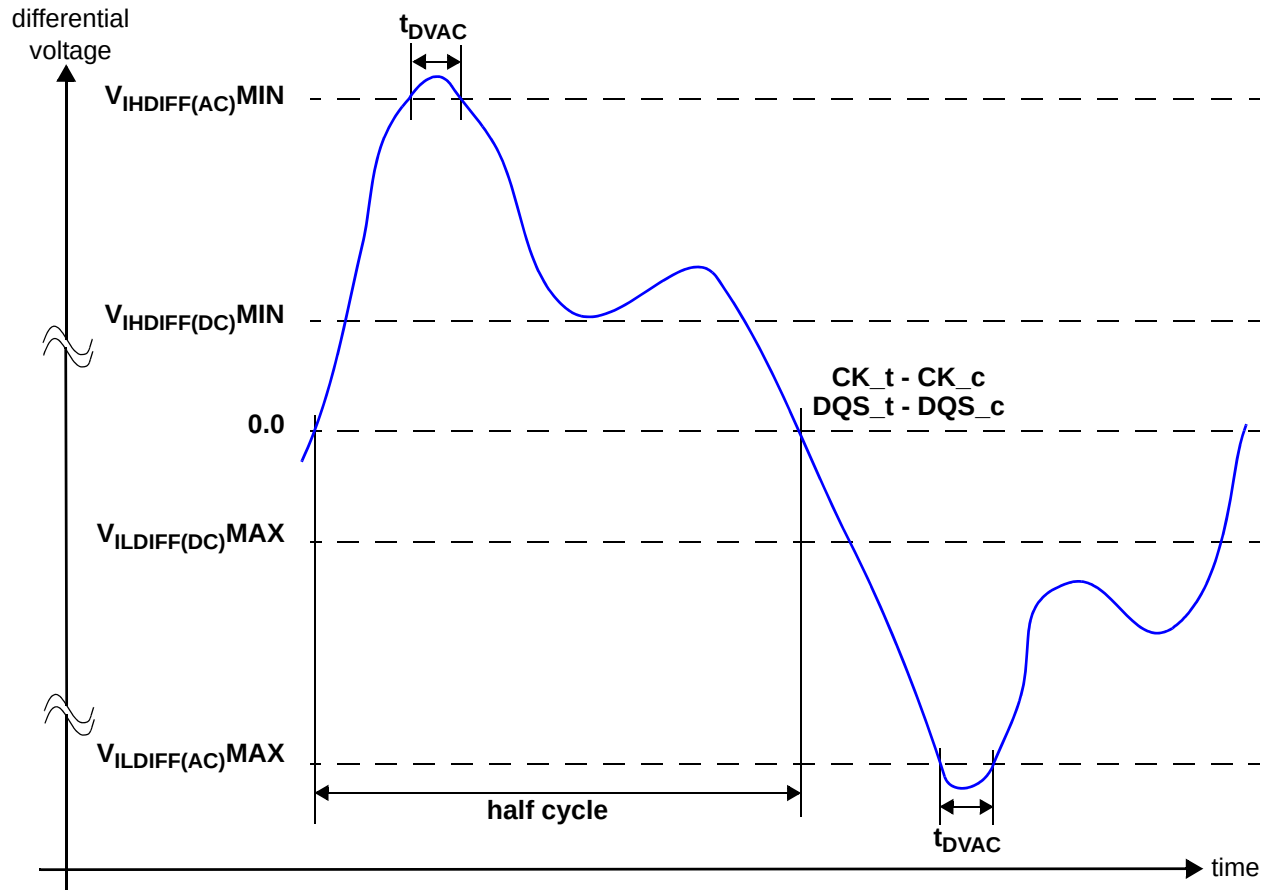


Figure 3 — Definition of differential ac-swing and “time above ac-level”  $t_{DVAC}$