

EIA/JEDEC STANDARD

High Speed Transceiver Logic (HSTL) A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits

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HIGH SPEED TRANSCEIVER LOGIC (HSTL)
A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE
STANDARD FOR DIGITAL INTEGRATED CIRCUITS

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(From JEDEC Council Ballot JCB-94-64, formulated under the cognizance of the JC-16 Committee on Electrical Interface and Power Supply Standards for Electronic Components.)

1 Scope

This standard defines the input and output specifications and ac test conditions for devices that are designed to operate in the HSTL logic switching range, nominally 0 V to 1.5 V. The standard may be applied to integrated circuits operating on any V_{DD} supply voltage as long as the output drivers do not drive beyond the value of V_{OH} (max.) shown in this standard. In most cases the use of a separate output supply voltage source (V_{DDQ}) is expected, though other implementations that meet the parametric requirements of this standard are allowed.

Single ended and differential input buffer specifications as well as various push-pull output driver specifications are incorporated in this standard. The standard is intended to provide for interoperability between all types of HSTL compliant digital integrated circuits.

1.1 Standard structure

The standard is defined in three sections. The first section defines pertinent supply voltage requirements common to all compliant integrated circuits. The second section defines the minimum dc and ac input parametric requirements and ac test conditions for both single ended and differential inputs on compliant devices. The third section specifies the minimum required output characteristics of, and ac test conditions for compliant outputs targeted for various application environments (e.g. lumped capacitive load, unterminated transmission line (T-line) load, series terminated T-line load, parallel terminated T-line load). The output specifications are divided into four classes (Class I through Class IV) depending upon output drive requirements.

A given integrated circuit need not be equipped with all four classes of output drivers, but each must support at least one to claim HSTL output compliance. The full input reference level (V_{REF}) range specified is required on each integrated circuit in order to allow any HSTL integrated circuit to receive signals from any HSTL output driver.

1.2 Rationale and assumptions

Historically, integrated circuit interface specifications have rightly been substantially influenced by the semiconductor technology and I/O buffer circuits used to implement the integrated circuits at hand. So interface specifications have been born of the “optimum” circuit structure for the technology in question (e.g. the rail-to-rail outputs and the supply voltage-ratioed input buffers of “CMOS” devices, or the near-ground asymmetric logic levels of bipolar TTL integrated circuits, or the below-ground logic levels of bipolar ECL integrated circuits). Although not intended to be “suboptimum”, this standard places a higher priority on flexibility and being technology independent, even supply voltage independent, than on being tailored to a particular semiconductor technology.

To this end, this standard has been developed with voltage scalable and technology independent I/O structures in mind, namely differential amplifier inputs (with one input internally tied to a user-supplied input reference voltage, V_{REF} , for single ended inputs) and outputs that use output power supply inputs (V_{DDQ}) that may be different from those that operate the integrated circuit (V_{DD}).

Although exceeding the requirements of the standard is clearly not required for compliance, it is reasonably likely that the buffer circuit structures employed by compliant devices will be amenable to extended ranges of operation, making adaptation of HSTL compliant integrated circuits to other, yet lower voltage interface logic levels reasonably straightforward.

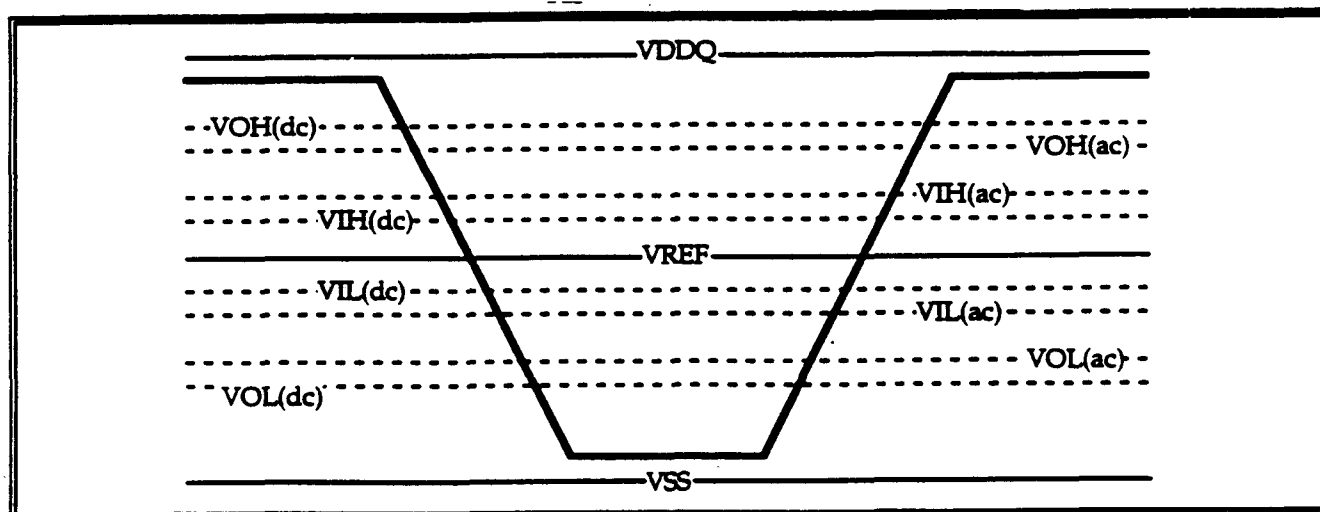


Figure 2.1 — HSTL I/O levels

2 Supply voltage and logic input levels

2.1 Supply voltage levels

Table 2.1 — Supply voltage levels

Symbol	Parameter	Min.	Nom	Max.	Units	Notes
V_{DD}	Device supply voltage	n/a		n/a	V	1
V_{DDQ}	Output supply voltage	1.4	1.5	1.6	V	
V_{REF}	Input reference voltage	0.68	0.75	0.90	V	2, 3

NOTES

- 1 There is no specific device V_{DD} supply voltage requirement for HSTL compliance. Early implementations are expected with 3.3 V or 2.5 V supply voltages, but other device supply voltage levels are acceptable.
- 2 V_{REF} of the receiving device should track the variations in the dc value of the V_{DDQ} of the sending device for best noise margins. The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user.
- 3 Peak to peak ac noise on V_{REF} may not exceed 2% V_{REF} (dc).

2.2 Single ended input parametrics

Table 2.2-a — Single ended input dc logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH}(dc)$	DC input logic high	$V_{REF} + 0.10$	$V_{DDQ} + 0.3$	V	1, 2
$V_{IL}(dc)$	DC input logic low	-0.30	$V_{REF} - 0.10$	V	2

NOTES

1 Within this standard, it is the relationship of the sending integrated circuits V_{DDQ} and the receiving integrated circuits V_{REF} that determines noise margins. However, in the case of $V_{IH}(max.)$ (i.e. input overdrive) it is the V_{DDQ} of the receiving integrated circuit that is referenced. In the case where an integrated circuit is implemented that supports HSTL inputs but has no HSTL outputs (e.g. a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 1.9 V (High corner $V_{DDQ} + 300$ mV).

2 Inputs should not be held at V_{REF} .

Table 2.2-b — Single ended input ac logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH}(ac)$	AC input logic high	$V_{REF} + 0.20$		V	
$V_{IL}(ac)$	AC input logic low		$V_{REF} - 0.20$	V	

Table 2.2-c — AC test conditions

Condition	Value	Units	Notes
Input timing measurement reference level	0.75	V	1
Input signal swing	1.0	V	2
Input signal edge rate	± 1.0	V/ns	3

NOTES

1 In all cases, input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test. Table 2.1 identifies the V_{REF} range supported in HSTL.

2 A 1.0 V input pulse level is specified to allow consistent, repeatable test results in an automatic test equipment (ATE) environment. Compliant devices must meet the $V_{IH}(ac)$ and $V_{IL}(ac)$ specifications under actual use conditions.

3 A 1 V/ns input signal edge rate is to be maintained in the 20% to 80% range of the input signal swing.