

EIA/JEDEC STANDARD

Stub Series Terminated Logic for 3.3 Volts (SSTL_3)

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Stub Series Terminated Logic for 3.3 Volts (SSTL-3)

A 3.3 V Supply Voltage based interface standard for digital integrated circuits

(From JEDEC Council Ballot JCB-96-23, formulated under the cognizance of the JC-16 Committee on Electrical Interface and Power Supply Standards for Digital Integrated Circuit Components.)

1 Scope

This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL-3 logic switching range, nominally 0 V to 3.3V. The standard may be applied to IC's operating with separate VDD and VDDQ supply voltages. In many cases VDD and VDDQ will have the same voltage level. However for noise rejection reasons, the supplies may be routed separately in the system interconnect. The VDD value is not specified in this standard other than that VDDQ value may not exceed that of VDD.

1.1 Standard structure

The standard is defined in three sections:

The first section defines pertinent supply voltage requirements common to all compliant IC's.

The second section defines the minimum dc and ac input parametric requirements and ac test conditions for inputs on compliant devices.

The third section specifies the minimum required output characteristics of, and ac test conditions for, compliant outputs targeted for various application environments. The output specifications are divided into two classes, Class I and Class II, which are distinguished by drive requirements and application.

A given IC need not be equipped with both classes of output drivers, but each must support at least one to claim SSTL-3 output compliance.

The full input reference level (VREF) range specified is required on each IC in order to allow any SSTL-3, IC to receive signals from any SSTL-3 output driver.

1.2 Rationale and assumptions

The SSTL-3 standard has been developed particularly with the objective of providing a relatively

simple upgrade path from LVTTTL designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs. External resistors provide this isolation and also reduce the on-chip power dissipation of the drivers. Busses may be terminated by resistors to an external termination voltage. Actual selection of the resistor values is a system design decision and beyond the scope of this standard. However in order to provide a basis, the driver characteristics will be derived in terms of a typical 50 Ohms environment.

While driver characteristics are derived from a 50 Ohm environment, this standard will work for other impedance levels. The system designer will be able to vary impedance levels, termination resistors and supply voltage and be able to calculate the effect on system voltage margins. This is accomplished precisely because drivers and receivers are specified independently of each other.

The standard defines a reference voltage V_{REF} which is used at the receivers as well as a voltage V_{TT} to which termination resistors are connected. In typical applications V_{TT} tracks as a ratio of V_{DDQ} . In turn V_{REF} will be given the value of V_{TT} . In some standards this ratio equals 0.5. If this value were to be applied to SSTL-3, the maximum value of V_{TT} and thus V_{REF} would be 1.8 V ($0.5 * 3.6$). In order to be more closely compatible with LVTTTL, the nominal ratio was selected to be 0.45. This leads to a typical V_{TT} and V_{REF} value of about 1.5 V if $V_{DDQ} = 3.3$ V. This value is close to the internal reference voltage in current LVTTTL designs.

2 Supply voltage and logic input levels

The standard defines both ac and dc input signal values. Making this distinction is important for the design of high gain, differential, receivers that are required. The ac values are chosen to indicate the levels at which the receiver must meet its timing specifications. The dc values are chosen such that the final logic state is unambiguously defined, that is once the receiver input has crossed this value, the receiver will change to and maintain the new logic state. The reason for this approach is that many input waveforms will include a certain amount of “ringing”. The system designer can be sure that the device will switch state a certain amount of time after the input has crossed ac threshold and not switch back as long as the input stays beyond the dc threshold. The relationship of the different levels is shown in figure 2.1. An example of ringing is illustrated in the dotted waveform.

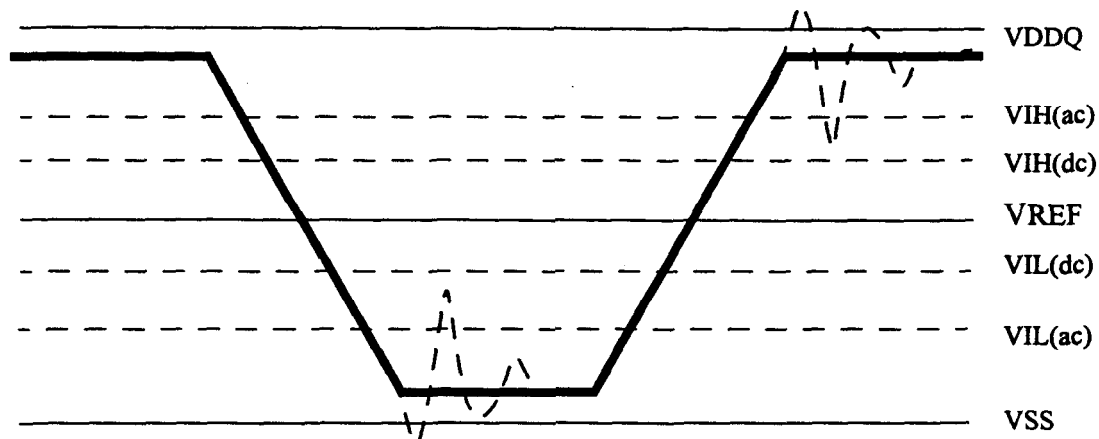


Figure 2.1 - SSTL_3 Input levels